MP4833A

32-Channel, High-Voltage Analog Switch with Output Bleed Resistors in a BGA Package

DESCRIPTION

The MP4833A is a 32-channel, high-voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors. It is designed to multiplex the transmit and receive voltages to and from multiple piezoelectric transducers (PZT), and is ideal for medical ultrasound imaging applications.

The output switches are controlled by a 32-bit serial shift register, followed by a 32-bit data latch. A data out pin (DOUT) allows multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high signal in the data latch turns on the corresponding analog switch; a logic low signal turns off the corresponding analog switch.

The MP4833A does not require any high-voltage supplies. It only requires two low-voltage supplies (3.3V and 10V). The analog switch can block or pass analog voltages up to ±90V with peak currents of up to ±2A.

The MP4833A is available in a BGA-80 (7mmx7mm) package.

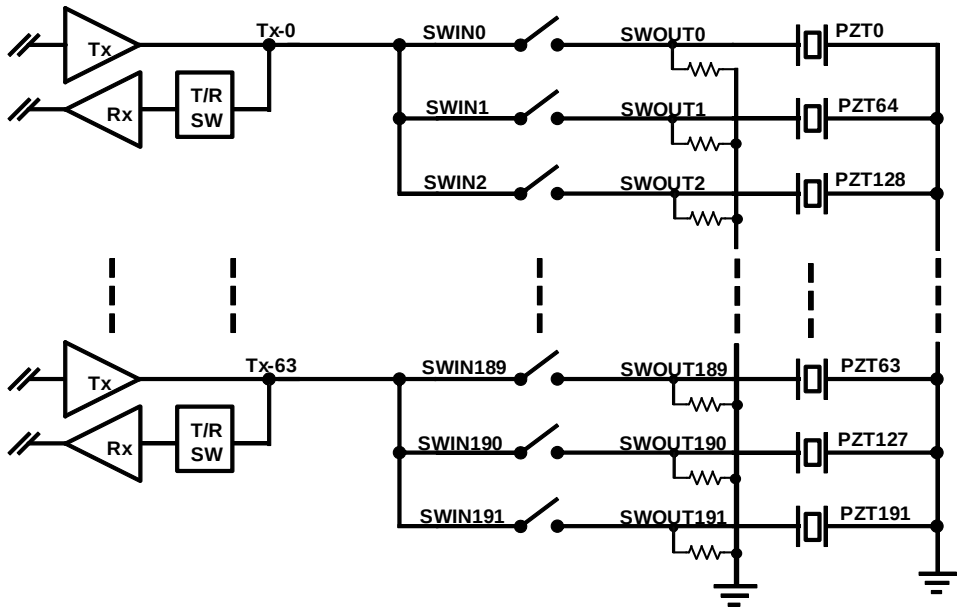
FEATURES

- No High-Voltage Supplies Required
- 32 Channels
- Up to ±90V Analog Signals
- 12.5Ω Typical Switch Resistance
- ±2A Typical Switch Peak Current
- Off-Isolation of -66dB at 5MHz
- Integrated Output Bleed Resistors
- 80MHz Clock Frequency
- Available in a BGA-80 (7mmx7mm) Package

APPLICATIONS

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT)

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP4833AGBN	BGA-80 (7mmx7mm)	*See Below*	3

* For Tray, add suffix -T (e.g. MP4833AGBN-T).

TOP MARKING

MPSYYWW

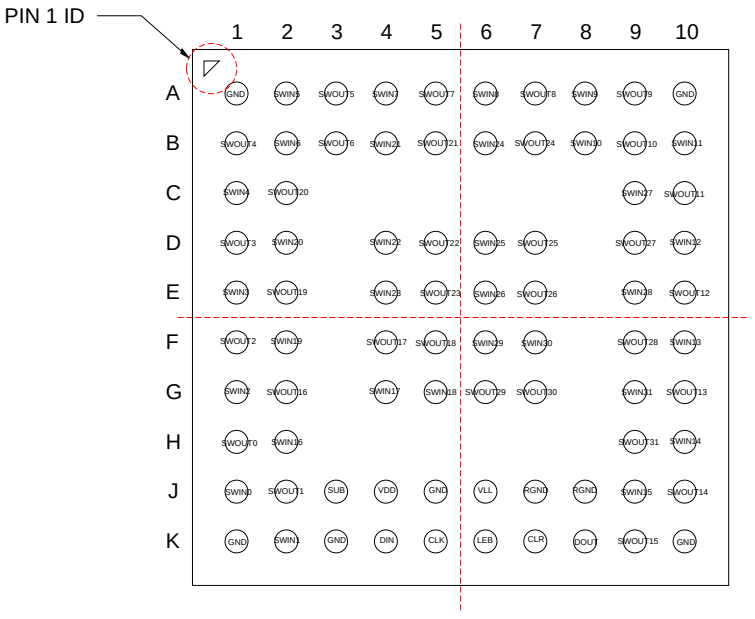
MP4833A

LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP4833A: Part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



BGA-80 (7mmx7mm)

PIN FUNCTIONS

Pin #	Name	Description
A1	GND	**Device ground.**
A2	SWIN5	**Analog switch input 5.** Connect SWIN5 to the high-voltage pulse/transmitter.
A3	SWOUT5	**Analog switch output 5.** Connect SWOUT5 to the piezoelectric transducer.
A4	SWIN7	**Analog switch input 7.** Connect SWIN7 to the high-voltage pulse/transmitter.
A5	SWOUT7	**Analog switch output 7.** Connect SWOUT7 to the piezoelectric transducer.
A6	SWIN8	**Analog switch input 8.** Connect SWIN8 to the high-voltage pulse/transmitter.
A7	SWOUT8	**Analog switch output 8.** Connect SWOUT8 to the piezoelectric transducer.
A8	SWIN9	**Analog switch input 9.** Connect SWIN9 to the high-voltage pulse/transmitter.
A9	SWOUT9	**Analog switch output 9.** Connect SWOUT9 to the piezoelectric transducer.
A10	GND	**Device ground.**
B1	SWOUT4	**Analog switch output 4.** Connect SWOUT4 to the piezoelectric transducer.
B2	SWIN6	**Analog switch input 6.** Connect SWIN6 to the high-voltage pulse/transmitter.
B3	SWOUT6	**Analog switch output 6.** Connect SWOUT6 to the piezoelectric transducer.
B4	SWIN21	**Analog switch input 21.** Connect SWIN21 to the high-voltage pulse/transmitter.
B5	SWOUT21	**Analog switch output 21.** Connect SWOUT21 to the piezoelectric transducer.
B6	SWIN24	**Analog switch input 24.** Connect SWIN24 to the high-voltage pulse/transmitter.
B7	SWOUT24	**Analog switch output 24.** Connect SWOUT24 to the piezoelectric transducer.
B8	SWIN10	**Analog switch input 10.** Connect SWIN10 to the high-voltage pulse/transmitter.
B9	SWOUT10	**Analog switch output 10.** Connect SWOUT10 to the piezoelectric transducer.
B10	SWIN11	**Analog switch input 11.** Connect SWIN11 to the high-voltage pulse/transmitter.
C1	SWIN4	**Analog switch input 4.** Connect SWIN4 to the high-voltage pulse/transmitter.
C2	SWOUT20	**Analog switch output 20.** Connect SWOUT20 to the piezoelectric transducer.
C9	SWIN27	**Analog switch input 27.** Connect SWIN27 to the high-voltage pulse/transmitter.
C10	SWOUT11	**Analog switch output 11.** Connect SWOUT11 to the piezoelectric transducer.
D1	SWOUT3	**Analog switch output 3.** Connect SWOUT3 to the piezoelectric transducer.
D2	SWIN20	**Analog switch input 20.** Connect SWIN20 to the high-voltage pulse/transmitter.
D4	SWIN22	**Analog switch input 22.** Connect SWIN22 to the high-voltage pulse/transmitter.
D5	SWOUT22	**Analog switch output 22.** Connect SWOUT22 to the piezoelectric transducer.
D6	SWIN25	**Analog switch input 25.** Connect SWIN25 to the high-voltage pulse/transmitter.
D7	SWOUT25	**Analog switch output 25.** Connect SWOUT25 to the piezoelectric transducer.
D9	SWOUT27	**Analog switch output 27.** Connect SWOUT27 to the piezoelectric transducer.
D10	SWIN12	**Analog switch input 12.** Connect SWIN12 to the high-voltage pulse/transmitter.
E1	SWIN3	**Analog switch input 3.** Connect SWIN3 to the high-voltage pulse/transmitter.
E2	SWOUT19	**Analog switch output 19.** Connect SWOUT19 to the piezoelectric transducer.
E4	SWIN23	**Analog switch input 23.** Connect SWIN23 to the high-voltage pulse/transmitter.
E5	SWOUT23	**Analog switch output 23.** Connect SWOUT23 to the piezoelectric transducer.
E6	SWIN26	**Analog switch input 26.** Connect SWIN26 to the high-voltage pulse/transmitter.
E7	SWOUT26	**Analog switch output 26.** Connect SWOUT26 to the piezoelectric transducer.
E9	SWIN28	**Analog switch input 28.** Connect SWIN28 to the high-voltage pulse/transmitter.
E10	SWOUT12	**Analog switch output 12.** Connect SWOUT12 to the piezoelectric transducer.
F1	SWOUT2	**Analog switch output 2.** Connect SWOUT2 to the piezoelectric transducer.
F2	SWIN19	**Analog switch input 19.** Connect SWIN19 to the high-voltage pulse/transmitter.
F4	SWOUT17	**Analog switch output 17.** Connect SWOUT17 to the piezoelectric transducer.
F5	SWOUT18	**Analog switch output 18.** Connect SWOUT18 to the piezoelectric transducer.
F6	SWIN29	**Analog switch input 29.** Connect SWIN29 to the high-voltage pulse/transmitter.
F7	SWIN30	**Analog switch input 30.** Connect SWIN30 to the high-voltage pulse/transmitter.
F9	SWOUT28	**Analog switch output 28.** Connect SWOUT28 to the piezoelectric transducer.
F10	SWIN13	**Analog switch input 13.** Connect SWIN13 to the high-voltage pulse/transmitter.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
G1	SWIN2	**Analog switch input 2.** Connect SWIN2 to the high-voltage pulse/transmitter.
G2	SWOUT16	**Analog switch output 16.** Connect SWOUT16 to the piezoelectric transducer.
G4	SWIN17	**Analog switch input 17.** Connect SWIN17 to the high-voltage pulse/transmitter.
G5	SWIN18	**Analog switch input 18.** Connect SWIN18 to the high-voltage pulse/transmitter.
G6	SWOUT29	**Analog switch output 29.** Connect SWOUT29 to the piezoelectric transducer.
G7	SWOUT30	**Analog switch output 30.** Connect SWOUT30 to the piezoelectric transducer.
G9	SWIN31	**Analog switch input 31.** Connect SWIN31 to the high-voltage pulse/transmitter.
G10	SWOUT13	**Analog switch output 13.** Connect SWOUT13 to the piezoelectric transducer.
H1	SWOUT0	**Analog switch output 0.** Connect SWOUT0 to the piezoelectric transducer.
H2	SWIN16	**Analog switch input 16.** Connect SWIN16 to the high-voltage pulse/transmitter.
H9	SWOUT31	**Analog switch output 31.** Connect SWOUT31 to the piezoelectric transducer.
H10	SWIN14	**Analog switch input 14.** Connect SWIN14 to the high-voltage pulse/transmitter.
J1	SWIN0	**Analog switch input 0.** Connect SWIN0 to the high-voltage pulse/transmitter.
J2	SWOUT1	**Analog switch output 1.** Connect SWOUT1 to the piezoelectric transducer.
J3	SUB	**Substrate connection.** Connect SUB to ground.
J4	VDD	**Translator supply voltage.** VDD has an operating range of 9V to 10V.
J5	GND	**Device ground.**
J6	VLL	**Translator supply voltage.** VLL has an operating range of 2.7V to 5.5V.
J7	RGND	**Output bleed resistor ground path.**
J8	RGND	**Output bleed resistor ground path.**
J9	SWIN15	**Analog switch input 15.** Connect SWIN15 to the high-voltage pulse/transmitter.
J10	SWOUT14	**Analog switch output 14.** Connect SWOUT14 to the piezoelectric transducer.
K1	GND	**Device ground.**
K2	SWIN1	**Analog switch input 1.** Connect SWIN1 to the high-voltage pulse/transmitter.
K3	GND	**Device ground.**
K4	DIN	**Logic input.** DIN is the data input for the 32-bit serial shift register.
K5	CLK	**Logic input.** CLK is the clock input for the 32-bit serial shift register. Load data into the register during the rising edge of the clock.
K6	LEB	**Logic input.** LEB is the latch enable bar for the 32-bit latch. Pull this pin logic low to transfer data from the serial shift registers to the latches; pull it high to hold the data in the latches.
K7	CLR	**Logic input.** CLR is the clear input for the 32-bit latch. Pull this pin logic high to clear the data in the latches by setting them all to 0. Data in the shift register remains unchanged.
K8	DOUT	**Logic output.** DOUT is the data output from the 32-bit serial shift register.
K9	SWOUT15	**Analog switch output 15.** Connect SWOUT15 to the piezoelectric transducer.
K10	GND	**Device ground.**

ABSOLUTE MAXIMUM RATINGS (1)

Logic supply voltage (V_{LL}) .....-0.5V to +6.6V
Translator supply voltage (V_{DD}).....-0.5V to +11V
Analog signal range (pulsed voltage) (V_{SIG}).....
.....0V to ±105V
Junction temperature .....150°C
Lead temperature .....260°C
Continuous power dissipation (T_A = 25°C) (2)
..... 2.9W
Storage temperature..... -55°C to +150°C

ESD Ratings

Human body model (HBM). .....JEDEC standard
SWOUTx.....Class 1B
SWINx.....Class 1C
Other pins.....Class 2

Recommended Operating Conditions (3)

Logic supply voltage (V_{LL}).....2.7V to 5.5V
Translator supply voltage (V_{DD}).....9V to 10V
Analog signal range (V_{SIG}) ..... 0 to ±90V
Junction temperature (T_J) ..... -25°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

BGA-80 (7mmx7mm)..... 35..... 9.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can cause excessive die temperature, which may result in permanent damage to the part.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-9, 4-layer PCB.

DC ELECTRICAL CHARACTERISTICS

V_{DD} = 10V, V_{LL} = 5V, unless otherwise noted. (5)

Parameter	Symbol	Conditions	T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Analog signal range	V_{SIG}	Applied to SWINx	0	±90	0		±90	0	±90	V
On resistance	R_{ON}	I_{SIG} = ±5mA, SWOUTx = 0V, see Figure 2 on page 10		16		12.5	19		24	Ω
		I_{SIG} = ±200mA, SWOUTx = 0V, see Figure 2 on page 10		16		12.5	19		24	
Small signal on-resistance matching	ΔR_{ON}	I_{SIG} = ±5mA, SWOUTx = 0V				5				%
Large signal on resistance (6)	R_{ONL}	I_{SIG} = ±1A, t_{PW} ≤ 500ns, duty cycle ≤ 1%, SWOUTx = 0V, see Figure 3 on page 10				13				Ω
Switch output peak current (6)	I_{SWPK}	t_{PW} < 100ns, duty cycle < 1%				±2				A
Output bleed resistor	R_{BLEED}	I_{SIG} = ±50µA	20	50	20	30	50	20	50	kΩ
Switch-off DC offset	V_{DC-OFF}	No load, no V_{SIG}, see Figure 4 on page 10		±50			±50		±50	mV
Switch-on DC offset	V_{DC-ON}	No load, no V_{SIG}, see Figure 4 on page 10		±50			±50		±50	mV
V_{LL} quiescent current	I_{LLQ}	All logic inputs are static		100			100		100	µA
V_{DD} quiescent current	I_{DDQ}	All switches on or off, SWINx = SWOUTx = GND		120			120		120	µA
V_{LL} average dynamic current	I_{LL}	f_{CLK} = 40MHz, D_{IN} = 20MHz, LE\ = H, CLR = L				4.4	12			mA
		f_{CLK} = 80MHz, D_{IN} = 40MHz, LE\ = H, CLR = L (6)				8.6				
V_{DD} average dynamic current	I_{DD}	All output switches turn on and off at 50kHz				4.6	8			mA
Logic low input voltage	V_{IL}		0	0.2 x V_{LL}	0		0.2 x V_{LL}	0	0.2 x V_{LL}	V
Logic high input voltage	V_{IH}		0.8 x V_{LL}	V_{LL}	0.8 x V_{LL}		V_{LL}	0.8 x V_{LL}	V_{LL}	V
Logic low input current	I_{IL}		-2		-2			-2		µA
Logic high input current	I_{IH}			2			2		2	µA
Logic low data out voltage	V_{OL}	I_{SINK} = 10mA		1			1		1	V
Logic high data out voltage	V_{OH}	I_{SOURCE} = 10mA	V_{LL} - 1		V_{LL} - 1			V_{LL} - 1		V
Logic input capacitance (6)	C_{IN}			10			10		10	pF

AC ELECTRICAL CHARACTERISTICS

V_{DD} = 10V, V_{LL} = 5V, unless otherwise noted. (5)

Parameter	Symbol	Conditions		T_J = 0°C		T_J = 25°C			T_J = 70°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
Clock frequency (6)	f_{CLK}	50% duty cycle	V_{LL} = 3.3V	0	40	0		40	0	40	MHz
			V_{LL} = 5V		80	0		80	0	80	
Clock rise time (6)	t_r				50			50		50	ns
Clock fall time (6)	t_f				50			50		50	ns
Set-up time from data to the rising edge of clock (6)	t_{SU}			3		3			3		ns
Hold time from the rising edge of clock to data (6)	t_H			3		3			3		ns
Set-up time before LE\ rises (6)	t_{SD}			6		6			6		ns
LE\ pulse width (6)	t_{WLE_BAR}			6		6			6		ns
Clear pulse width (6)	t_{WCLR}			6		6			6		ns
Data out propagation delay time from the rising edge of clock (6)	t_{DOLH}, t_{DOHL}	20pF on DOUT to GND		4	8	4	6	8	4	8	ns
Output switch turn-on time	t_{ON}	SWINx = 2V, SWOUTx = 50Ω to GND, see Figure 5 on page 11			2			2		2	µs
Output switch turn-off time	t_{OFF}				2			2		2	µs
Analog signal slew rate (6)	dV/dt				20			20		20	V/ns
Off isolation (6)	K_O	Freq = 5MHz, R_{LOAD} = 50Ω, see Figure 6 on page 11					-66				dB
Switch crosstalk (6)	K_{CR}	Freq = 5MHz, R_{LOAD} = 50Ω, see Figure 7 on page 11					-60				dB
Switch-off capacitance (6)	$C_{SWIN-OFF}$						10				pF
Switch-on capacitance (6)	C_{SW-ON}						13				pF
Positive output voltage spike (6)	$+V_{SPK}$	SWINx = 1kΩ to GND, SWOUTx = 50Ω to GND, see Figure 8 on page 12					16				mV
Negative output voltage spike (6)	$-V_{SPK}$						-14				mV
Output charge injection (6)	Q_{INJ}	C_{LOAD} = 1000pF, see Figure 9 on page 12					18				pC

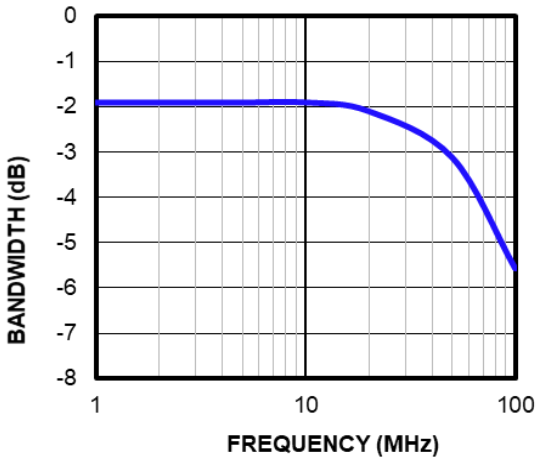
Notes:

5) Tested at 25°C in production. 0° and 70° limits are guaranteed by design and characterization.
6) Not tested in mass production. Guaranteed by design or bench characterization.

TYPICAL PERFORMANCE CHARACTERISTICS

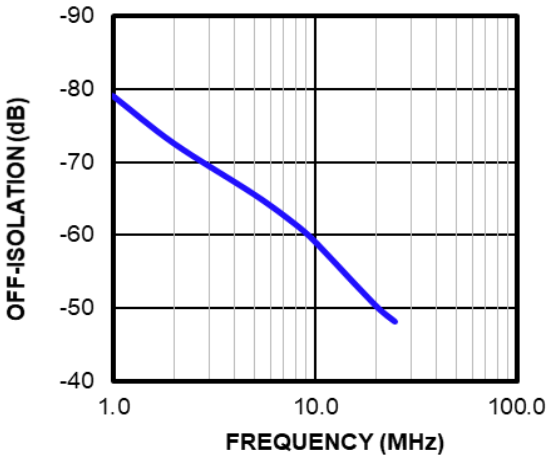
Bandwidth vs. Frequency

R_{LOAD} = 50Ω



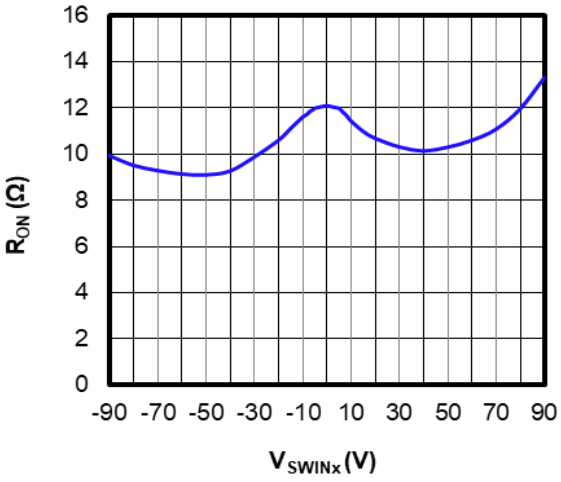
Off-Isolation vs. Frequency

R_{LOAD} = 50Ω



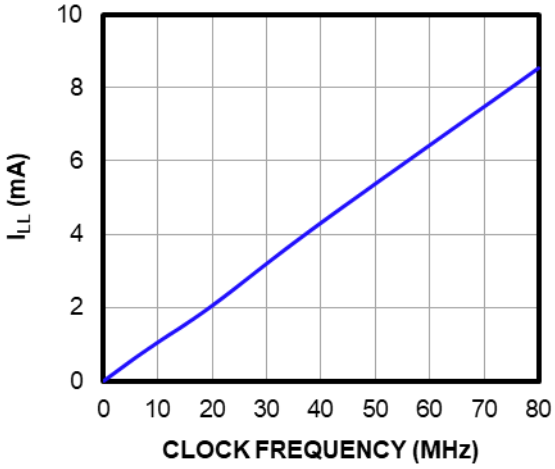
On Resistance vs. Switch Input Voltage

R_{LOAD} = 50Ω



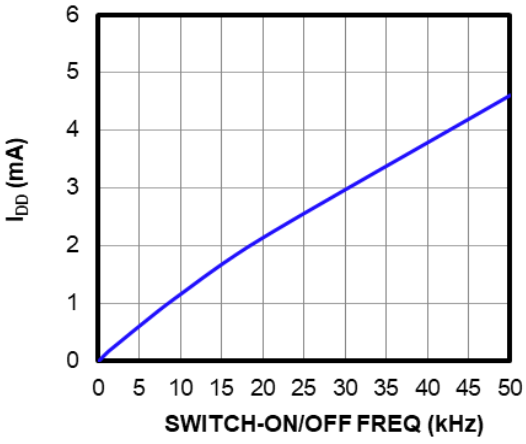
V_{LL} Average Dynamic Current vs. Clock Frequency

V_{LL} = 5V, V_{DD} = 10V



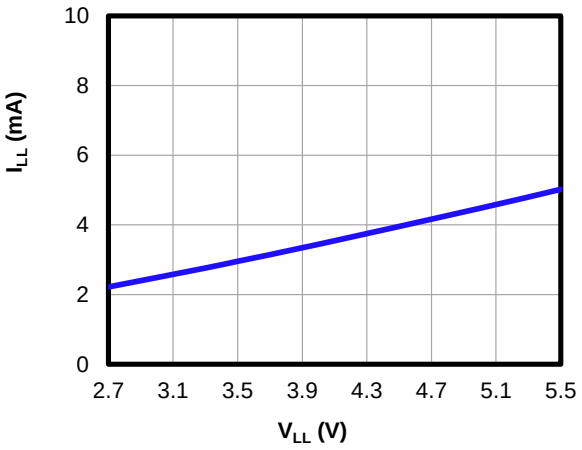
I_{DD} vs. Switch-On/Off Frequency

V_{LL} = 5V, V_{DD} = 10V,
all 32 channels switching



V_{LL} Average Dynamic Current vs. Logic Supply Voltage

CLK = 40MHz, D_{IN} = 20MHz



TIMING DIAGRAM

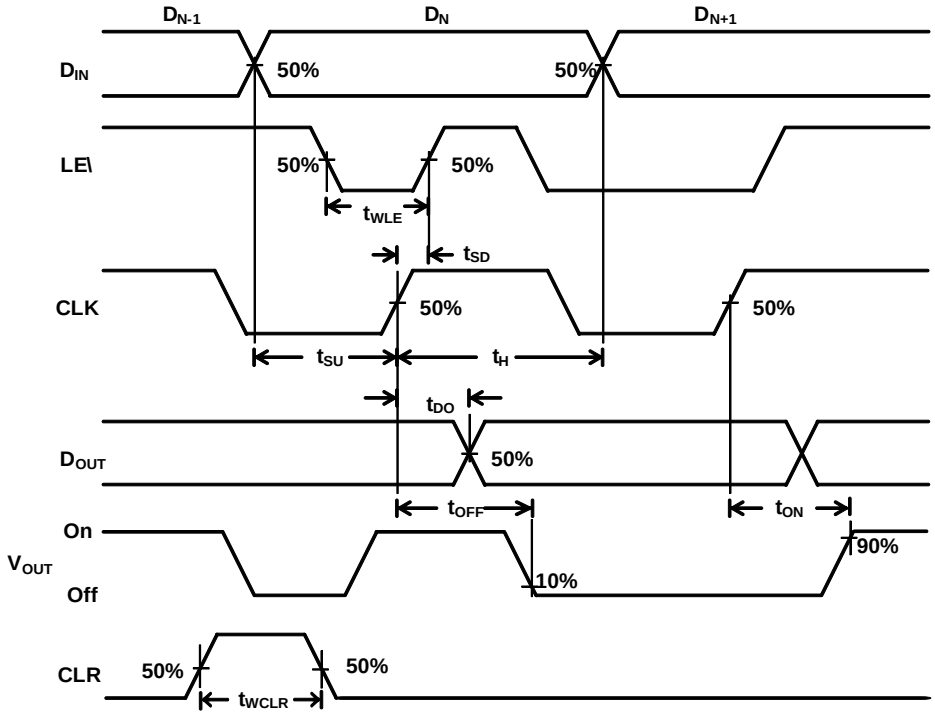


Figure 1: Timing Diagram

LOGIC TRUTH TABLE

Logic Input							Switch State				
D0	D1	D2	___	D31	LE Bar	CLR	SW0	SW1	SW2	---	SW31
L	-	-		-	L	L	Off	-	-		-
H	-	-		-	L	L	On	-	-		-
-	L	-		-	L	L	-	Off	-		-
-	H	-		-	L	L	-	On	-		-
-	-	L		-	L	L	-	-	Off		-
-	-	H		-	L	L	-	-	On		-
⋮	⋮	⋮		⋮	⋮	⋮	⋮	⋮	⋮		⋮
-	-	-		L	L	L	-	-	-		Off
-	-	-		H	L	L	-	-	-		On
x	x	x		x	H	L	Hold previous state				
x	x	x		x	x	H	All switches off				

Note:

7) "L" denotes logic low, "H" denotes logic high, and "x" denotes not applicable.

TEST CIRCUITS

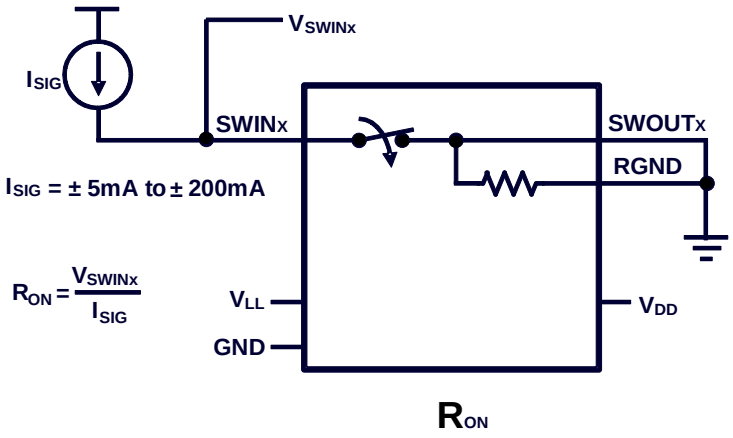


Figure 2: Test Circuit 1

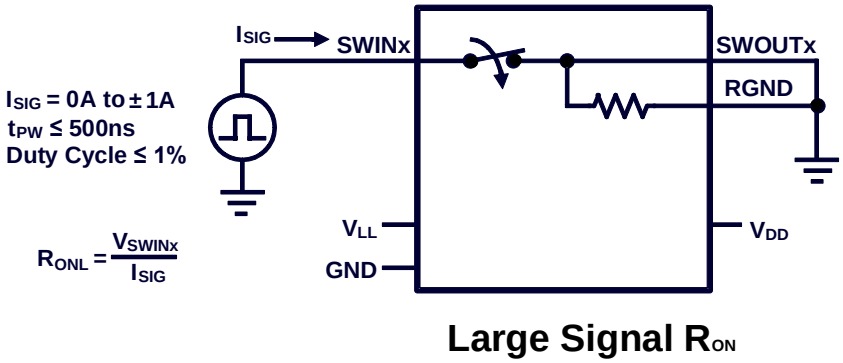


Figure 3: Test Circuit 2

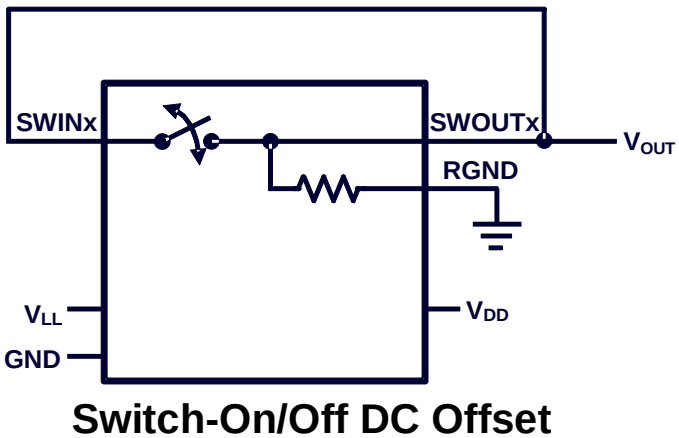


Figure 4: Test Circuit 3

TEST CIRCUITS *(continued)*

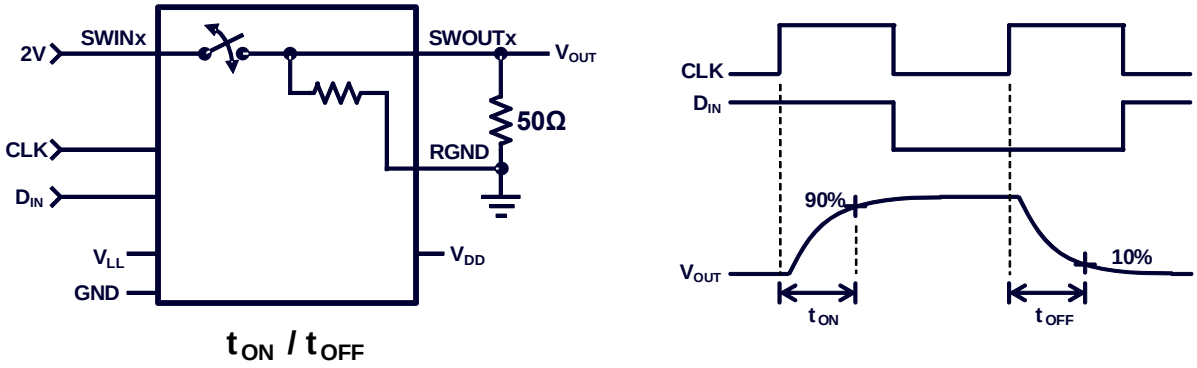
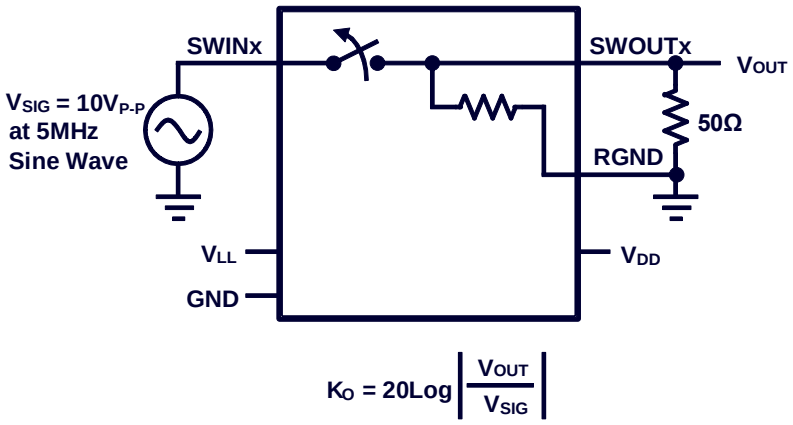
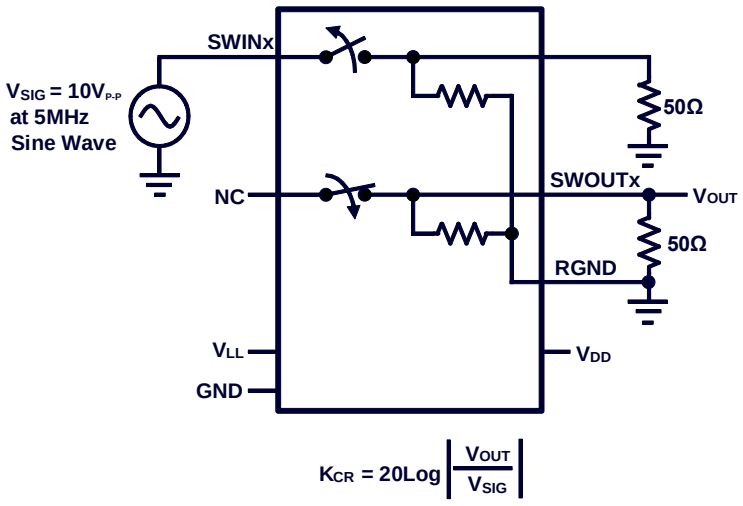


Figure 5: Test Circuit 4



Switch-Off Isolation

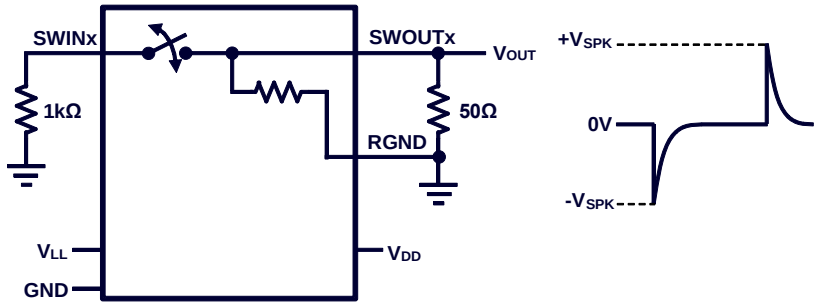
Figure 6: Test Circuit 5



Switch Crosstalk

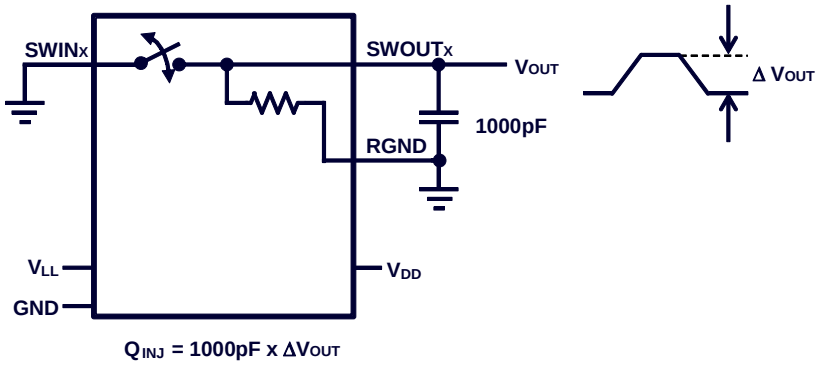
Figure 7: Test Circuit 6

TEST CIRCUITS *(continued)*



Output Voltage Spike

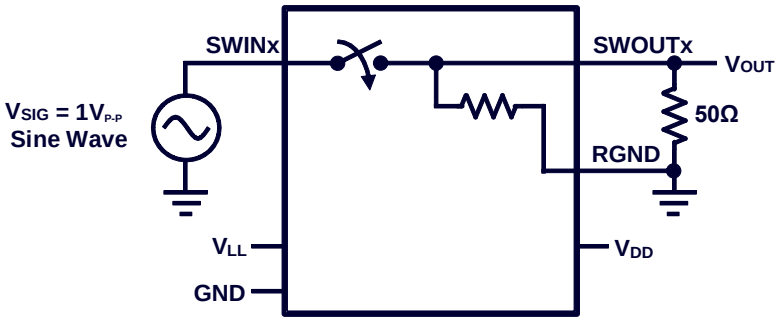
Figure 8: Test Circuit 7



$Q_{INJ} = 1000pF \times \Delta V_{OUT}$

Charge Injection

Figure 9: Test Circuit 8



Small Signal Bandwidth

Figure 10: Test Circuit 9

FUNCTIONAL BLOCK DIAGRAM

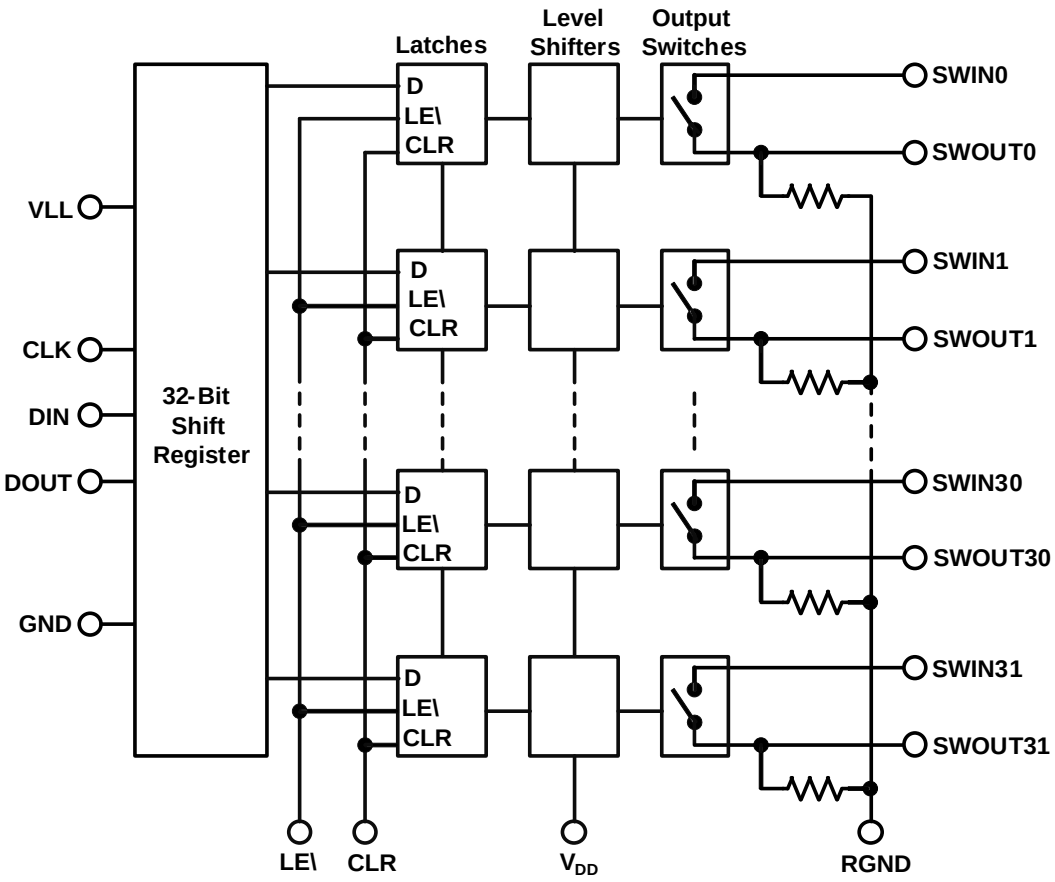


Figure 11: Functional Block Diagram

OPERATION

The MP4833A is a 32-channel, high-voltage, single-pole single-throw (SPST) analog switch with integrated output bleed resistors. It is designed for medical ultrasound imaging and non-destructive testing (NDT) applications. The MP4833A is designed to multiplex high transmission voltages to the selected piezoelectric (PZT) transducers, and to multiplex small analog echo signals to the selected receivers.

The output switches are controlled by a 32-bit serial shift register, followed by a 32-bit data latch. A data out (DOUT) pin allows for multiple devices to be cascaded together. This helps minimize the number of input/output (I/O) control lines. A logic high signal in the data latch turns on the corresponding analog switch; a logic low signal turns off the corresponding analog switch.

The MP4833A has a unique, patented design that does not require any high-voltage negative or positive supplies. As a result, the MP4833A eliminates:

- The need to generate high-voltage positive and negative supplies
- The need for high-voltage bypass capacitors next to each device
- Safety concerns on high-voltage buses
- Concerns for start-up and/or shutdown fault conditions

Analog Switch

Analog switches have a typical on resistance (R_{ON}) of 12.5Ω. When turned on, the MP4833A can pass transmission voltages up to ±90V with peak currents of up to ±2A. When turned off, the device can block voltages up to ±90V.

Each switch has a dedicated input and output pin (SWINx and SWOUTx). The transmission voltages must be connected to the SWINx pins, and the PZT load to the SWOUTx pins. The SWINx and SWOUTx pins are not interchangeable.

Short bursts of high-voltage pulses make up typical high-voltage transmission waves. The burst can consist of a single cycle or multiple cycles of 1MHz to 15MHz pulses, starting and ending at 0V (see Figure 12).

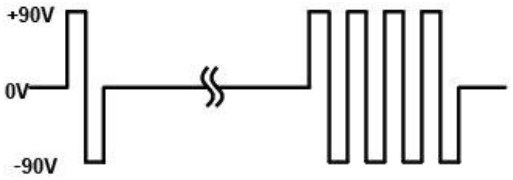


Figure 12: Typical High-Voltage Burst

The SWINx input must be close to ground before sending the high-voltage pulses. This allows the internal circuitry to properly drive the output switches.

Transmission voltages above ±5V require frequencies above 500kHz. There is no restriction when receiving echo signals in which the voltages are below ±0.5V. The switch can pass low-voltage DC signals.

Logic Interface

The MP4833A is controlled by a 32-bit serial shift register, followed by a 32-bit latch. Data is loaded to the shift register during the rising edge of the clock. No data is transferred during the falling edge. Data is shifted in to register 0, then data is shifted out from register 31.

Figure 13 shows the logic interface details. During the first clock cycle, the first data bit enters shift register 0. After 31 more clocked cycles, the first bit is in register 31.

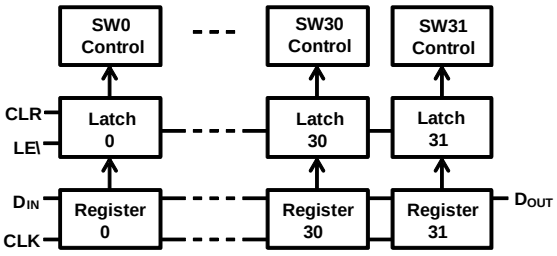


Figure 13: Logic Interface Details

When the latch enable bar (LE\) is low, the data in the shift registers is transferred to the 32-bit latch. When LE\ is high, the data in the latches is held. With high LE\, new data can be shifted to the 32-bit serial shift register without affecting the data in the 32-bit latch. The output switch states follow the data in the 32-bit latch. The CLR pin only clears the data in the 32-bit latch, without affecting the data in the 32-bit serial shift register.

APPLICATION INFORMATION

The MP4833A's maximum clock frequency is 80MHz. The front-end logic control is designed to minimize the number of I/O control lines. For example, a system with 192 channels would require six devices. Figure 14 shows six MP4833A devices in a single daisy chain configuration. With an 80MHz clock, all 192 channels can be updated in 2.4µs. Only four control lines are required: clock, data in, latch enable bar, and clear.

For systems requiring a faster update, multiple data input lines can be used (see Figure 15). Figure 15 shows a 192-channel system incorporating three data input lines: D_{INA}, D_{INB}, and D_{INC}. Each MP4833A device has its own data input line daisy-chained together with six control lines. With an 80MHz clock, all 192 channels can be updated in 800ns.

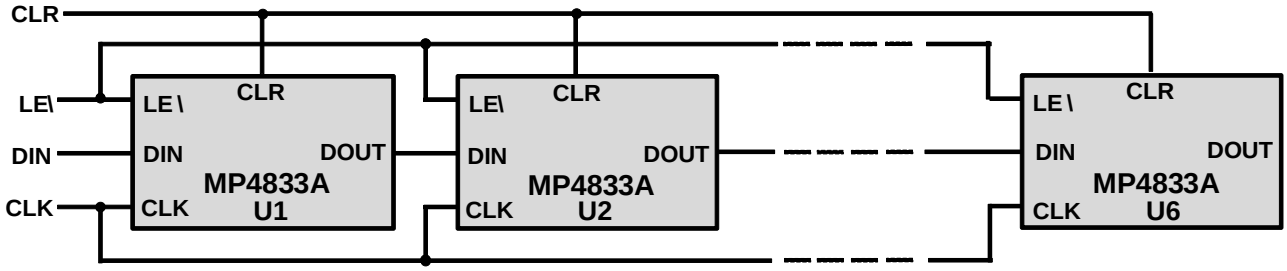


Figure 14: Daisy-Chaining Six MP4833A Devices with a Single Data Input Line

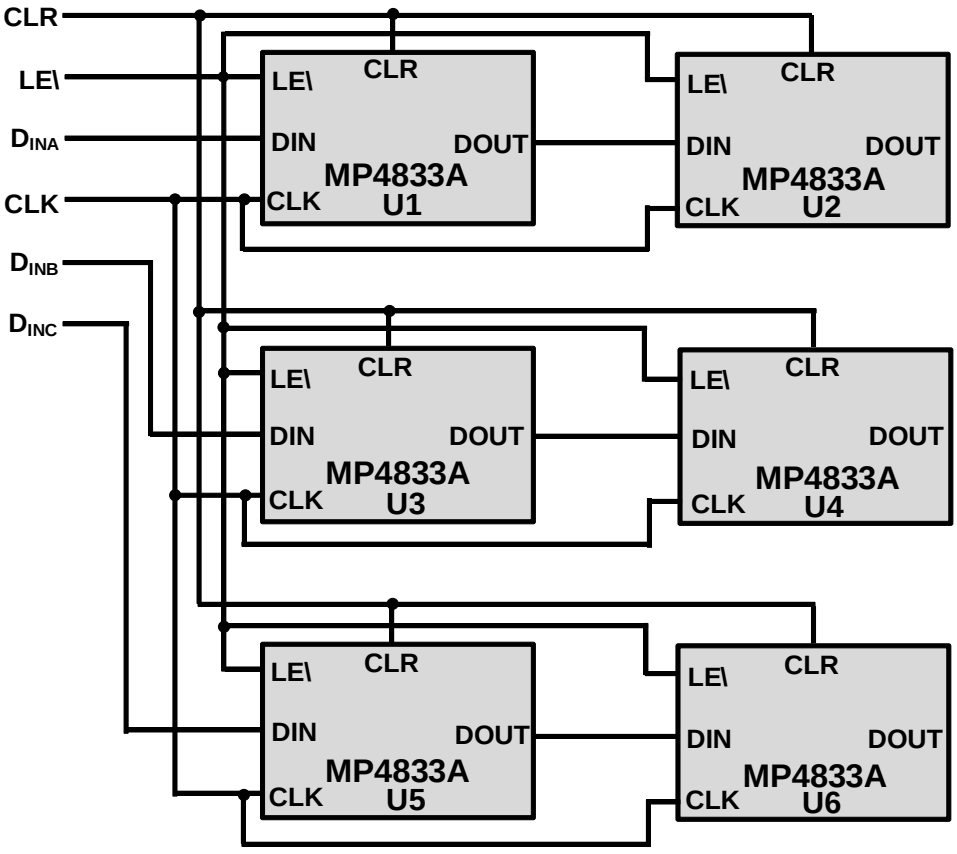


Figure 15: Daisy-Chaining Six MP4833A Devices with Multiple Data Input Lines

Figure 16 shows where the MP4833A analog switches reside in an ultrasound system. A 1:3 multiplexing configuration is shown as an example. Multiplexing configurations can range from 1:2 to 1:8 or higher. 1:8 or higher ratios have slower image frame rates and/or lower quality images, which are generally used in the lower-end, lower-cost ultrasound market. The MP4833A can be used in any ratio.

The main advantage of using the MP4833A is to simplify the transmitter and receiver circuitry. Without any analog switches, the ultrasound console requires 192 transmitters and receivers to drive an ultrasound probe with 192 PZT elements. With analog switches, only 64 transmitters and receivers are required. This reduction saves board space, power, and cost, since the transmitter and receiver circuitry can be quite complex. These benefits are especially important for portable ultrasound systems in which space, battery life, and weight are all at a premium.

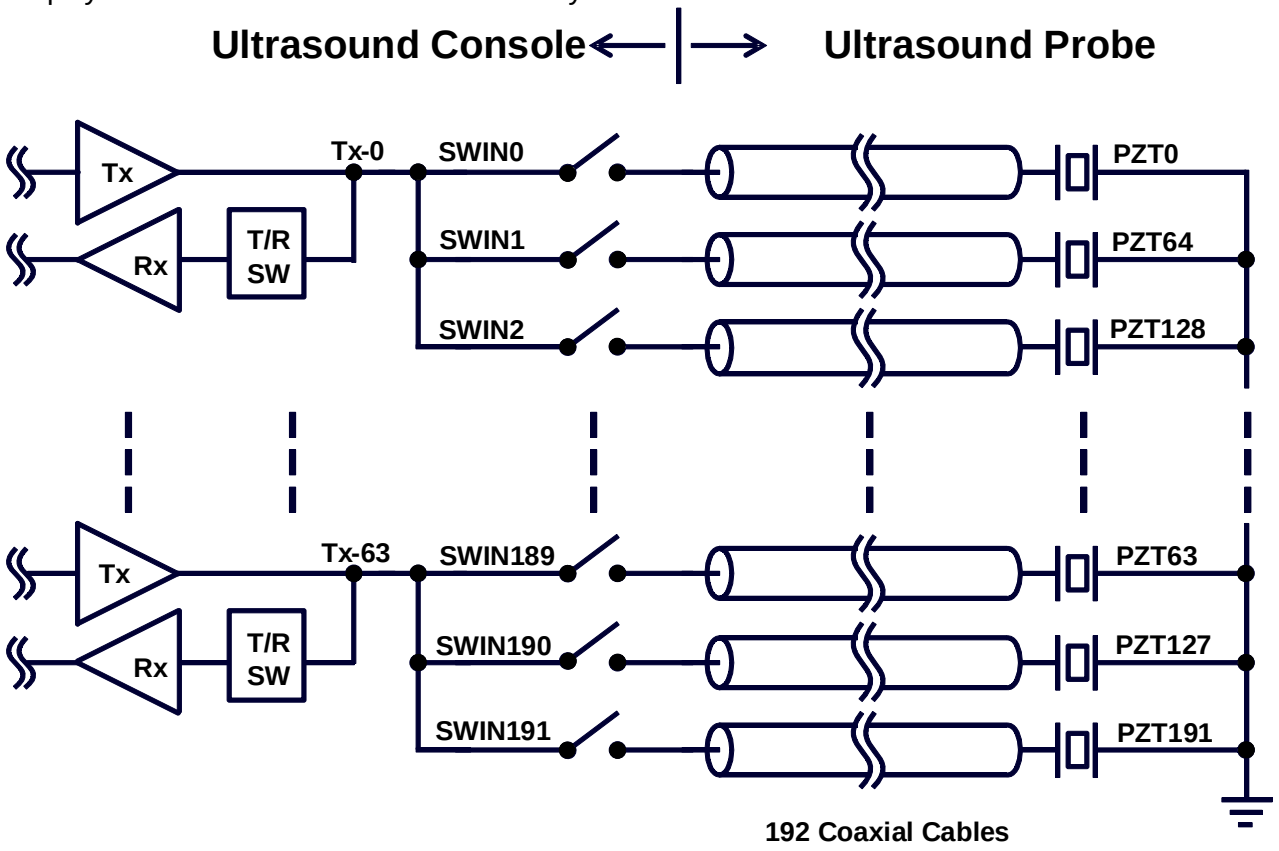


Figure 16: The MP4833A in an Ultrasound Console

Figure 17 shows the advantages of placing analog switches inside the probe head, which is called an active probe. Typically, the probe head is severely space-limited and thermally limited. The housing is waterproof since it must be submersed in alcohol for sterilization. By employing analog switches inside the probe head, the number of coaxial cables can be reduced. Instead of 192 coaxial cables, only 64 coaxial cables are required for the PZT elements, plus 10 or fewer additional coaxial cables for the supply lines and logic interface.

The reduced number of coaxial cables provides significant cost savings for the probe head, as the coaxial cable is by far the most expensive item. Aside from the material cost, the labor to connect the coaxial cables is also typically quite costly. An added user benefit is the increased maneuverability of the probe head. The sonographer undergoes less fatigue using an active probe. Because it does not require high-voltage supplies, the MP4833A eliminates safety concerns about running high-voltage DC lines on the coaxial cables. The minimal power dissipation design also minimizes thermal constraints inside the probe head, and the higher clock speed helps reduce the number of data lines.

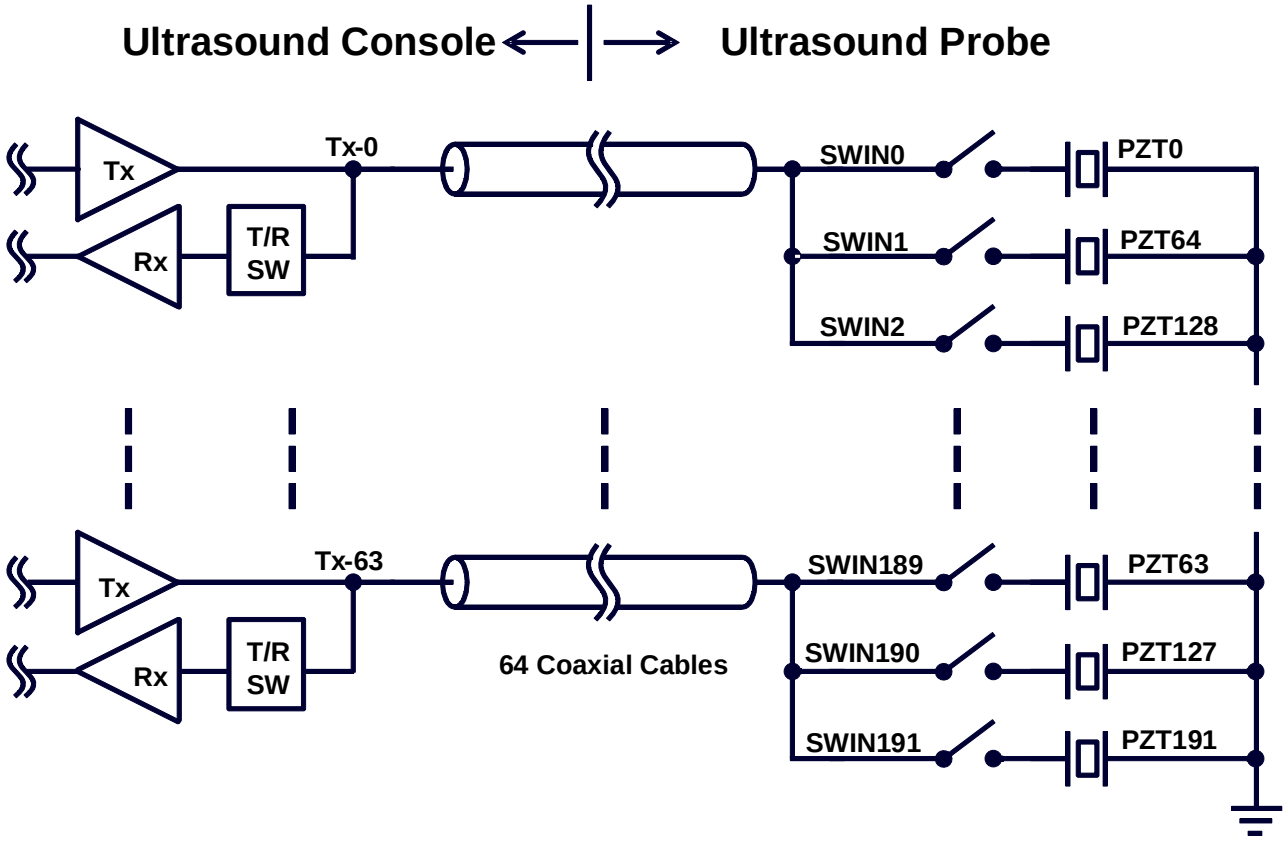


Figure 17: The MP4833A inside the Ultrasound Probe Head

TYPICAL APPLICATION CIRCUIT

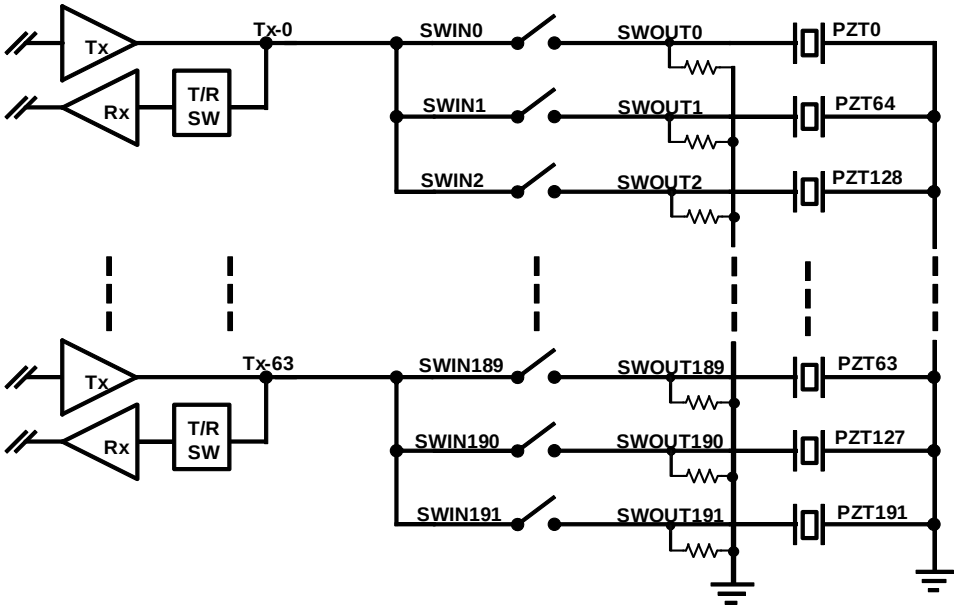
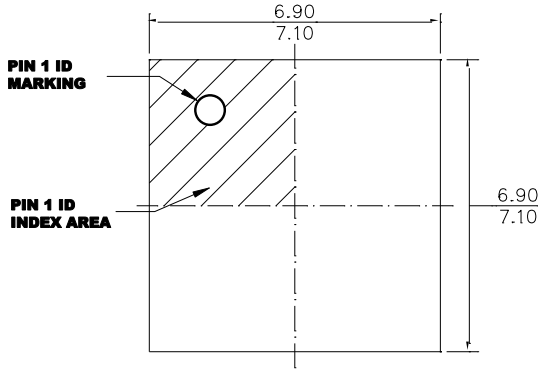


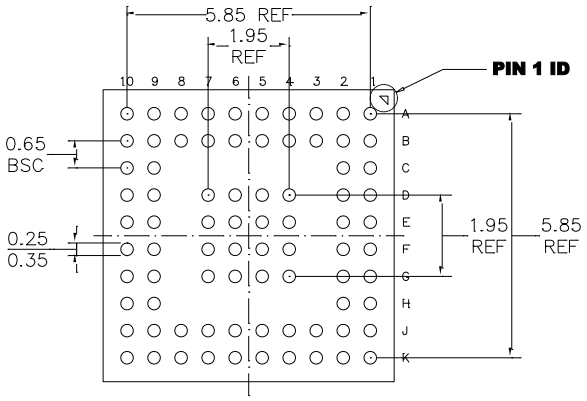
Figure 18: Typical Application Circuit

PACKAGE INFORMATION

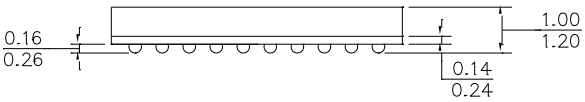
BGA-80 (7mmx7mm)



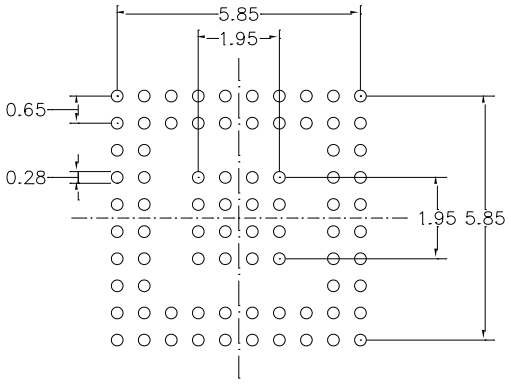
TOP VIEW



BOTTOM VIEW



SIDE VIEW

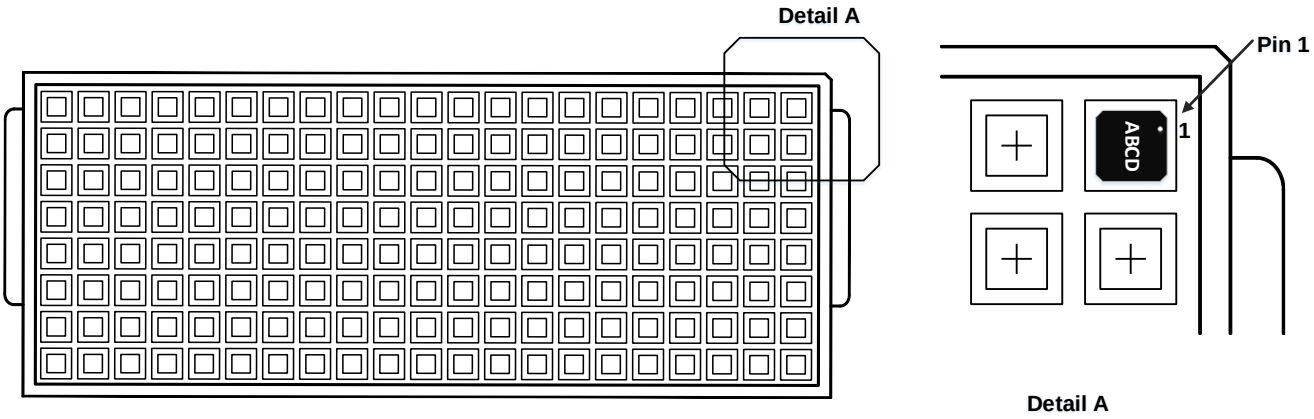


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4833AGBN-T	BGA-80 (7mmx7mm)	N/A	N/A	260	N/A	N/A	N/A

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/16/2021	Initial Release	-