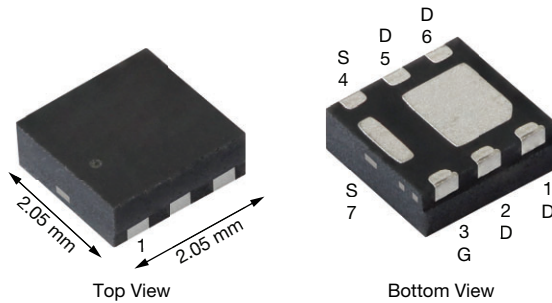


Automotive N-Channel 100 V (D-S) 175 °C MOSFET

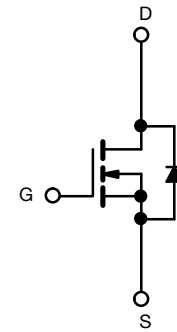
PowerPAK® SC-70W-6L Single

Marking Code: Q2XXXX
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

| PRODUCT SUMMARY | |
|--|--------|
| V _{DS} (V) | 100 |
| R _{DS(on)} (Ω) at V _{GS} = 4.5 V | 0.099 |
| R _{DS(on)} (Ω) at V _{GS} = 10 V | 0.079 |
| I _D (A) | 9 |
| Configuration | Single |



N-Channel MOSFET

| ORDERING INFORMATION | |
|---------------------------------|--|
| Package | PowerPAK SC-70W-6L |
| Lead (Pb)-free and halogen-free | SQA700CEJW (for detailed order number please see www.vishay.com/doc?79776) |

| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-------------------------------------|-----------------------------------|-------------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | | V _{DS} | 100 | V |
| Gate-source voltage | | V _{GS} | ± 20 | |
| Continuous drain current | T _C = 25 °C ^a | I _D | 9 | A |
| | T _C = 125 °C | | 5.2 | |
| Continuous source current (diode conduction) ^a | | I _S | 9 | |
| Pulsed drain current ^a | | I _{DM} | 24 | |
| Single pulse avalanche current | L = 0.1 mH | I _{AS} | 7.3 | |
| Single pulse avalanche energy | | E _{AS} | 2.66 | mJ |
| Maximum power dissipation | T _C = 25 °C | P _D | 13.6 | W |
| | T _C = 125 °C | | 4.5 | |
| Operating junction and storage temperature range | | T _J , T _{stg} | -55 to +175 | °C |
| Soldering recommendations (peak temperature) ^{d, e} | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------|------------------------|-------------------|-------|------|
| PARAMETER | | SYMBOL | LIMIT | UNIT |
| Junction-to-ambient | PCB mount ^c | R _{thJA} | 90 | °C/W |
| Junction-to-case (drain) | | R _{thJC} | 11 | |

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70W-6L is a leadless package and features wettable terminals. The end of the lead terminal is plated with tin
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------|--|--|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 100 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 1.5 | 2.0 | 2.5 | |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 100\text{ V}$ | - | - | 1 | μA |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 100\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | - | - | 50 | |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 100\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | - | - | 250 | |
| On-state drain current ^a | $I_{D(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | 10 | - | - | A |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 3\text{ A}$ | - | 0.056 | 0.079 | Ω |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 3\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | - | - | 0.077 | |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 3\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | - | - | 0.090 | |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 3\text{ A}$ | - | 0.070 | 0.099 | |
| Forward transconductance ^b | g_{fs} | $V_{DS} = 15\text{ V}, I_D = 3\text{ A}$ | | - | 9.0 | - | S |
| Dynamic ^b | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | - | 271 | 380 | pF |
| Output capacitance | C_{oss} | | | - | 140 | 200 | |
| Reverse transfer capacitance | C_{rss} | | | - | 12 | 17 | |
| Total gate charge ^c | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 50\text{ V}, I_D = 2\text{ A}$ | - | 6.2 | 9.5 | nC |
| Gate-source charge ^c | Q_{gs} | | | - | 1.2 | - | |
| Gate-drain charge ^c | Q_{gd} | | | - | 1.3 | - | |
| Gate resistance | R_g | $f = 1\text{ MHz}$ | | 0.5 | 1.1 | 1.6 | Ω |
| Turn-on delay time ^c | $t_{d(on)}$ | $V_{DD} = 50\text{ V}, R_L = 25\text{ }\Omega$ $I_D \cong 2\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$ | | - | 6.0 | 10 | ns |
| Rise time ^c | t_r | | | - | 4 | 7 | |
| Turn-off delay time ^c | $t_{d(off)}$ | | | - | 14 | 22 | |
| Fall time ^c | t_f | | | - | 5 | 8 | |
| Source-Drain Diode Ratings and Characteristics ^b | | | | | | | |
| Pulsed current ^a | I_{SM} | | | - | - | 24 | A |
| Forward voltage | V_{SD} | $I_F = 4.5\text{ A}, V_{GS} = 0\text{ V}$ | | - | 0.86 | 1.2 | V |
| Body diode reverse recovery time | t_{rr} | $I_F = 2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ | | - | 24 | 48 | ns |
| Body diode reverse recovery charge | Q_{rr} | | | - | 20 | 40 | nC |
| Reverse recovery fall time | t_a | | | - | 15 | - | ns |
| Reverse recovery rise time | t_b | | | - | 9 | - | |
| Body diode peak reverse recovery current | $I_{RM(REC)}$ | | | - | -1.5 | - | A |

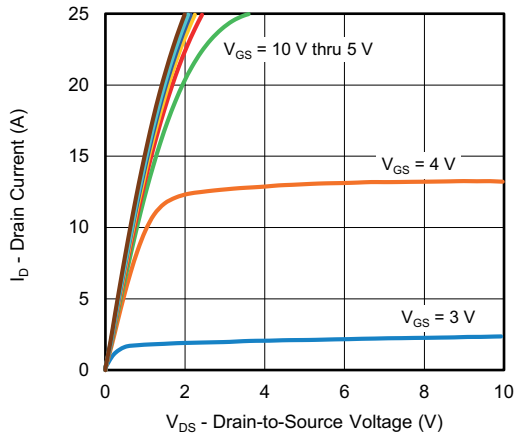
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

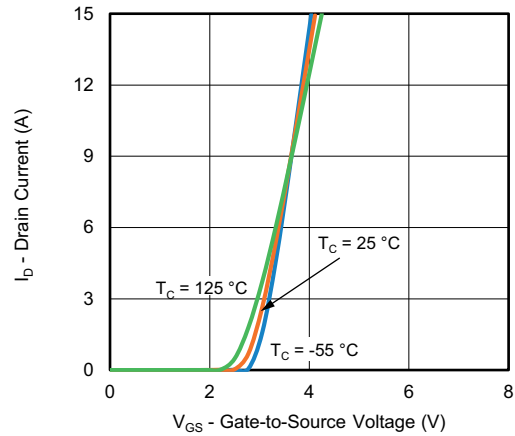
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



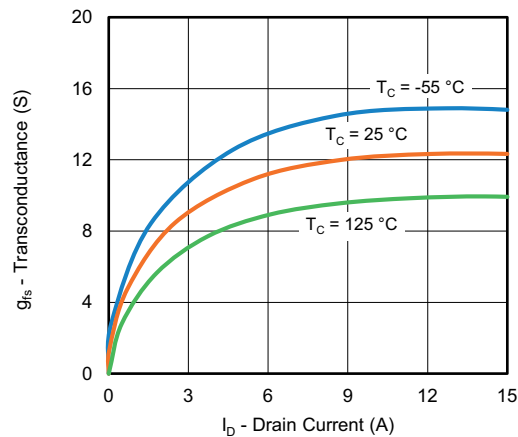
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



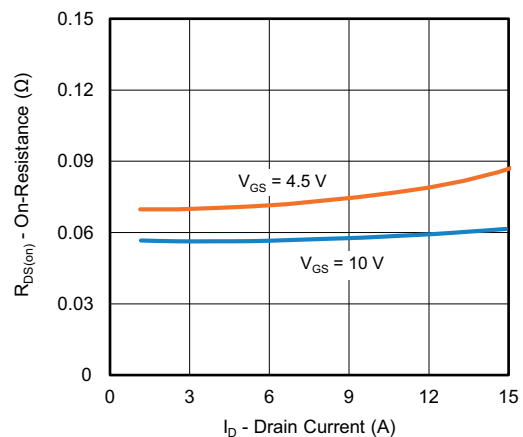
Output Characteristics



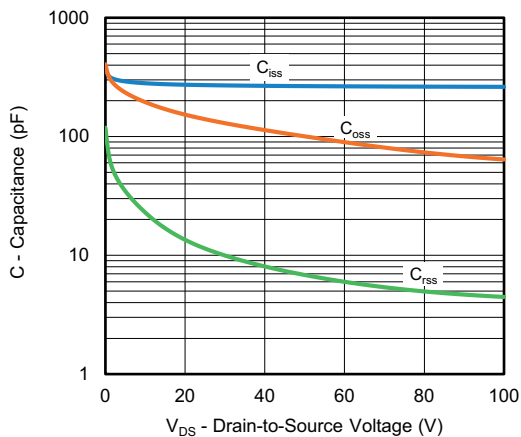
Transfer Characteristics



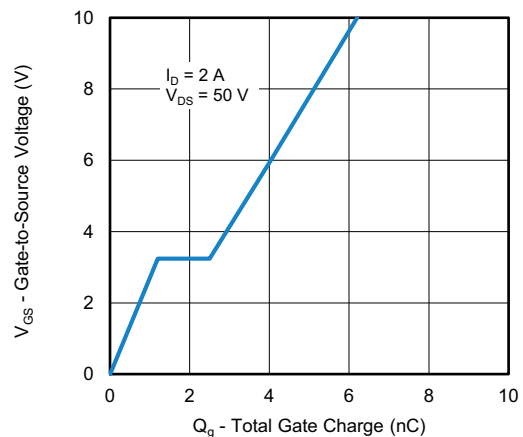
Transconductance



On-Resistance vs. Drain Current



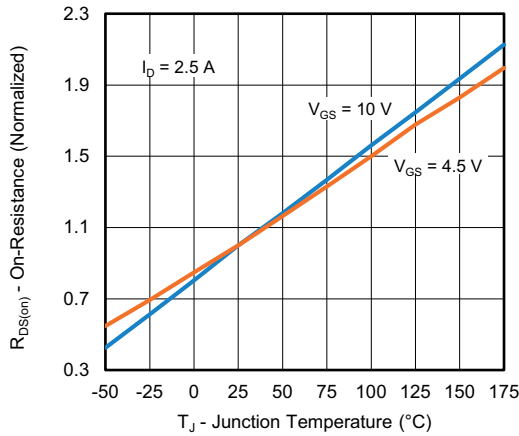
Capacitance



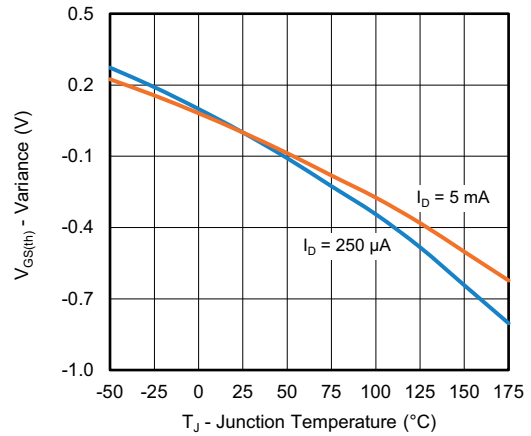
Gate Charge



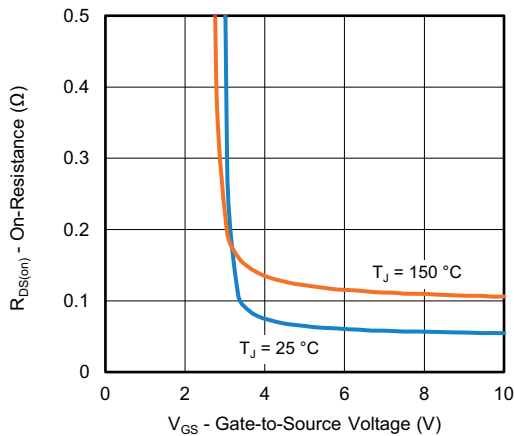
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



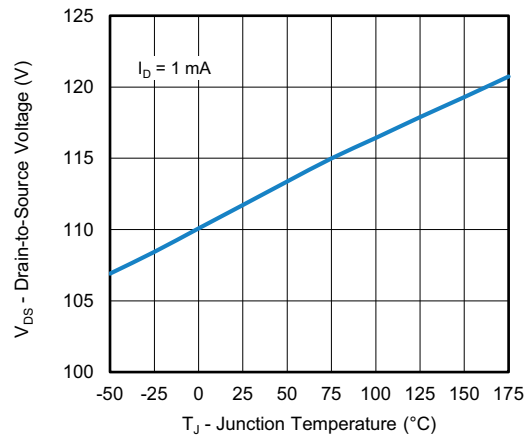
On-Resistance vs. Junction Temperature



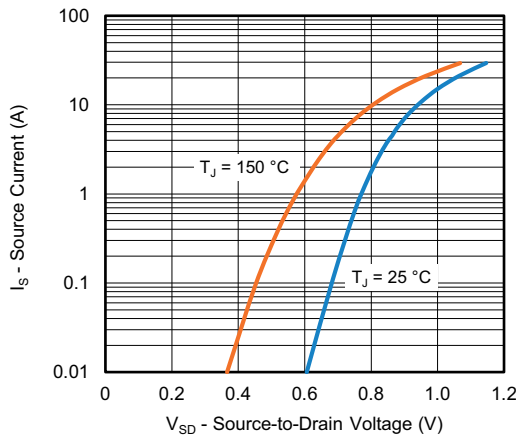
Threshold Voltage



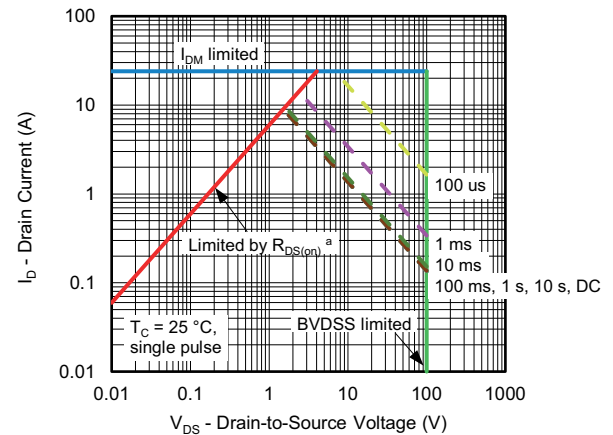
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



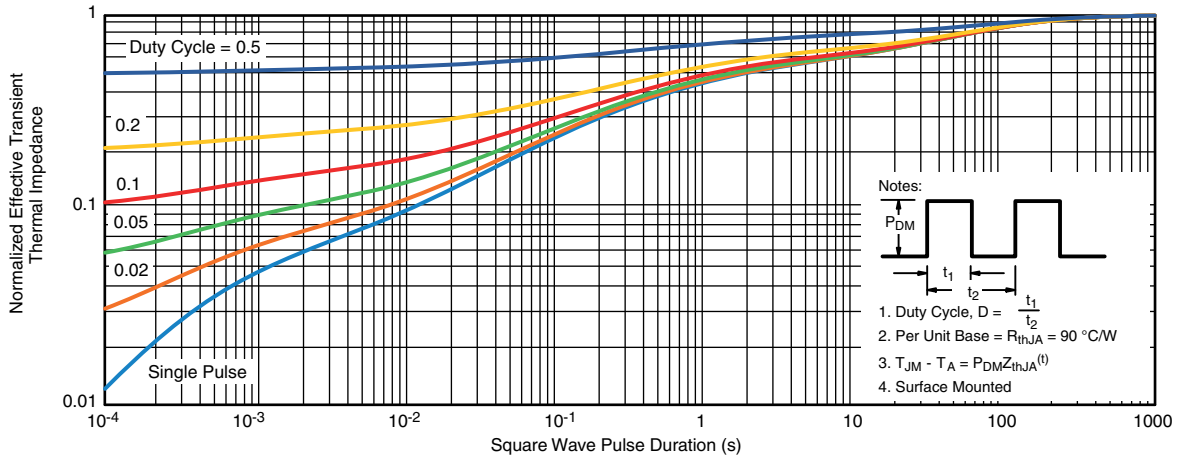
Source Drain Diode Forward Voltage



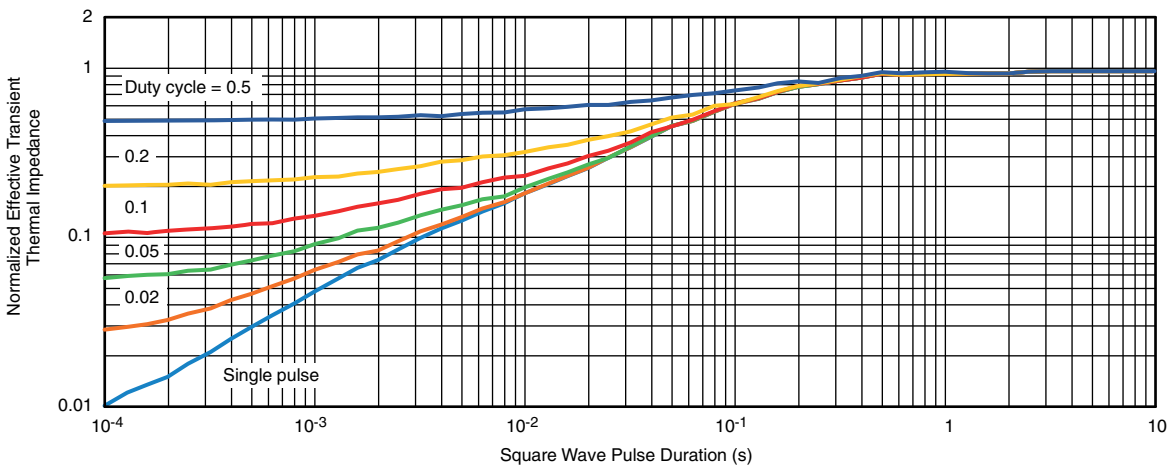
Safe Operating Area



THERMAL RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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