Product Change Notification - SYST-08UUHO160

Date:

10 Oct 2019

Product Category:

16-Bit - Microcontrollers and Digital Signal Controllers

Affected CPNs:

Notification subject:

ERRATA - dsPIC33CH128MP508 Family Silicon Errata and Datasheet Clarification

Notification text:

SYST-08UUHO160

Microchip has released a new Product Documents for the dsPIC33CH128MP508 Family Silicon Errata and Datasheet Clarification of devices. If you are using one of these devices please read the document located at dsPIC33CH128MP508 Family Silicon Errata and Datasheet Clarification.

Notification Status: Final

Description of Change:

1) Adds silicon issue 27 (CPU), 28 (CPU), 29 (DMA) and 30 (PWM).
2) Updates silicon issue 26 (I/O).
3) Updates device data sheet reference to the current revision D.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 10 Oct 2019

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

dsPIC33CH128MP508 Family Silicon Errata and Datasheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

DSPIC33CH128MP202-E/2N
DSPIC33CH128MP202-E/SS
DSPIC33CH128MP202-H/2N
DSPIC33CH128MP202-H/SS
DSPIC33CH128MP202-I/2N
DSPIC33CH128MP202-I/SS
DSPIC33CH128MP202T-I/2N
DSPIC33CH128MP202T-I/SS
DSPIC33CH128MP203-E/M5
DSPIC33CH128MP203-H/M5
DSPIC33CH128MP203-I/M5
DSPIC33CH128MP203T-I/M5
DSPIC33CH128MP205-E/M4
DSPIC33CH128MP205-E/PT
DSPIC33CH128MP205-H/M4
DSPIC33CH128MP205-H/PT
DSPIC33CH128MP205-I/M4
DSPIC33CH128MP205-I/PT
DSPIC33CH128MP205T-I/M4
DSPIC33CH128MP205T-I/PT
DSPIC33CH128MP206-E/MR
DSPIC33CH128MP206-E/PT
DSPIC33CH128MP206-H/MR
DSPIC33CH128MP206-H/PT
DSPIC33CH128MP206-I/MR
DSPIC33CH128MP206-I/PT
DSPIC33CH128MP206T-I/MR
DSPIC33CH128MP206T-I/PT
DSPIC33CH128MP208-E/PT
DSPIC33CH128MP208-H/PT
DSPIC33CH128MP208-I/PT
DSPIC33CH128MP208T-I/PT
DSPIC33CH128MP502-E/2N
DSPIC33CH128MP502-E/SS
DSPIC33CH128MP502-H/2N
DSPIC33CH128MP502-H/SS
DSPIC33CH128MP502-I/2N
DSPIC33CH128MP502-I/SS
DSPIC33CH128MP502T-I/2N
DSPIC33CH128MP502T-I/SS
DSPIC33CH128MP503-E/M5
DSPIC33CH128MP503-H/M5
DSPIC33CH128MP503-I/M5
DSPIC33CH128MP503T-I/M5
DSPIC33CH128MP505-E/M4
DSPIC33CH128MP505-E/PT

DSPIC33CH128MP505-H/M4
DSPIC33CH128MP505-H/PT
DSPIC33CH128MP505-I/M4
DSPIC33CH128MP505-I/PT
DSPIC33CH128MP505T-I/M4
DSPIC33CH128MP505T-I/PT
DSPIC33CH128MP506-E/MR
DSPIC33CH128MP506-E/MRVAO
DSPIC33CH128MP506-E/PT
DSPIC33CH128MP506-H/MR
DSPIC33CH128MP506-H/PT
DSPIC33CH128MP506-I/MR
DSPIC33CH128MP506-I/PT
DSPIC33CH128MP506T-E/MRVAO
DSPIC33CH128MP506T-I/MR
DSPIC33CH128MP506T-I/PT
DSPIC33CH128MP508-E/PT
DSPIC33CH128MP508-E/PTVAO
DSPIC33CH128MP508-H/PT
DSPIC33CH128MP508-I/PT
DSPIC33CH128MP508T-I/PT
DSPIC33CH64MP202-E/2N
DSPIC33CH64MP202-E/SS
DSPIC33CH64MP202-H/2N
DSPIC33CH64MP202-H/SS
DSPIC33CH64MP202-I/2N
DSPIC33CH64MP202-I/SS
DSPIC33CH64MP202T-I/2N
DSPIC33CH64MP202T-I/SS
DSPIC33CH64MP203-E/M5
DSPIC33CH64MP203-H/M5
DSPIC33CH64MP203-I/M5
DSPIC33CH64MP203T-I/M5
DSPIC33CH64MP205-E/M4
DSPIC33CH64MP205-E/PT
DSPIC33CH64MP205-H/M4
DSPIC33CH64MP205-H/PT
DSPIC33CH64MP205-I/M4
DSPIC33CH64MP205-I/PT
DSPIC33CH64MP205T-I/M4
DSPIC33CH64MP205T-I/PT
DSPIC33CH64MP206-E/MR
DSPIC33CH64MP206-E/PT
DSPIC33CH64MP206-H/MR
DSPIC33CH64MP206-H/PT
DSPIC33CH64MP206-I/MR
DSPIC33CH64MP206-I/PT
DSPIC33CH64MP206T-I/MR
DSPIC33CH64MP206T-I/PT

DSPIC33CH64MP208-E/PT
DSPIC33CH64MP208-H/PT
DSPIC33CH64MP208-I/PT
DSPIC33CH64MP208T-I/PT
DSPIC33CH64MP502-E/2N
DSPIC33CH64MP502-E/SS
DSPIC33CH64MP502-H/2N
DSPIC33CH64MP502-H/SS
DSPIC33CH64MP502-I/2N
DSPIC33CH64MP502-I/SS
DSPIC33CH64MP502T-I/2N
DSPIC33CH64MP502T-I/SS
DSPIC33CH64MP503-E/M5
DSPIC33CH64MP503-H/M5
DSPIC33CH64MP503-I/M5
DSPIC33CH64MP503T-I/M5
DSPIC33CH64MP505-E/M4
DSPIC33CH64MP505-E/PT
DSPIC33CH64MP505-H/M4
DSPIC33CH64MP505-H/PT
DSPIC33CH64MP505-I/M4
DSPIC33CH64MP505-I/PT
DSPIC33CH64MP505T-I/M4
DSPIC33CH64MP505T-I/PT
DSPIC33CH64MP506-E/MR
DSPIC33CH64MP506-E/PT
DSPIC33CH64MP506-H/MR
DSPIC33CH64MP506-H/PT
DSPIC33CH64MP506-I/MR
DSPIC33CH64MP506-I/PT
DSPIC33CH64MP506T-I/MR
DSPIC33CH64MP506T-I/PT
DSPIC33CH64MP508-E/PT
DSPIC33CH64MP508-H/PT
DSPIC33CH64MP508-I/PT
DSPIC33CH64MP508T-I/PT

dsPIC33CH128MP508

dsPIC33CH128MP508 Family
Silicon Errata and Data Sheet Clarification

The dsPIC33CH128MP508 family devices that you have received conform functionally to the current Device Data Sheet (DS70005319**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33CH128MP508 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 11, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various dsPIC33CH128MP508 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision
		A2
Master (With CAN FD)		
dsPIC33CH64MP502	0x8740	0x0002
dsPIC33CH128MP502	0x8750	
dsPIC33CH64MP503	0x8741	
dsPIC33CH128MP503	0x8751	
dsPIC33CH64MP505	0x8742	
dsPIC33CH128MP505	0x8752	
dsPIC33CH64MP506	0x8743	
dsPIC33CH128MP506	0x8753	
dsPIC33CH64MP508	0x8744	
dsPIC33CH128MP508	0x8754	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID(1)	Revision ID for Silicon Revision
		A2
Slave (With CAN FD)		
dsPIC33CH64MP502S1	0x87C0	0x0002
dsPIC33CH128MP502S1	0x87D0	
dsPIC33CH64MP503S1	0x87C1	
dsPIC33CH128MP503S1	0x87D1	
dsPIC33CH64MP505S1	0x87C2	
dsPIC33CH128MP505S1	0x87D2	
dsPIC33CH64MP506S1	0x87C3	
dsPIC33CH128MP506S1	0x87D3	
dsPIC33CH64MP508S1	0x87C4	
dsPIC33CH128MP508S1	0x87D4	
Master (Without CAN FD)		
dsPIC33CH64MP202	0x8700	0x0002
dsPIC33CH128MP202	0x8710	
dsPIC33CH64MP203	0x8701	
dsPIC33CH128MP203	0x8711	
dsPIC33CH64MP205	0x8702	
dsPIC33CH128MP205	0x8712	
dsPIC33CH64MP206	0x8703	
dsPIC33CH128MP206	0x8713	
dsPIC33CH64MP208	0x8704	
dsPIC33CH128MP208	0x8714	
Slave (Without CAN FD)		
dsPIC33CH64MP202S1	0x8780	0x0002
dsPIC33CH128MP202S1	0x8790	
dsPIC33CH64MP203S1	0x8781	
dsPIC33CH128MP203S1	0x8791	
dsPIC33CH64MP205S1	0x8782	
dsPIC33CH128MP205S1	0x8792	
dsPIC33CH64MP206S1	0x8783	
dsPIC33CH128MP206S1	0x8793	
dsPIC33CH64MP208S1	0x8784	
dsPIC33CH128MP208S1	0x8794	

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A2
ECC	Status	1.	ECCSTATH/L registers cannot be read.	X
ECC	Status	2.	SECSYNDx bits in the ECCSTATH register cannot be read.	X
I^2C	Interrupt	3.	In Slave mode, an incorrect interrupt is generated with DHEN = 1.	X
I^2C	Error	4.	Bus collision error cannot be cleared.	X
I^2C	Error	5.	False bus collision error generated.	X
I^2C	Idle	6.	Address cannot be received in Idle mode.	X
Oscillator	PLL	7.	FRCDIVN drives the PLL instead of the FRC.	X
Oscillator	HS,XT	8.	The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early.	X
PWM	Dead Time	9.	When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.	X
UART	FERR	10.	The OERR bit cannot be cleared by software.	X
UART	OERR	11.	The FERR bit will not get set if one Stop bit is received.	X
UART	TRMT	12.	The 9th byte received will not be available to be read.	X
UART	TRMT	13.	The TRMT bit takes time to set on the last transmit completion.	X
UART	TRMT	14.	The TRMT bit is unreliable when there is back-to-back Break character transmission.	X
UART	Idle	15.	SLPEN = 1 will not keep the UART BRG clock active in Sleep mode.	X
UART	RIDLE	16.	The RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.	X
UART	TXWRE	17.	The TXWRE bit (UxSTAH[7]) cannot be cleared once it gets set.	X
UART	Address Detect	18.	When writing to UxP1 with UTXBRK = 1, the content of P1 will not get transmitted.	X
UART	DMX	19.	In DMX mode with reception enabled, no interrupt is generated on receiving start code or break of data frame.	X
UART	UART	20.	When UART is used in DMX mode (MOD[3:0] (UxMODE[3:0]) = 0b1010) with reception enabled, no interrupt is generated on receiving start code or break of data frame.	X
UART	Smart Card	21.	The Waiting Time Counter Interrupt Flag (WTCIF) is set when the last x character transmitted has the bit, LAST = 0.	X
UART	XOFF	22.	XOFF is transmitted when one empty space remains in the RX buffer.	X
CPU	FLIM Instruction	23.	When the operands are of different signs, the FLIM instruction may not force the correct data limit.	X
SCCP/ MCCP	Clock Source	24.	Using FOSC as the clock source may cause synchronization issues.	X
I^2C	SMBus 3.0	25.	When Configuration bit, SMBEN (FDEVOPT[10]) = 1, the SMBus 3.0 VIH minimum specification may not be met.	X
I/O	POR	26.	Spike on I/O at POR.	X
CPU	MAXAB/MINAB Instructions	27.	When the operands are of different signs, the MAXAB, MINAB and MINZAB instructions may not output the correct value.	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A2
CPU	`div.sd` Instruction	28.	When using the signed 32-by-16-bit division instruction, `div.sd`, the Overflow bit is not getting set when an overflow occurs.	X
DMA	ADC Triggers	29.	DMA is triggered continuously from ADC.	X
PWM	Time Base Capture	30.	PWM Capture Status (CAP) flag will not set again under certain conditions.	X

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: ECC

The ECCSTATH/L registers cannot be read when an ECC error happens. The ECC Double-Bit Error (ECCDBE) trap and ECC Single Bit Error (ECCSBE) interrupt will work correctly, but the ECCSTATH/ECCSTATL registers will always read as zero.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave			

2. Module: ECC

In the ECCSTATH register, the SECSYNDx bits cannot be read when an ECC error happens.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master			
Slave	X		

3. Module: I^2C

In Slave mode with DHEN = 1 (Data Hold Enable), if software sends a NACK, a Slave interrupt is asserted at the 9th falling edge of the clock.

Work around

Software should ignore the Slave interrupt that is asserted after sending a NACK.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

4. Module: I^2C

In Slave mode, the Bus Collision Detect (BCL) bit cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I^2C module and then re-enable the module.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

5. Module: I^2C

In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1) and a Stop bit is received.

Work around

Ignore the bus collision. Disable the I^2C module and then re-enable the module.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

6. Module: I^2C

In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

7. Module: Oscillator

When using the 8 MHz internal FRC Oscillator with Primary PLL as either a system clock or a peripheral source, FRCDIVN drives the PLL instead of the FRC.

This means that the PLL FRC input selection is subject to the FRCDIV[2:0] bits and could lead to a condition where the minimum PLL input requirement of 8 MHz is not maintained.

Work around

Ensure FRCDIV[2:0] bits are maintained as zero when using FRCPLL as either a system clock or a peripheral source.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

8. Module: Oscillator

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Then, switch to the POSC source.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

9. Module: PWM

When feed-forward PCI is used for dead-time compensation (DTCMPSEL = 1), the PWMx outputs are overridden.

Work around

Use Sync PCI (DTCMPSEL = 0) for dead-time compensation.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

10. Module: UART

Once the UART receive buffer overflows and the OERR bit (UxSTA[1]) is set, the OERR bit cannot be cleared by software.

Work around

1. Make sure that the receive buffer never overflows. Do not let the OERR bit get set by reading the received data byte on each byte reception.
2. Disable and enable UART before clearing the OERR bit.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

11. Module: UART

When the UART is operating with STSEL[1:0] = 2 (two Stop bits sent, two checked at receive), the FERR bit will not get set if one Stop bit is received.

Work around

Use STSELx = 3 instead of STSELx = 2. When operating with STSELx = 3 mode, the UART will be configured to send two Stop bits, but check one at receive.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

12. Module: UART

When the receive buffer overflows, the 9th byte received will get lost and cannot be read.

Work around

Do not allow the OERR bit to get set by reading the received data byte on each byte reception.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

13. Module: UART

At low BRG value, the TRMT bit takes time to set on the last transmit completion, which may result in the transmitted data getting lost.

Work around

1. Use the UTXBE bit to monitor for the next transmit
2. Provide a delay to stabilize the POSC.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

14. Module: UART

The Transmit Shifter Empty (TRMT) bit is unreliable when there is back-to-back Break character transmission.

Work around

Poll the UART Transmit Break bit, UTXBRK (UxMODE[8]), to be cleared instead of the TRMT bit.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

15. Module: UART

UART will not work correctly in Sleep mode. SLPEN = 1 will not keep the UART baud rate clock active in Sleep mode.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

16. Module: UART

During a UART Auto-Baud Detection sequence, the RIDLE bit takes one instruction cycle to get cleared after ABAUD is set.

Work around

Ignore the RIDLE bit until the Auto-Baud Detection sequence is complete.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

17. Module: UART

Once the TX Write Transmit Error Status bit, TXWRE (UxSTAH[7]), gets set, the TXWRE cannot be cleared by a single clear instruction.

Work around

Use multiple clear instructions of loop until the TXWRE bit gets cleared.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

18. Module: UART

In UART Address Detect mode, writing to UxP1 with UTXBRK = 1 should cause a Break to be transmitted, followed by the content in P1, but the content of P1 will not get transmitted.

Work around

After writing to P1, wait for UTXBRK to get clear and then rewrite to P1.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

19. Module: UART

When UART is in DMX mode, MOD[3:0] (UxMODE[3:0]) = 0b1010 with transmission enabled, any write to the UxP1 register after enabling UART would be ignored.

Work around

Write the value of the UxP1 register before enabling the UART.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

20. Module: UART

When UART is used in DMX mode, MOD[3:0] (UxMODE[3:0]) = 0b1010 with reception enabled, no interrupt is generated on receiving a start code or break of data frame. Depending on the URXISEL[2:0] (UxSTAH[10:8]) bits, an interrupt will be generated on receiving the data bytes.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

21. Module: UART

In Smart Card T = 1 mode, the Wait Time Counter Interrupt Flag (WTCIF) is set when the last character transmitted has the bit, LAST = 0.

Work around

Ignore WTC interrupt events on non-last bytes.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

22. Module: UART

In Software Flow Control mode, XOFF is transmitted when one empty space remains in the RX buffer. XOFF transmission can get further delayed if the transmitter has already been loaded, resulting in XOFF transmission on a receive buffer full event.

Work around 1

Give a minimum one-byte delay before each byte transmission.

Work around 2

Use the UART RX interrupt with URXISEL[2:0] set to at least two empty slots. This allows the RX buffer to be read in time to prevent RX buffer overflow.

Affected Silicon Revisions.

Core	A2		
Master	X		
Slave	X		

23. Module: CPU

The FLIM instruction may incorrectly limit the data range when operating on signed operands of different sign values. If the operands are either all negative or all positive, the limit is correct.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

24. Module: SCCP/MCCP

When FOSC is selected as the clock source using the CLKSEL[2:0] bits (CCPxCON1L[10:8]), unexpected operation may occur. For proper SCCP/MCCP input clock synchronization, do not use FOSC as the system clock source.

Work around

Use any of the other available clock sources in CLKSEL[2:0].

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

25. Module: I^2C

When selecting SMBus 3.0 operation using Configuration bit, SMBEN (FDEVOPT[10]), the Voltage Input High (VIH) of the SMBus 3.0 specification minimum may not be met.

Work around

None.

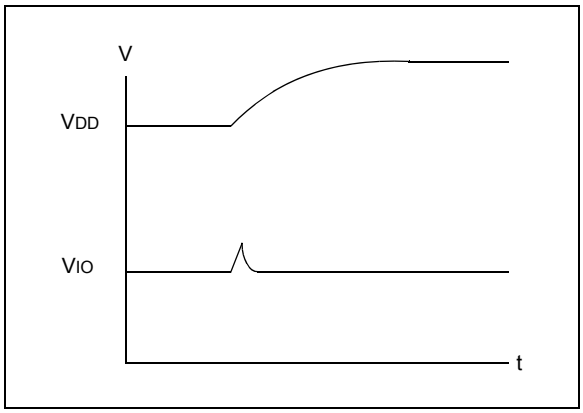
Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

26. Module: I/O

During a fast device power-up, when the VDD ramp is less than 4 mS, the I/O pins may drive up to 100 µA current for a duration of up to 10 µS (Figure 1).

FIGURE 1: I/O RAMP



Work around

1. Slow down the VDD ramp time (greater than 4 mS for VDD to ramp 0V to 3.3V).
2. Ensure the circuitry that is connected to the pins can endure this pulse.

Example applications affected may include complementary power switches, where a transient current shoot-through might occur.

High-voltage applications with complementary switches should power the high-voltage 200 µSec later than powering the dsPIC® device to avoid the current shoot-through. This behavior is specific to each device and not affected by aging.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

27. Module: CPU

When operating on signed operands of different sign values, the output for `MAXAB`, `MINAB` and `MINZAB` instructions may be incorrect. If the operands are either all negative or all positive, the output is correct.

Work around

None.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

28. Module: CPU

When using the Signed 32-by-16-Bit Division instruction, `div.sd`, the Overflow bit may not always get set when an overflow occurs. This erratum only affects operations in which at least one of the following conditions is true:

- Dividend and divisor differ in sign,
- Dividend > 0x3FFFFFFF or
- Dividend < 0xC0000000

Work around

The application software must perform both of the following actions to handle possible undetected overflow conditions:

a) The value of the dividend must always be constrained to be in the following range: 0xC0000000 ≤ Dividend ≤ 0x3FFFFFFF.

b) If the dividend and divisor differ in sign (e.g., dividend is negative and divisor is positive), then after executing the `div.sd` instruction or the compiler built-in function, `__builtin_divsd()`, inspect the sign of the resultant quotient. If the quotient is found to be a positive number, then treat it as an overflow condition.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

29. Module: DMA

The DMA receives multiple continuous triggers from the ADC until the trigger event from ADC is cleared. The OVRUNIF flag (DMAINTn[3]) will be set. When the OVRUNIF bit changes state, from '`0`' to '`1`', a DMA interrupt is generated.

Work around

Ignore the OVRUNIF bit and the first DMA interrupt. Clear the ADC trigger source, ANxRDY, with a DMA read of the ADC buffer, ADCBUFx, for the corresponding ADC channel.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

30. Module: PWM

When using a PWM Control Input (PCI) to trigger a time base capture, the Capture Status flag, CAP (PGxSTAT[5]), may not set again under certain conditions. When a subsequent PWM capture event occurs while, or just after, reading the current capture value from the PGxCAP register, the Capture Status flag, CAP, will not set again.

Work around

Read the PWM Generator Capture (PGxCAP, x = 1 to 8) register at a known time to avoid the condition. The timing of the PGxCAP read operation can be scheduled by using the PWM Generator (1-8) interrupt, or any of the six PWM Event (A-F) interrupts, corresponding to the PCI event which triggered the time base capture. Read the PGxCAP value after the CAP bit has been set within the interrupt.

Affected Silicon Revisions

Core	A2		
Master	X		
Slave	X		

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70005319**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2018)

Initial release of this document; issued for revision A2.

Rev B Document (11/2018)

Adds silicon issue 23 (CPU), 24 (SCCP/MCCP), 25 (I^2C) and 26 (I/O).

Rev C Document (10/2019)

Adds silicon issue 27 (CPU), 28 (CPU), 29 (DMA) and 30 (PWM).

Updates silicon issue 26 (I/O).

Updates device data sheet reference to the current revision D.

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