Chopper-Stabilized Precision Hall-Effect Latches

Features and Benefits

- AEC-Q100 automotive qualified
- Symmetrical latch switchpoints
- Resistant to physical stress
- Superior temperature stability
- Output short-circuit protection
- Operation from unregulated supply down to 3 V
- Reverse-battery protection
- Solid-state reliability
- Small package sizes

Packages:

Not to scale

3-pin SOT23W
(suffix LH)

(A1220
and 1221)

(A1222
and A1223)

3-pin SIP (suffix UA)

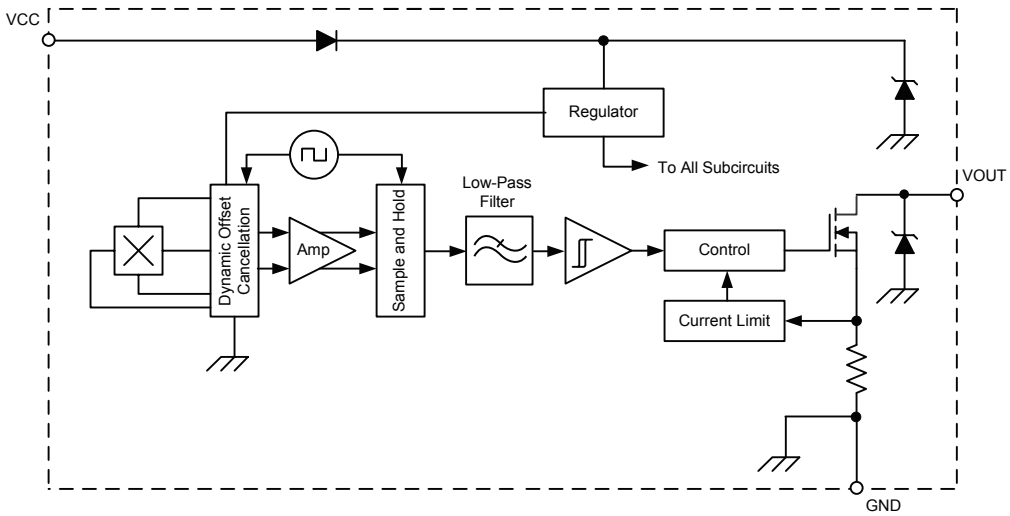
Description

The A1220, A1221, A1222, and A1223 Hall-effect sensor ICs are extremely temperature-stable and stress-resistant devices especially suited for operation over extended temperature ranges to 150°C. Superior high-temperature performance is made possible through dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. Each device includes on a single silicon chip a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit protected open-drain output to sink up to 25 mA. A south pole of sufficient strength turns the output on. A north pole of sufficient strength is necessary to turn the output off.

An onboard regulator permits operation with supply voltages of 3 to 24 V. The advantage of operating down to 3 V is that the device can be used in 3 V applications or with additional external resistance in series with the supply pin for greater protection against high voltage transient events.

Two package styles provide magnetically optimized packages for most applications. Package type LH is a modified 3-pin SOT23W surface-mount package, while UA is a three-pin ultra-mini SIP for through-hole mounting. Both packages are lead (Pb) free, with 100% matte-tin-plated leadframes.

Functional Block Diagram



Selection Guide

Part Number	Packing[1]	Mounting	Ambient, T_A	B_{RP} (Min)	B_{OP} (Max)
A1220ELHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 85ºC	–40	40
A1220ELHLT-T[2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount			
A1220EUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1220LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 150ºC		
A1220LLHLT-T[2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount			
A1220LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1221ELHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 85ºC	–90	90
A1221ELHLT-T[2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount			
A1221EUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1221LLHLX-T	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 150ºC		
A1221LLHLT-T[2]	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount			
A1221LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1222ELHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 85ºC	–150	150
A1222ELHLX-T[2]	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1222EUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1222LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 150ºC		
A1222LLHLX-T[2]	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1222LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1223ELHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 85ºC	–180	180
A1223ELHLX-T[2]	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1223EUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A1223LLHLT-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	–40ºC to 150ºC		
A1223LLHLX-T[2]	13-in. reel, 10000 pieces/reel	3-pin SOT23W surface mount			
A1223LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			

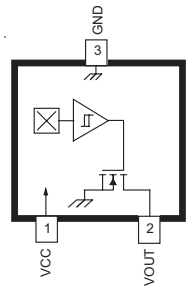
[1]Contact Allegro for additional packing options.
[2]Available through authorized Allegro distributors only.

Absolute Maximum Ratings

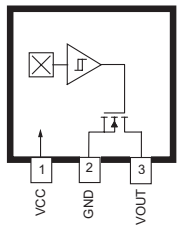
Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		26.5	V
Reverse Supply Voltage	V_{RCC}		–30	V
Output Off Voltage	V_{OUT}		26	V
Continuous Output Current	I_{OUT}		25	mA
Reverse Output Current	I_{ROUT}		–50	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pin-out Diagrams

Package LH



Package UA



Terminal List

Name	Description	Number	
		Package LH	Package UA
VCC	Connects power supply to chip	1	1
VOUT	Output from circuit	2	3
GND	Ground	3	2

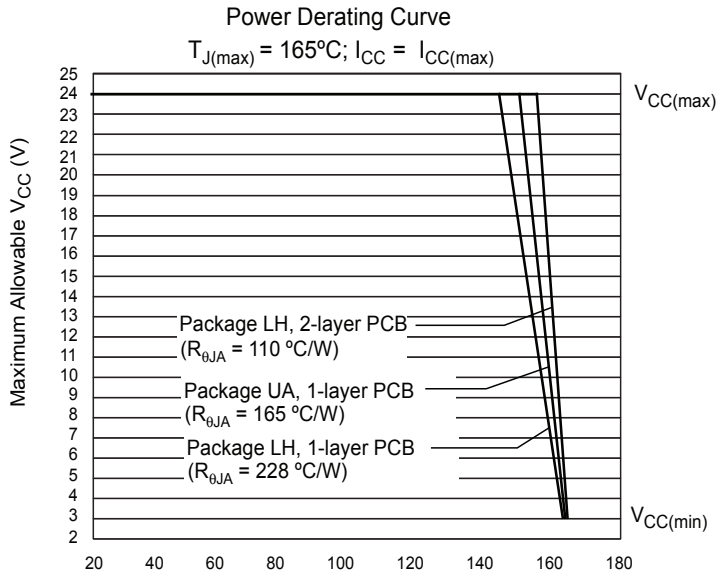
ELECTRICAL CHARACTERISTICS Valid valid over full operating voltage and ambient temperature ranges; unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ.[1]	Max.	Unit[2]
Electrical Characteristics							
Forward Supply Voltage	V_{CC}	Operating, T_J < 165°C		3	–	24	V
Output Leakage Current	I_{OUTOFF}	V_{OUT} = 24 V, B < B_{RP}		–	–	10	µA
Output Saturation Voltage	$V_{OUT(SAT)}$	I_{OUT} = 20 mA, B > B_{OP}		–	185	500	mV
Output Current Limit	I_{OM}	B > B_{OP}		30	–	60	mA
Power-On Time[3]	t_{PO}	V_{CC} > 3.0 V, B < B_{RP}(min) – 10 G, B > B_{OP}(max) + 10 G		–	–	25	µs
Chopping Frequency	f_C			–	800	–	kHz
Output Rise Time[3,4]	t_r	R_L = 820 Ω, C_L = 20 pF		–	0.2	2	µs
Output Fall Time[3,4]	t_f	R_L = 820 Ω, C_L = 20 pF		–	0.1	2	µs
Supply Current	$I_{CC(ON)}$	B > B_{OP}, V_{CC} = 12 V		–	–	4	mA
	$I_{CC(OFF)}$	B < B_{RP}, V_{CC} = 12 V		–	–	4	mA
Reverse Supply Current	I_{RCC}	V_{RCC} = –30 V		–	–	–5	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 5 mA; T_A = 25°C		28	–	–	V
Zener Impedance	I_Z	I_{CC} = 5 mA; T_A = 25°C		–	50	–	Ω
Magnetic Characteristics							
Operate Point	B_{OP}	A1220		5	22	40	G
		A1221		15	50	90	G
		A1222		70	110	150	G
		A1223		100	150	180	G
Release Point	B_{RP}	A1220		–40	–23	–5	G
		A1221		–90	–50	–15	G
		A1222		–150	–110	–70	G
		A1223		–180	–150	–100	G
Hysteresis	B_{HYS}	A1220	(B_{OP} – B_{RP})	10	45	80	G
		A1221		30	100	180	G
		A1222		140	220	300	G
		A1223		200	300	360	G

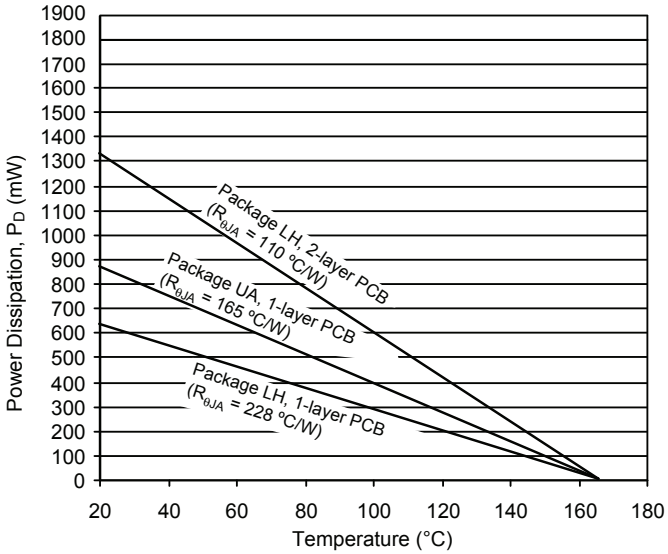
[1]Typical data are are at T_A = 25°C and V_{CC} = 12 V, and are for initial design estimations only.
[2]1 G (gauss) = 0.1 mT (millitesla).
[3]Guaranteed by device design and characterization.
[4]C_L = oscilloscope probe capacitance.

THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	ºC/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area each side connected by thermal vias	110	ºC/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	ºC/W



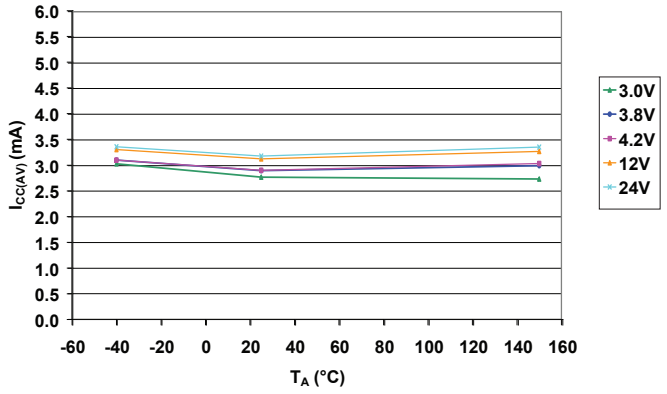
Power Dissipation versus Ambient Temperature



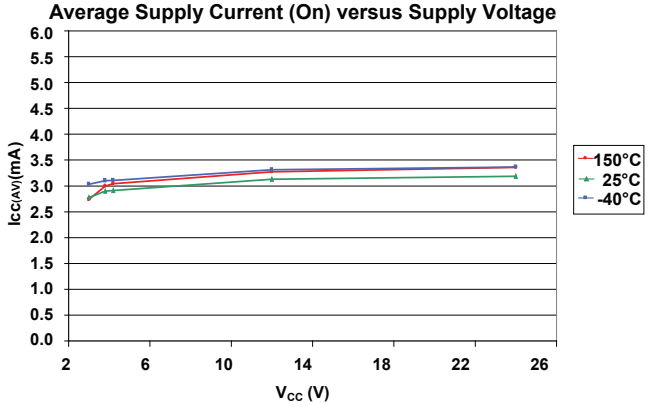
Characteristic Performance

A1220, A1221, A1222, and A1223 Electrical Characteristics

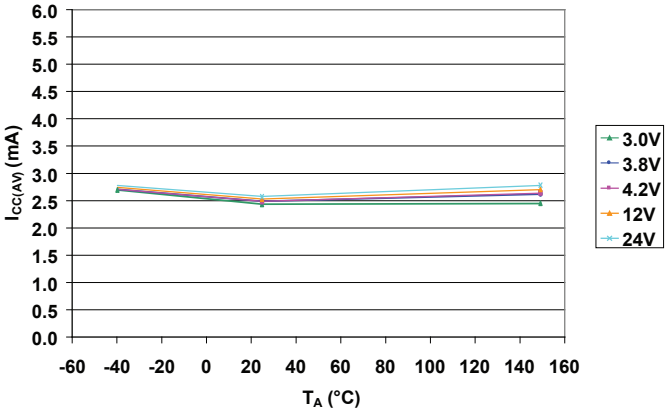
Average Supply Current (On) versus Temperature



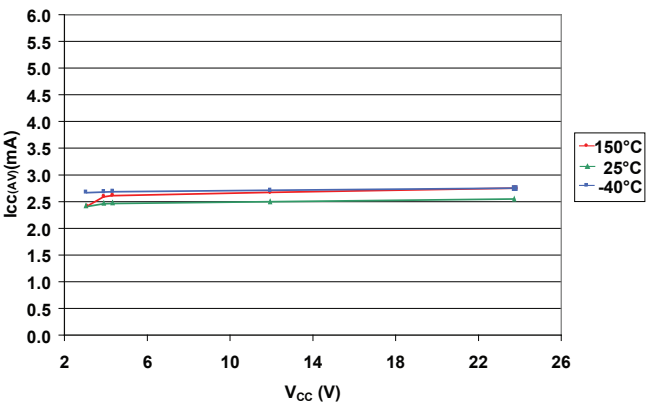
Average Supply Current (On) versus Supply Voltage



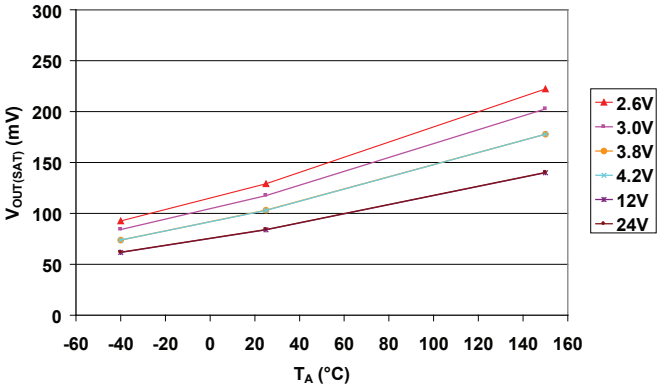
Average Supply Current (Off) versus Temperature



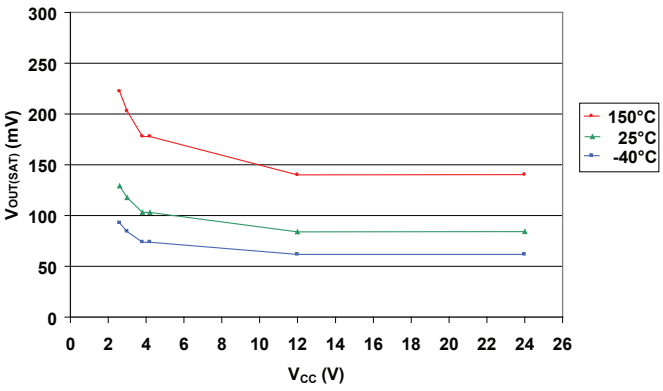
Average Supply Current (Off) versus Supply Voltage



Saturation Voltage versus Temperature

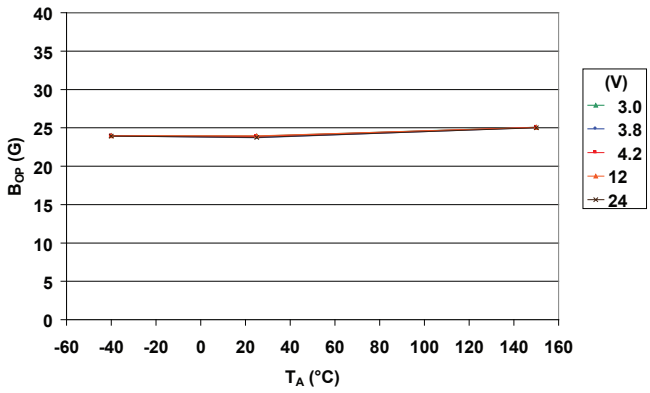


Saturation Voltage versus Supply Voltage

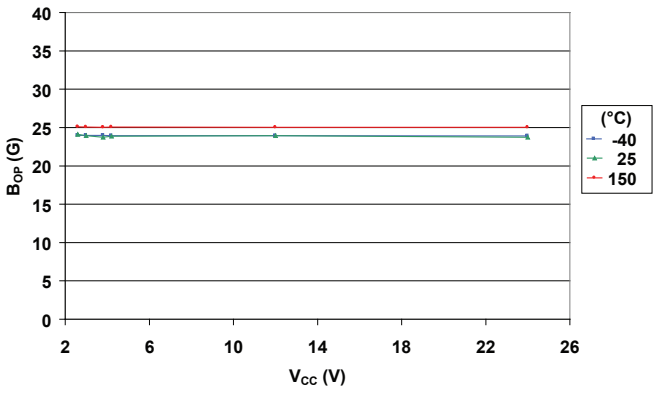


A1220 Magnetic Characteristics

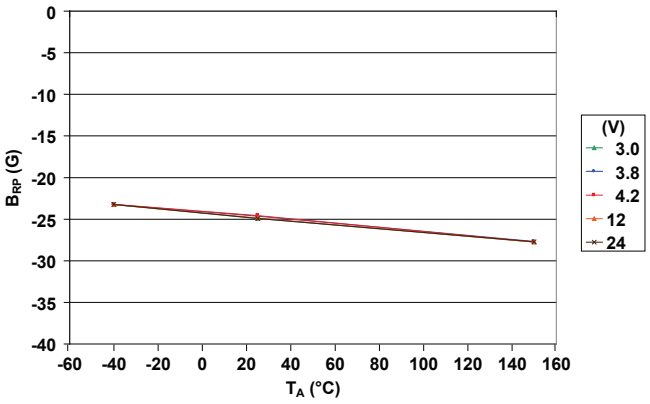
Operate Point versus Temperature



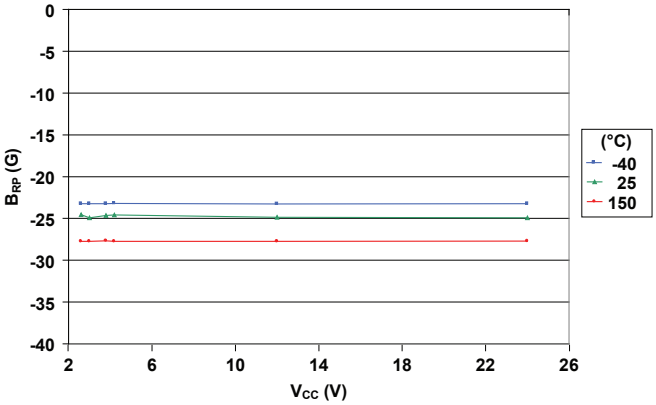
Operate Point versus Supply Voltage



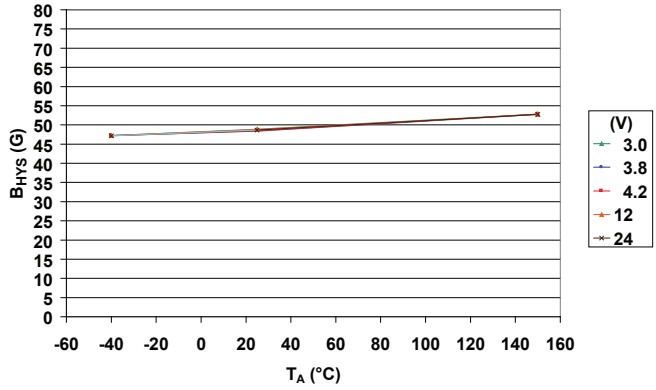
Release Point versus Temperature



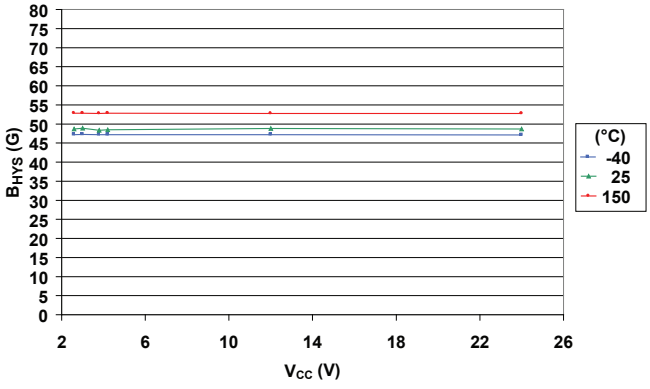
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Temperature

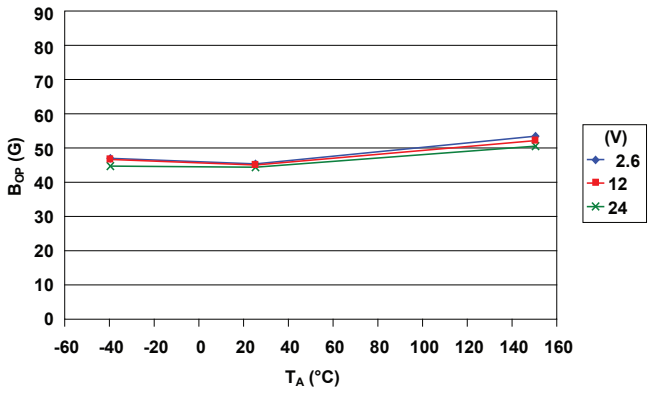


Switchpoint Hysteresis versus Supply Voltage

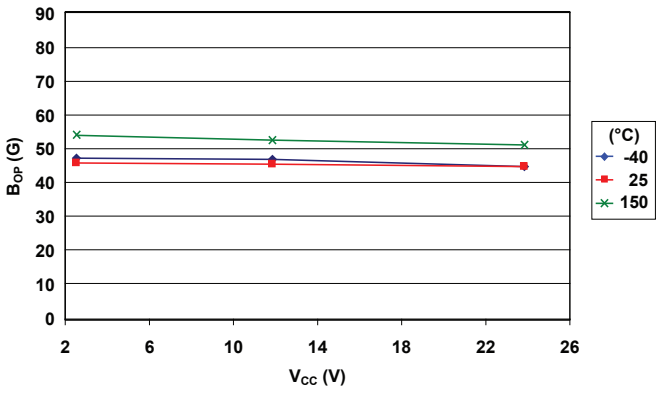


A1221 Magnetic Characteristics

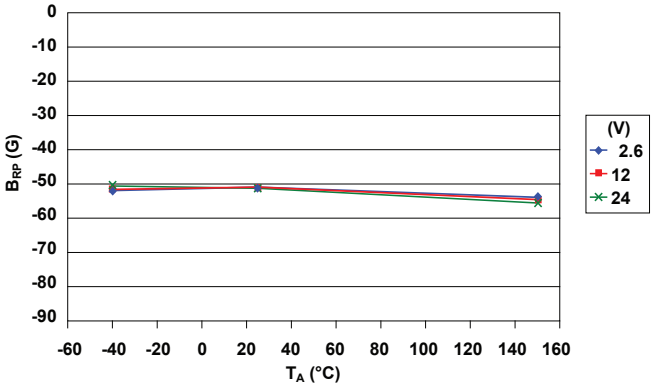
Operate Point versus Temperature



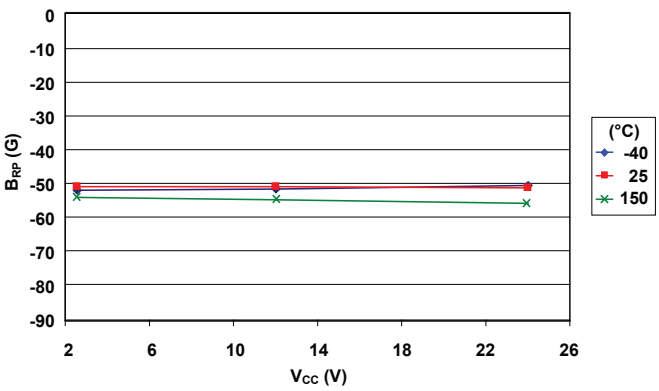
Operate Point versus Supply Voltage



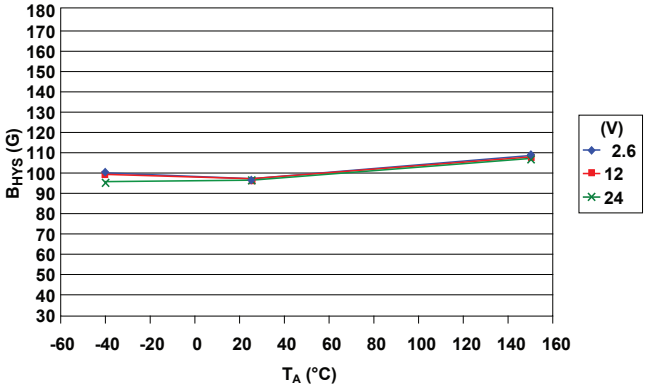
Release Point versus Temperature



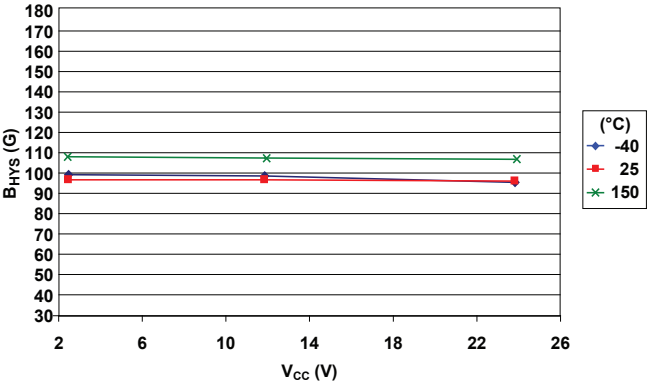
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Temperature

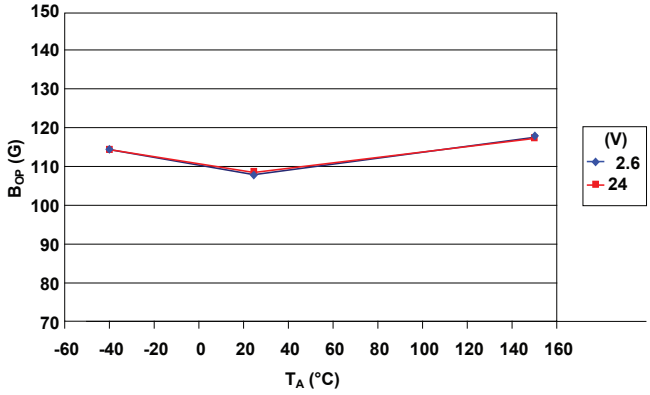


Switchpoint Hysteresis versus Supply Voltage

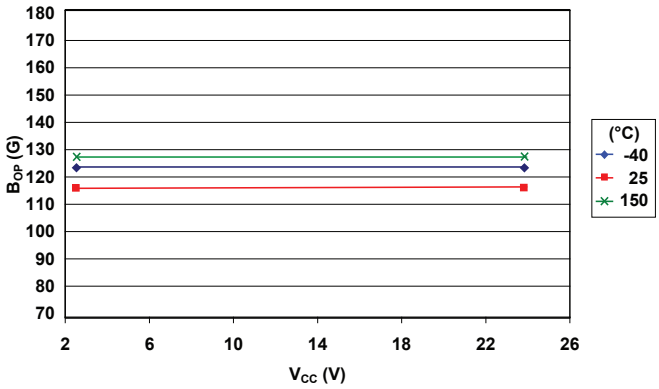


A1222 Magnetic Characteristics

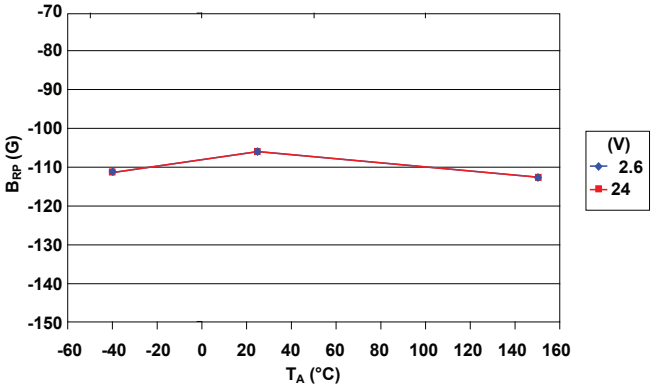
Operate Point versus Temperature



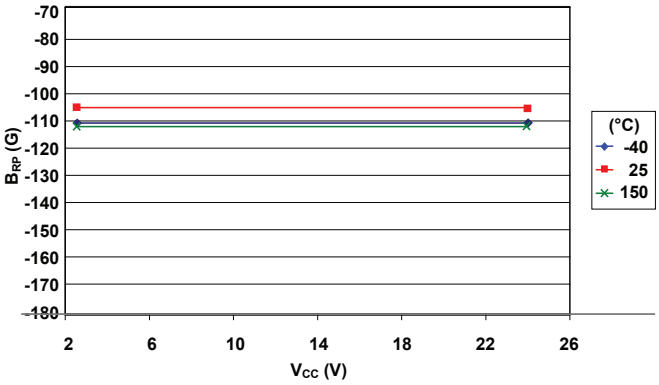
Operate Point versus Supply Voltage



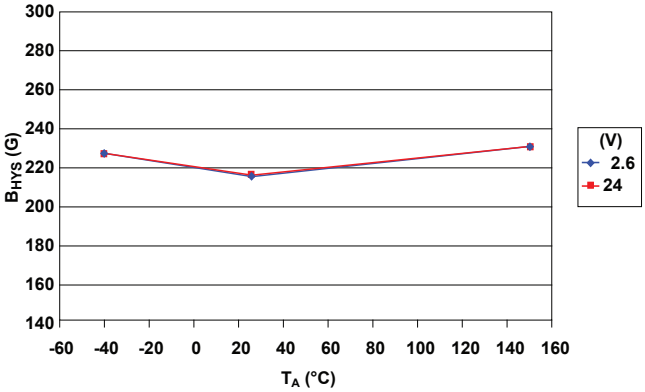
Release Point versus Temperature



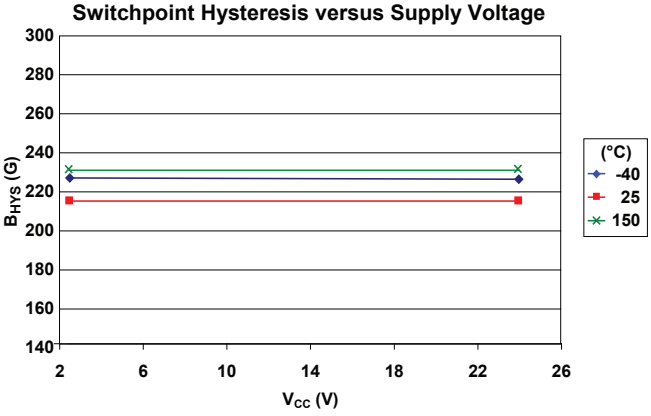
Release Point versus Supply Voltage



Switchpoint Hysteresis versus Temperature



Switchpoint Hysteresis versus Supply Voltage



Functional Description

Operation

The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold, B_{OP} (see panel A of figure 1). After turn-on, the output voltage is $V_{OUT(SAT)}$. The output transistor is capable of sinking current up to the short circuit current limit, I_{OM}, which is a minimum of 30 mA. When the magnetic field is reduced below the release point, B_{RP}, the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Removal of the magnetic field will leave the device output latched on if the last crossed switchpoint is B_{OP}, or latched off if the last crossed switch point is B_{RP}.

Powering-on the device in the hysteresis range (less than B_{OP} and higher than B_{RP}) will give an indeterminate output state. The correct state is attained after the first excursion beyond B_{OP} or B_{RP}.

Applications

It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in panel B of figure 1, a 0.1 µF capacitor is typical.

Extensive applications information for Hall effect devices is available in:

• *Hall-Effect IC Applications Guide*, Application Note 27701

• *Guidelines for Designing Subassemblies Using Hall-Effect Devices*, Application Note 27703.1

• *Soldering Methods for Allegro's Products – SMT and Through-Hole*, Application Note 26009

All are provided in *Allegro Electronic Data Book*, AMS-702, and the Allegro Web site, www.allegromicro.com.

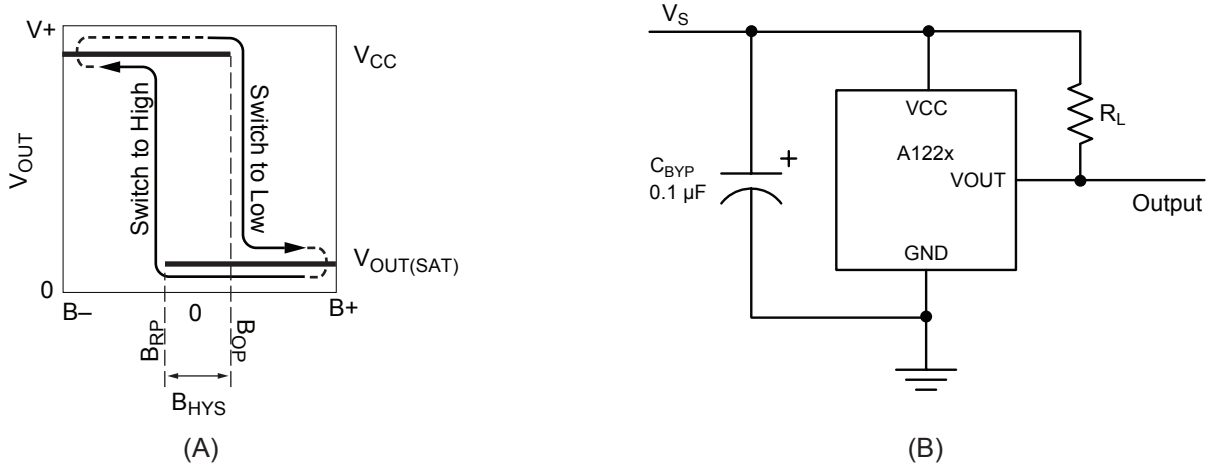


Figure 1. Switching behavior of latches. In panel A, on the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity). This behavior can be exhibited when using a circuit such as that shown in panel B.

Chopper Stabilization Technique

When using Hall effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall element. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated DC offset is suppressed. This configuration is illustrated in figure 2.

The chopper stabilization technique uses a 400 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (800 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications, Allegro recommends its digital device families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

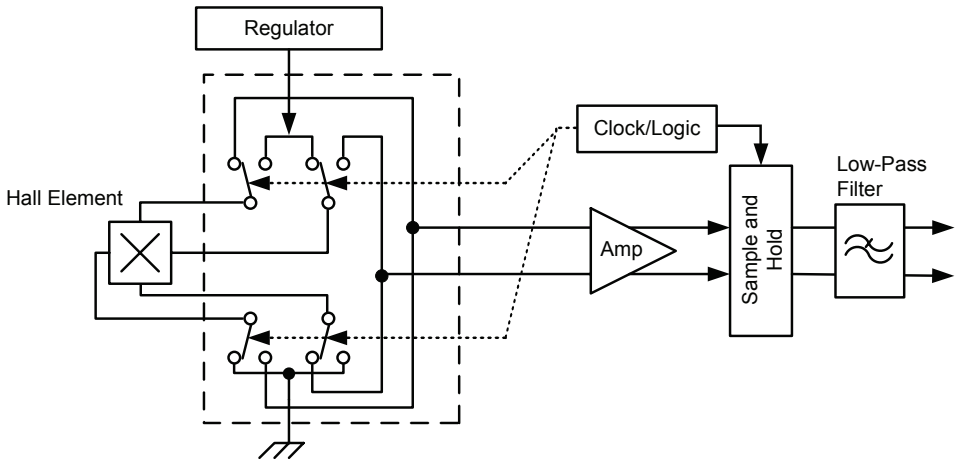


Figure 2. Model of chopper stabilization technique

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \qquad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \qquad (2)$$

$$T_J = T_A + \Delta T \qquad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 1.6 mA, and $R_{\theta JA}$ = 165 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 1.6\ mA = 19\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 19\ mW \times 165\ °C/W = 3°C$$

$$T_J = T_A + \Delta T = 25°C + 3°C = 28°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package LH, using a minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=228°C/W, $T_J(max)$ = 165°C, $V_{CC}(max)$ = 24 V, and $I_{CC}(max)$ = 4 mA.

Calculate the maximum allowable power level, $P_D(max)$. First, invert equation 3:

$$\Delta T_{max} = T_J(max) - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_D(max) = \Delta T_{max} \div R_{\theta JA} = 15°C \div 228\ °C/W = 66\,mW$$

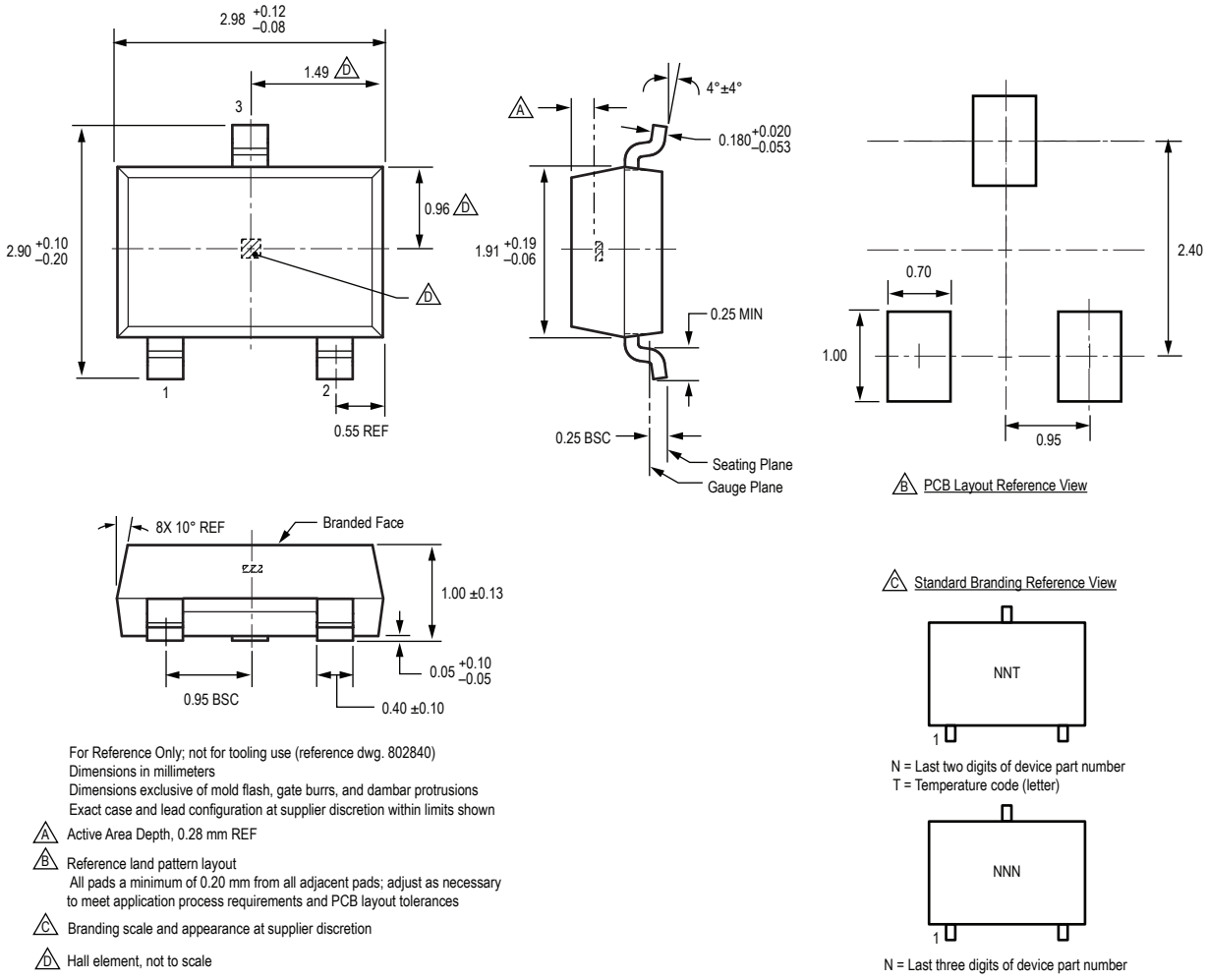
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_D(max) \div I_{CC}(max) = 66\,mW \div 4\,mA = 16.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC}(max)$. If $V_{CC(est)} \leq V_{CC}(max)$, then reliable operation between $V_{CC(est)}$ and $V_{CC}(max)$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC}(max)$, then operation between $V_{CC(est)}$ and $V_{CC}(max)$ is reliable under these conditions.

Package LH, 3-Pin (SOT-23W)



For Reference Only; not for tooling use (reference dwg. 802840)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

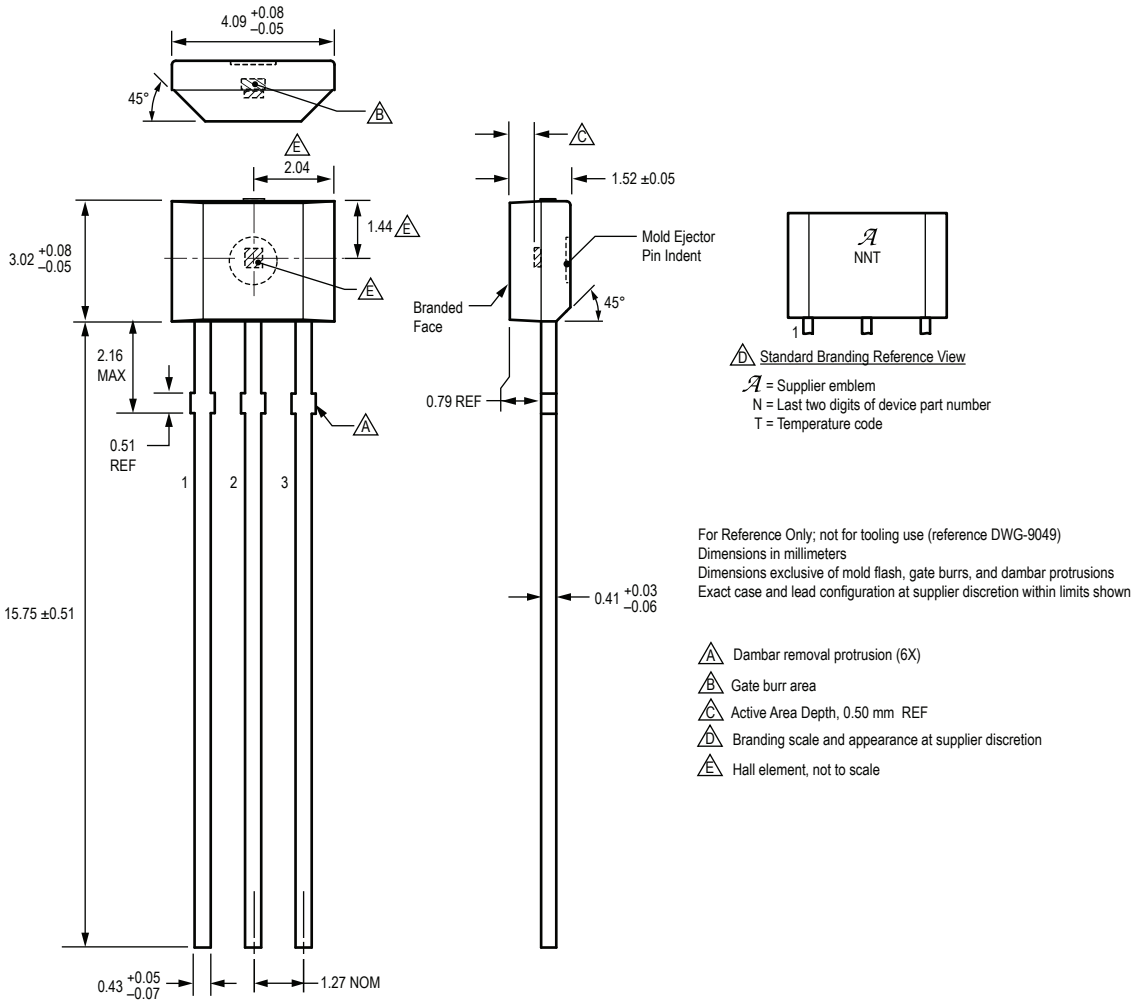
A Active Area Depth, 0.28 mm REF

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

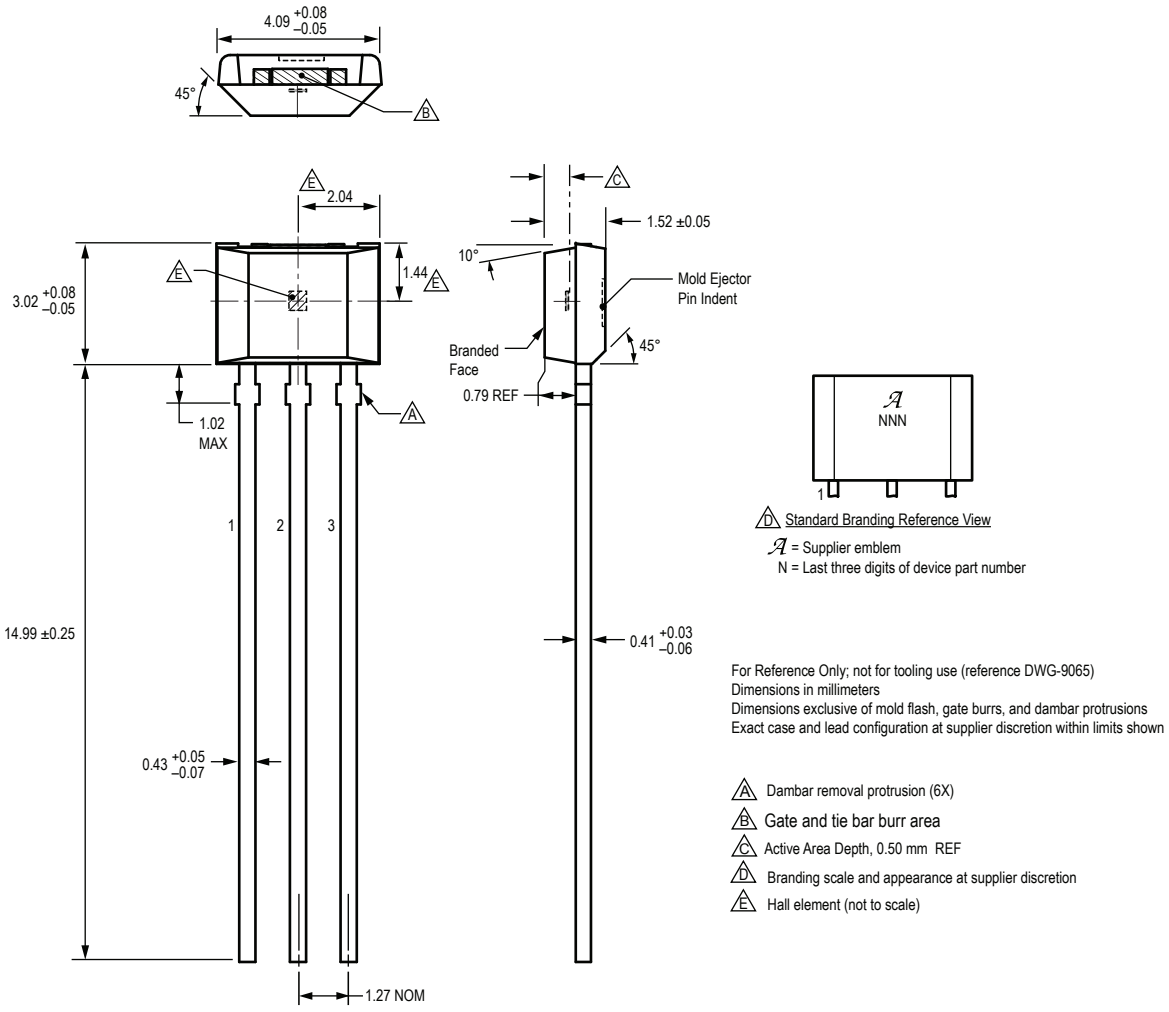
Package UA, 3-Pin SIP
(A1220 and A1221)



For Reference Only; not for tooling use (reference DWG-9049)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element, not to scale

Package UA, 3-Pin SIP
(A1222 and A1223)



For Reference Only; not for tooling use (reference DWG-9065)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (6X)
B Gate and tie bar burr area
C Active Area Depth, 0.50 mm REF
D Branding scale and appearance at supplier discretion
E Hall element (not to scale)

Revision History

Revision	Current Revision Date	Description of Revision
15	September 16, 2013	Update UA package drawing
16	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits

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