

CD4063B Types

CMOS 4-Bit Magnitude Comparator

High Voltage Types (20-Volt Rating)

■ CD4063B is a 4-bit magnitude comparator designed for use in computer and logic applications that require the comparison of two 4-bit words. This logic circuit determines whether one 4-bit word (Binary or BCD) is "less than", "equal to", or "greater than" a second 4-bit word.

The CD4063B has eight comparing inputs (A_3, B_3 through A_0, B_0), three outputs ($A < B, A = B, A > B$) and three cascading inputs ($A < B, A = B, A > B$) that permit systems designers to expand the comparator function to 8, 12, 16 . . . 4N bits. When a single CD4063B is used, the cascading inputs are connected as follows: ($A < B$) = low, ($A = B$) = high, ($A > B$) = low.

For words longer than 4 bits, CD4063B devices may be cascaded by connecting the outputs of the less-significant comparator to the corresponding cascading inputs of the more-significant comparator. Cascading inputs ($A < B, A = B$, and $A > B$) on the least significant comparator are connected to a low, a high, and a low level, respectively.

The CD4063B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes). This device is pin-compatible with the standard 7485 TTL type.

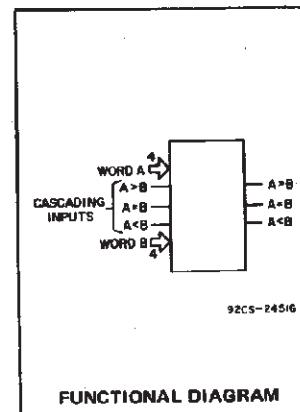
Features:

- Expansion to 8, 12, 16 . . . 4N bits by cascading units
- Medium-speed operation:
compares two 4-bit words
in 250 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V
over full package temperature range;
100 nA at 18 V and 25°C
- Noise margin (full package temperature range)
range) = 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V

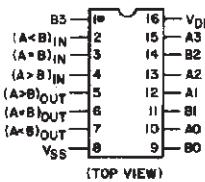
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Servo motor controls ■ Process controllers



FUNCTIONAL DIAGRAM



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal) -0.5V to +20V

INPUT VOLTAGE RANGE, ALL INPUTS

-0.5V to V_{DD} +0.5V

DC INPUT CURRENT, ANY ONE INPUT

±10mA

POWER DISSIPATION PER PACKAGE (P_D):

For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$ 500mW

For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$ Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

100mW

FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)

-55°C to $+125^\circ\text{C}$

OPERATING-TEMPERATURE RANGE (T_A)

-65°C to $+150^\circ\text{C}$

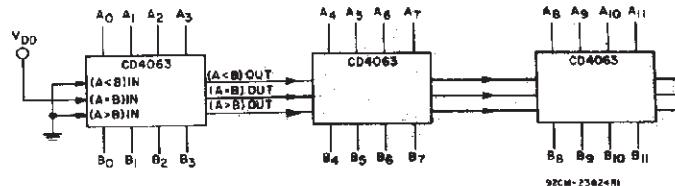
STORAGE TEMPERATURE RANGE (T_{STG})

-65°C to $+150^\circ\text{C}$

LEAD TEMPERATURE (DURING SOLDERING):

+265°C

At distance $1/16 \pm 1/32$ inch (1.59 \pm 0.79mm) from case for 10s, max



$t_p^{\text{TOTAL}} = t_p^{\text{(COMPARE)}} + 2 \times t_p^{\text{(CASCADE)}}$, AT $V_{DD} = 10$ V
(3 STAGES)

= $250 + (2 \times 200) = 650$ ns (TYP)

Fig. 1 — Typical speed characteristics of a 12-bit comparator.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A =Full Package- Temperature Range)	3	18	V

CD4063B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS	
	V _O (V)	V _{IN} (V)	V _{DD} (V)	+25				Min.	Typ.	Max.		
				-55	-40	+85	+125					
Quiescent Device Current, I _{DD} Max.	-	0,5	5	5	5	150	150	-	0,04	5	μA	
	-	0,10	10	10	10	300	300	-	0,04	10		
	-	0,15	15	20	20	600	600	-	0,04	20		
	-	0,20	20	100	100	3000	3000	-	0,08	100		
Output Low (Sink) Current I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA	
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-		
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-		
Output High (Source) Current I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA	
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-		
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-		
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-		
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0,05				-	0	0,05	V	
	-	0,10	10	0,05				-	0	0,05		
	-	0,15	15	0,05				-	0	0,05		
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4,95				4,95	5	-	V	
	-	0,10	10	9,95				9,95	10	-		
	-	0,15	15	14,95				14,95	15	-		
Input Low Voltage, V _{IL} Max.	0,5, 4,5	-	5	1,5				-	-	1,5	V	
	1,9	-	10	3				-	-	3		
	1,5, 13,5	-	15	4				-	-	4		
Input High Voltage, V _{IH} Min.	0,5, 4,5	-	5	3,5				3,5	-	-	V	
	1,9	-	10	7				7	-	-		
	1,5, 13,5	-	15	11				11	-	-		
Input Current I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA	

3

COMMERCIAL CMOS
HIGH VOLTAGE ICs

TRUTH TABLE

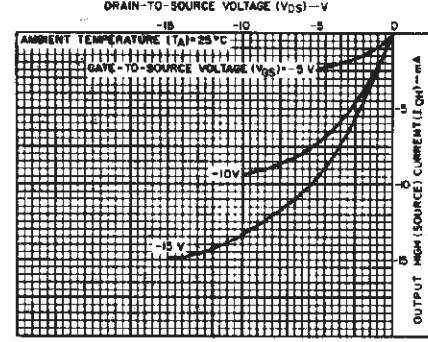
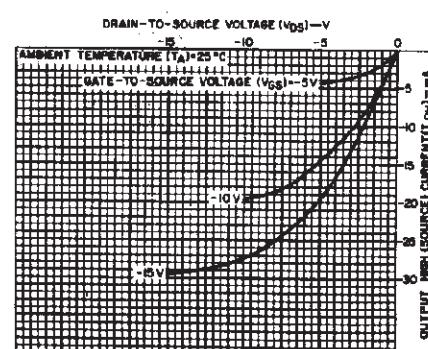
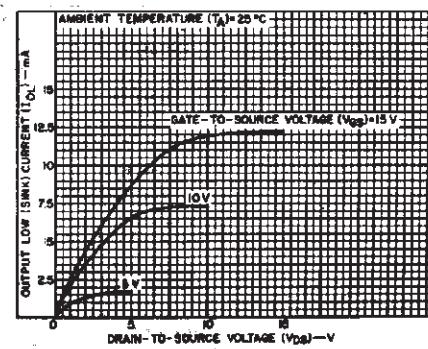
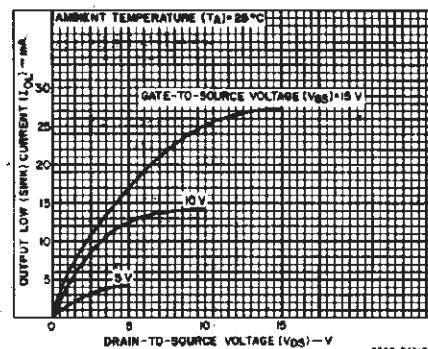
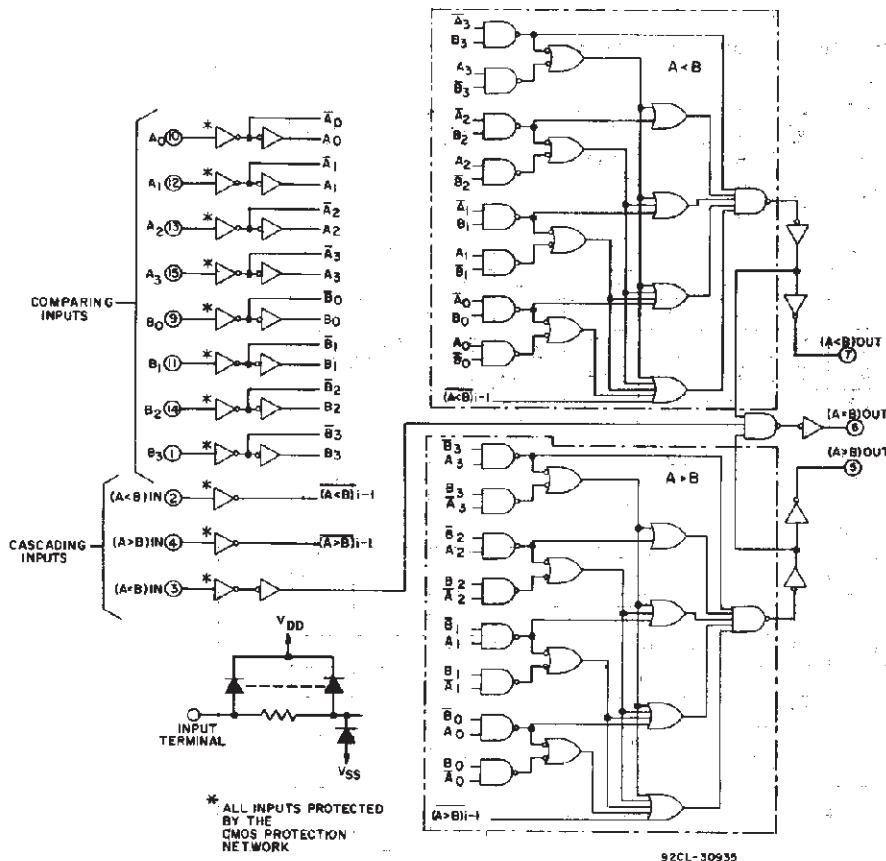
INPUTS				OUTPUTS					
COMPARING				CASCADING					
A ₃ , B ₃	A ₂ , B ₂	A ₁ , B ₁	A ₀ , B ₀	A < B	A = B	A > B	A < B	A = B	A > B
A ₃ > B ₃	X	X	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ > B ₂	X	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ > B ₁	X	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ > B ₀	X	X	X	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0	0	1	0	0	1
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	0	1	0	0	1	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ = B ₀	1	0	0	1	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ = B ₁	A ₀ < B ₀	X	X	X	1	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₁ < B ₁	X	X	X	X	1	0	0
A ₃ = B ₃	A ₂ = B ₂	A ₂ < B ₂	X	X	X	X	1	0	0
A ₃ < B ₃	X	X	X	X	X	X	1	0	0

X = Don't Care

Logic 1 ≡ High Level

Logic 0 ≡ Low Level

CD4063B Types



DYNAMIC ELECTRICAL CHARACTERISTICS

At $T_A = 25^\circ\text{C}$; Input t_p , $t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		V _{DD} Volts	Typ.	Max.	
Propagation Delay Time: Comparing Inputs to Outputs, t_{PHL} , t_{PLH}		5	625	1250	ns
		10	250	500	
		15	175	350	
Cascading Inputs to Outputs, t_{PHL} , t_{PLH}		5	500	1000	
		10	200	400	
		15	140	280	
Transition Time, t_{THL} , t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF	

CD4063B Types

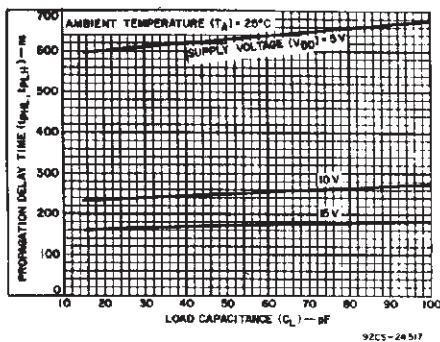


Fig. 7 — Typical propagation delay time vs. load capacitance ("comparing inputs" to outputs).

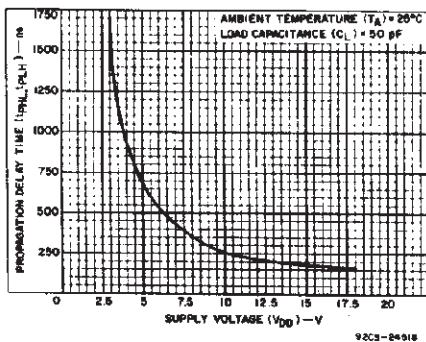


Fig. 8 — Typical propagation delay time vs. supply voltage ("comparing inputs" to outputs).

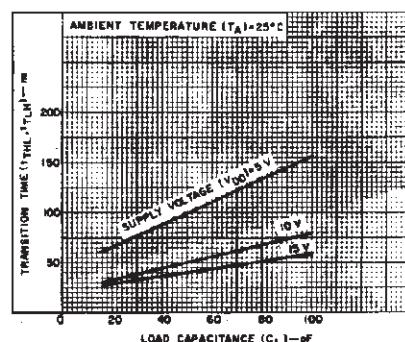


Fig. 9 — Typical transition time vs. load capacitance.

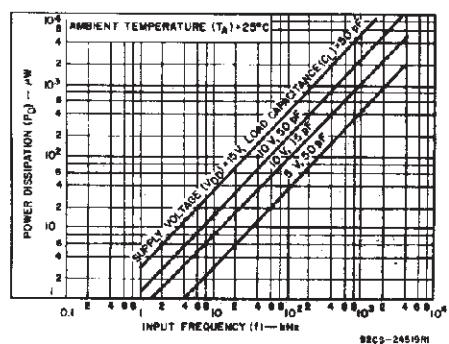


Fig. 10 — Typical power dissipation vs. frequency (see Fig. 12 — dynamic power dissipation test circuit).

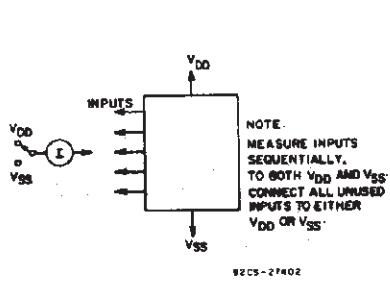


Fig. 11 — Input current test circuit.

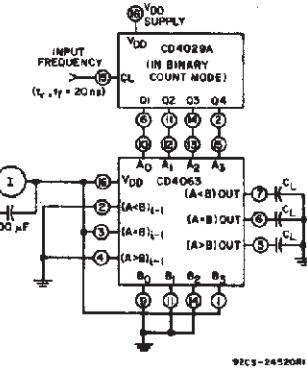


Fig. 12 — Dynamic power dissipation test circuit.

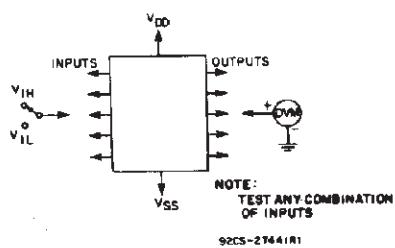


Fig. 13 — Input-voltage test circuit.

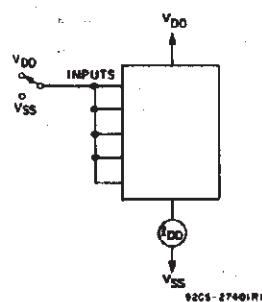
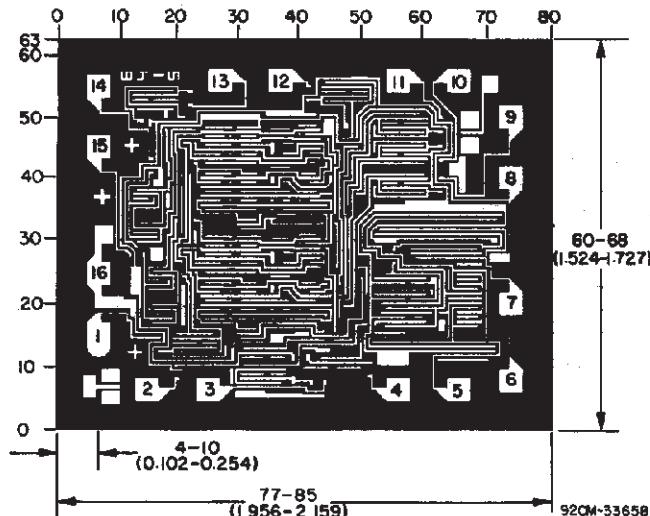


Fig. 14 — Quiescent-device-current test circuit.



Dimensions and pad layout for CD4063BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD4063BE	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4063BE
CD4063BE.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD4063BE
CD4063BF	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4063BF
CD4063BF.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4063BF
CD4063BF3A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4063BF3A
CD4063BF3A.A	Active	Production	CDIP (J) 16	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD4063BF3A
CD4063BM	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4063BM
CD4063BM96	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4063BM
CD4063BM96.A	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4063BM
CD4063BM96E4	Active	Production	SOIC (D) 16	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4063BM
CD4063BMT	Obsolete	Production	SOIC (D) 16	-	-	Call TI	Call TI	-55 to 125	CD4063BM
CD4063BNSR	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4063B
CD4063BNSR.A	Active	Production	SOP (NS) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4063B

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

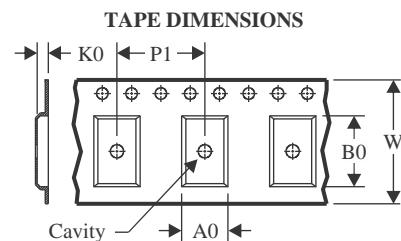
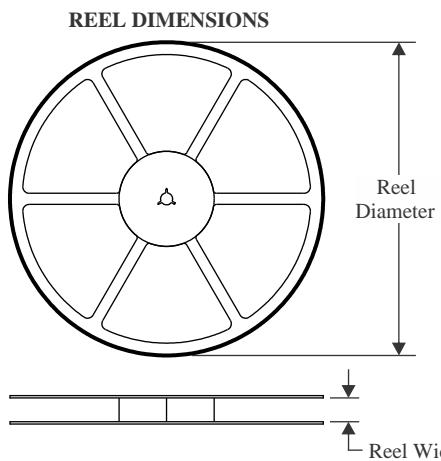
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD4063B, CD4063B-MIL :

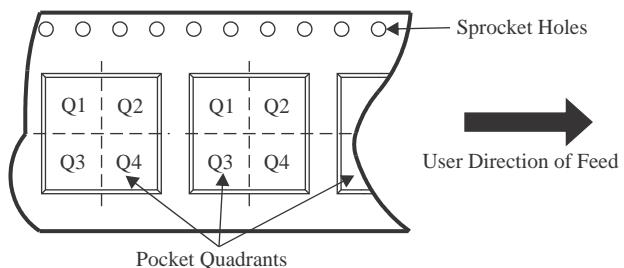
- Catalog : [CD4063B](#)
- Military : [CD4063B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


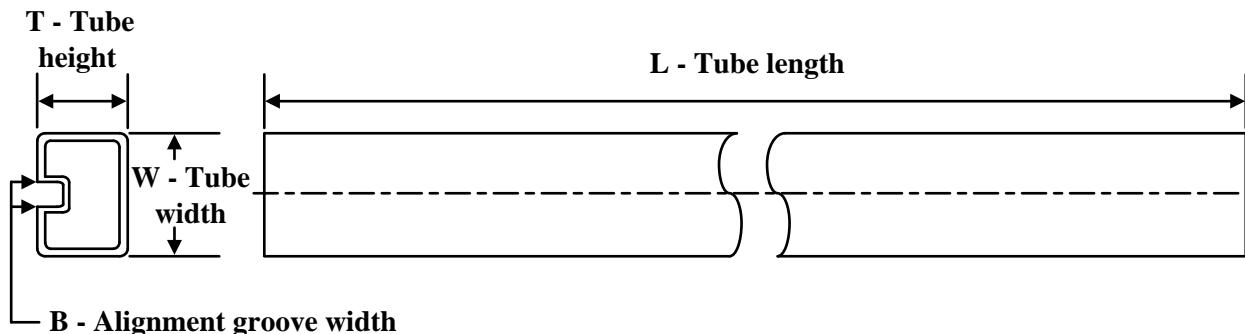
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4063BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD4063BNSR	SOP	NS	16	2000	330.0	16.4	8.1	10.4	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4063BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD4063BNSR	SOP	NS	16	2000	353.0	353.0	32.0

TUBE


*All dimensions are nominal

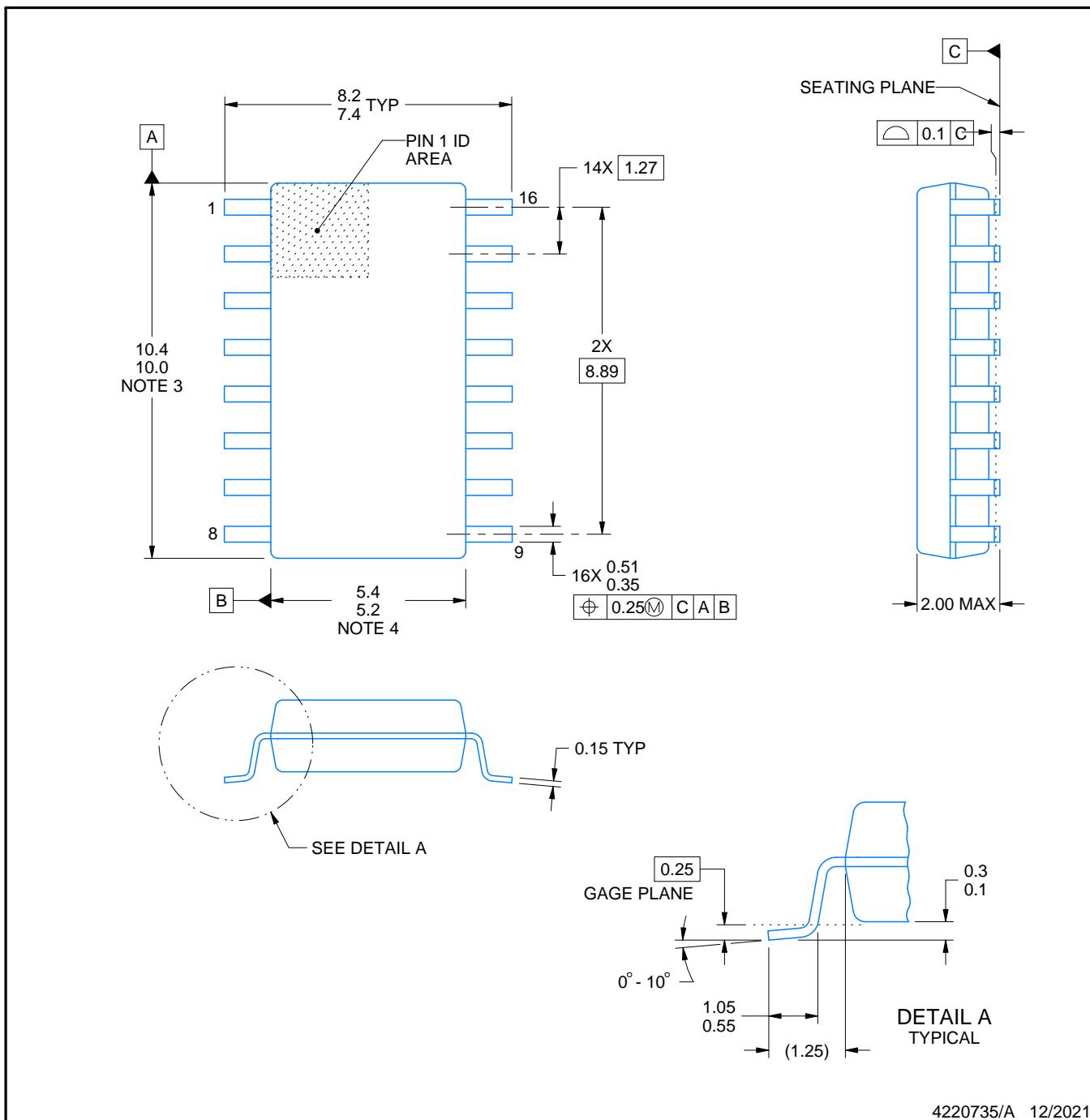
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD4063BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4063BE	N	PDIP	16	25	506	13.97	11230	4.32
CD4063BE.A	N	PDIP	16	25	506	13.97	11230	4.32
CD4063BE.A	N	PDIP	16	25	506	13.97	11230	4.32



PACKAGE OUTLINE

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

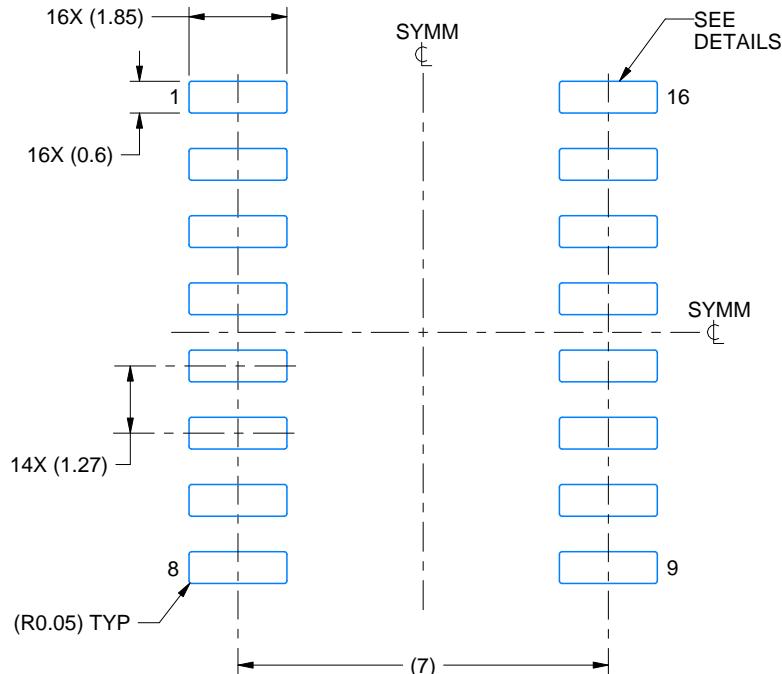
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

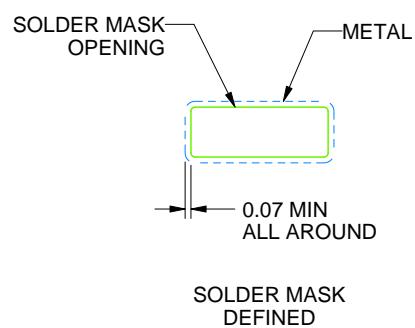
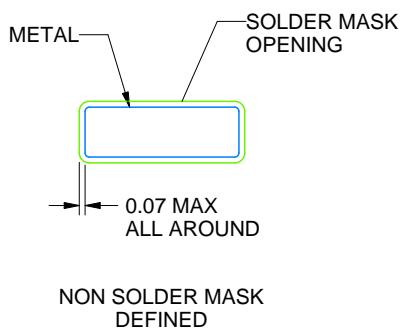
NS0016A

SOP - 2.00 mm max height

SOP



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

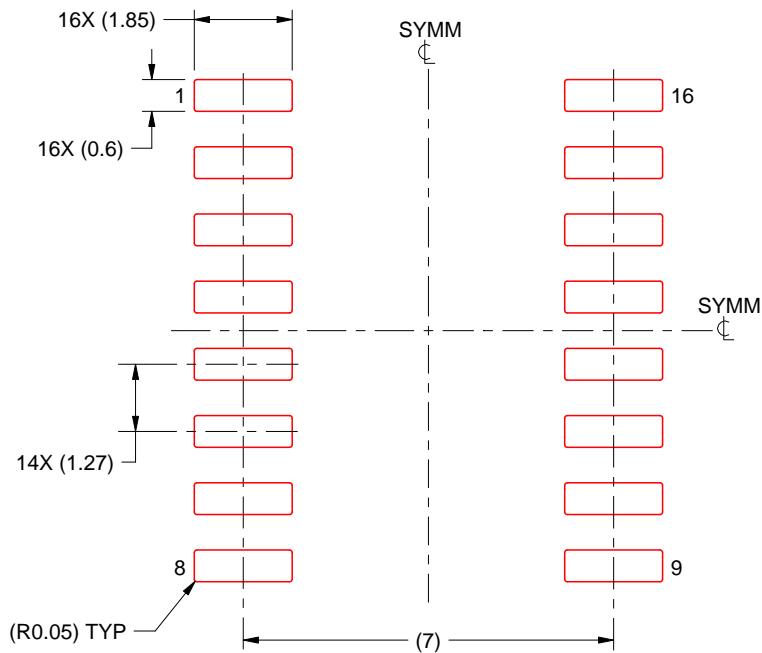
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

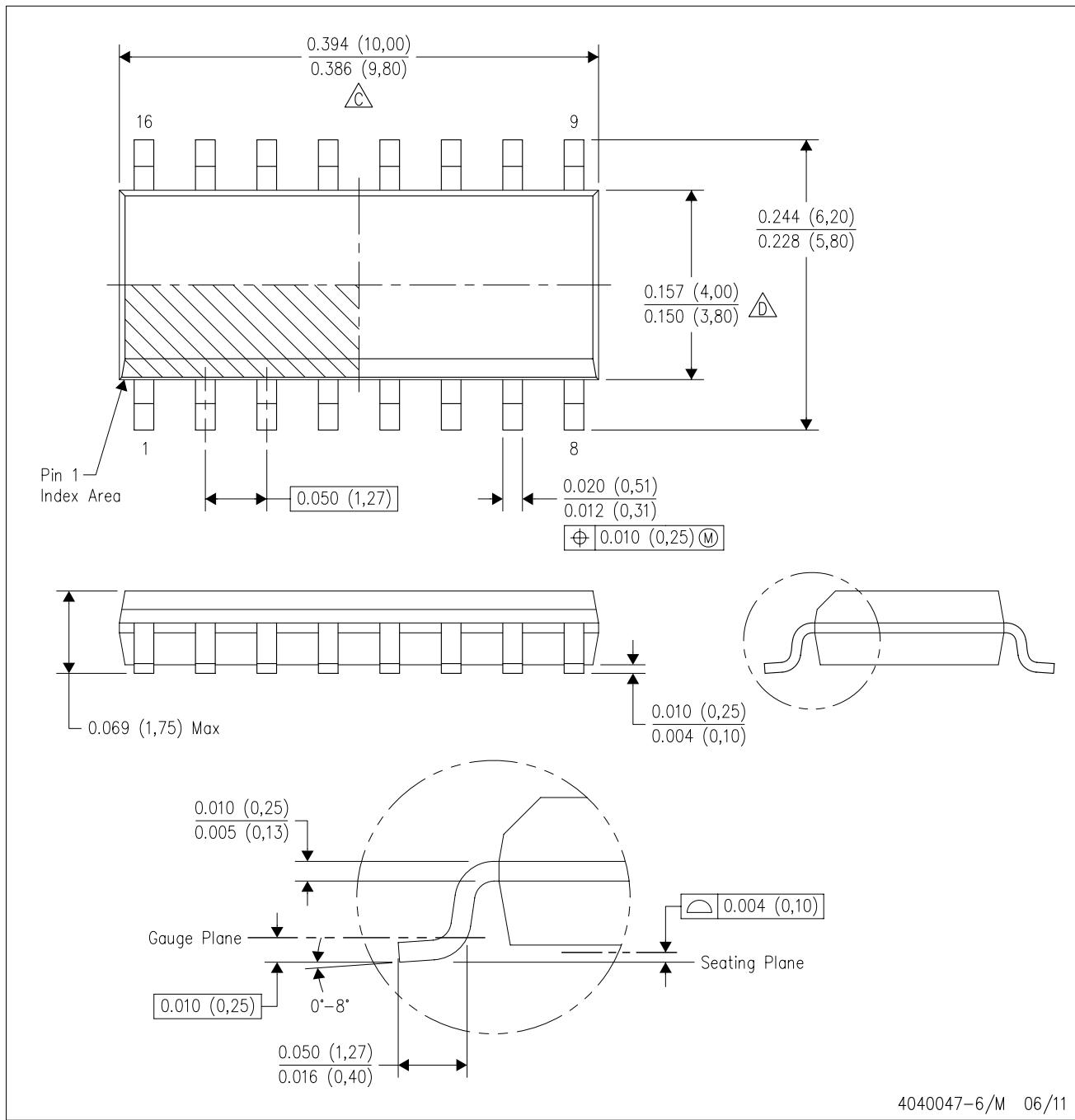
4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

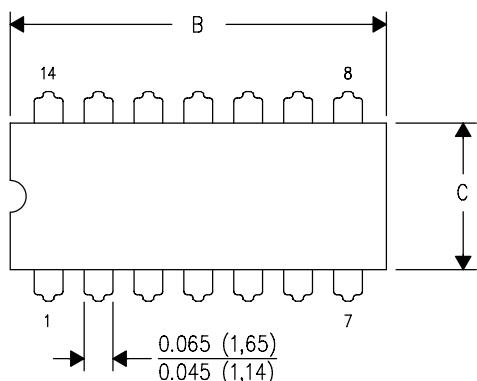
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

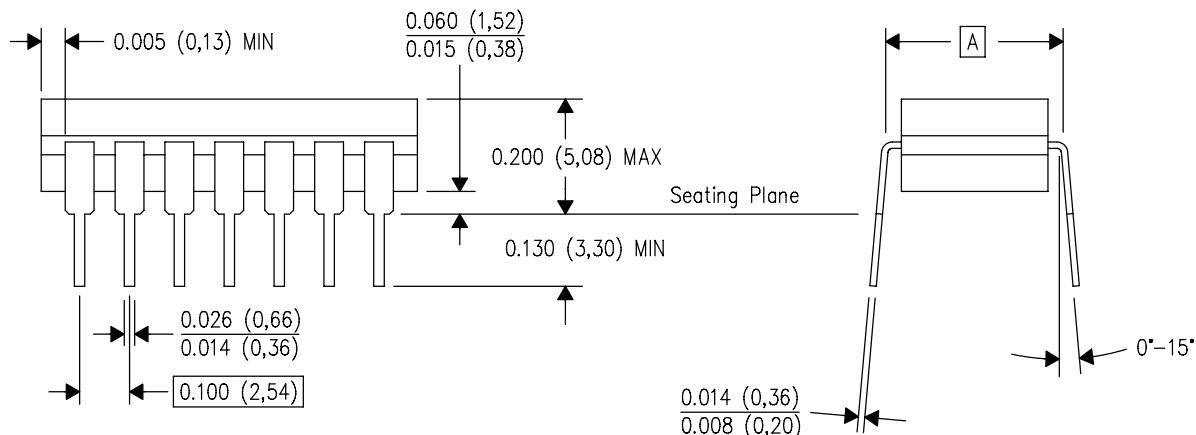
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.