PIC32MK General Purpose and Motor Control (GP/MC) Silicon Errata and Data Sheet Clarification

The PIC32MK General Purpose and Motor Control (GP/MC) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001402**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MK General Purpose and Motor Control (GP/MC) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections (if applicable) start on page 14 following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(1)
		A1
PIC32MK1024MCF100	0x06201053	0x1
PIC32MK1024MCF064	0x06202053	
PIC32MK0512MCF100	0x06204053	
PIC32MK0512MCF064	0x06205053	
PIC32MK1024GPE100	0x06207053	
PIC32MK1024GPE064	0x06208053	
PIC32MK0512GPE100	0x0620A053	
PIC32MK0512GPE064	0x0620B053	
PIC32MK1024GPD100	0x0620D053	
PIC32MK1024GPD064	0x0620E053	
PIC32MK0512GPD100	0x06210053	
PIC32MK0512GPD064	0x06211053	

Note 1: Refer to the **"Memory Organization"** and **"Special Features"** chapters in the current Device Data Sheet (DS60001402**D**) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
Primary Oscillator	POSC	1.	Crystal primary oscillator (POSC) supports reduced operating range with restrictions.	X
Secondary Oscillator	SOSC	2.	The Secondary Oscillator (SOSC) does not support crystal operation.	X
Clocks	PBCLK6	3.	PBCLK6 defaults to 1:2 instead of 1:4.	X
FSCM	Clock Fail	4.	Device falls back to LPRC instead of FRC on FSCM event.	X
VBAT	VBAT	5.	VBAT is not functional.	X
VBAT	RTCC	6.	RTCC may lose SOSC clocks momentarily during a VDD to VBAT switch over event.	X
ADC	Level Trigger	7.	The ADC level trigger will not perform burst conversions in Debug mode.	X
ADC	Turbo Mode	8.	Turbo mode is not functional when two channels are linked for the purpose of increasing effective throughput.	X
ADC	DNL	9.	In Differential mode, DNL for code 3072 is not within specification.	X
ADC	AN26	10.	ADC input AN26 is not functional.	X
ADC	Scan	11.	Scan list conversion will restart without finishing current scan list if new trigger occurs before scan completion with ADC7.	X
ADC	Scan	12.	Shared ADC7 has high Offset and Gain Error in scan mode.	X
Op-Amp	Op amp	13.	Enabling an op amp output control bit disables respective comparators output pin function if also enabled but comparator output status bit is still functional.	X
Op-Amp	Op amp	14.	OPAMP output is always enabled regardless of output enable control bit if OPAMP is enabled.	X
Op-Amp	Op amp PGA Mode	15.	When used in PGA Unity Gain mode, OPAMP continues to function despite being disabled i.e. AMPMOD = 0.	X
Op-Amp	Op amp PGA Mode	16.	Op amps in Unity Gain mode (i.e. CFGCON2<ENPGAx>=1) are non functional.	X
Op-Amp	PSRR	17.	Op amp does not meet PSRR electrical specification.	X
Op-Amp	Common Mode	18.	Op amps do not meet common mode voltage range (VCMR) specification.	X
Op-Amp	CMRR	19.	Op amps do not meet CMRR specification.	X
Op-Amp	Gain Margin	20.	Op amps do not meet gain margin specification.	X
DAC	INL	21.	The DACs do not meet INL specification at AVDD<3v and Ta>85oC.	X
DAC	DNL	22.	The DACs do not meet DNL specification at AVDD<3v.	X
Timer1	Counter Async	23.	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external ext T1CK input.	X
Timer1	Sleep Async	24.	TMR1 register of Timer1 in Asynchronous mode remains at initial set value for 5 external clock pulses after wake-up from Sleep mode.	X
Timer1	Sleep Async	25.	Back-to-back writes to the TMR1 register are not allowed for (4) PBCLK2 cycles.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
I/O	RTCC	26.	RTCC alarm output driver does not return to default/reset state on deep sleep wakeup through MCLR.	X
Deep Sleep	I/O	27.	Deep Sleep mode is non functional.	X
RCON	Register	28.	RCON status bits VBPOR, PORIO, PORCORE, and VBAT are inconsistent and cannot be used.	X
Sleep	IPD	29.	3mA increase in sleep when PB5DIV is disabled.	X
Sleep	IPD	30.	Increase in sleep IPD current if USB pins D+ and D- are floating.	X
PMP	Status Flags	31.	PMP input buffer full flag IB0F and out buffer underflow OBUF are set as soon as PMP is turned ON in Slave mode, when TTLEN = 1.	X
PMP	Slave Mode	32.	CS is de-asserting before RD in Slave mode.	X
CTMU	Triggers	33.	Edge Sequencing mode (EDGSEQEN(CTMUCON<2>)) triggers are not functional	X
CTMU	TGEN	34.	When the TGEN bit is set, manual current sourcing (i.e. setting the EDG1STAT bit) from CTMU is not possible.	X
ICAP	Debug	35.	Debug breakpoints are not supported when using Input Capture with DMA.	X
PWM	Time Base	36.	Leading edge blanking in XPRES mode, PWMCONx<XPRES>=1, is not functional.	X
PWM	I/O	37.	Alternate pin & I/O functions on unused PWM channels do not function when the PWM module is enabled.	X
PWM	LEB	38.	Incorrect LEB trigger applied if dead time is enabled.	X
PWM	Interrupts	39.	Multiple PWM Interrupts can occur for a single TRGIF, PWMLIF, and PWMHIF interrupt events and it cause the ISR to be re-executed multiple times if the PWM pre-scalar (i.e., PTCON<PCLKDIV> or STCON< SCLKDIV>) is greater than 5.	X
UART	Tx/Rx Int	40.	UART Transmit UxSTA<UTXISEL> = 0b00 Interrupt is generated and asserted while the transmit buffer contains at least one empty space and the UART receiver UxSTA<URXISEL> = 0b00 interrupt flag bit is asserted while receive buffer is not empty and non functional.	X
UART	Tx Int	41.	UART Transmit UxSTA<UTXISEL> = 0b01 Interrupt is generated but does not remain asserted when all the characters have been transmitted.	X
UART	Tx Int	42.	UART Transmit UxSTA<UTXISEL> = 0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty.	X
UART	Rx Int	43.	UART Receive UxSTA<URXISEL> = 0b01 interrupt flag bit is asserted only when receive buffer = ½ full and not when receive buffer > ½ full.	X
UART	Rx Int	44.	UART receive UxSTA<URXISEL> = 0b10 interrupt flag bit is asserted only when receive buffer = ¾ full and not when receive buffer > ¾ full.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item	Issue Summary	Affected Revisions(1)
				A1
Temperature Sensor	Temperature Sensor	45.	Temperature sensor is not functional.	X
CAN	Interrupt	46.	The CAN CxINT<WAKIF> (wake interrupt flag) bit is set even when the CAN module is disabled.	X
DMT	Reset	47.	The DMT module does not cause an NMI on a BAD1, BAD2, or DMTEVENT.	X
WDT	WDT	48.	Multiple valid key writes can be performed outside the WDT window before a Reset occurs instead of the required single write.	X
ICSP	TDO	49.	The TDO pin becomes an output and toggles while programming on any of the ICSP PGECx/PGEDx pair.	X
VIH	Input Specification	50.	VIH(MIN) does not meet the electrical specification of (0.65*VDD), but instead VIH(MIN) = (0.8*VDD).	X
Cache	Exception	51.	Data Bus Error Exception can occur when pre-fetch cache is enabled, CHECON<PREFEN>=0b01.	X
BOR	POR	52.	On a BOR event when DEVCFG2<BORSEL> = 0, RCON<POR> status may also be erroneously set.	X
BOR	Reset	53.	On a BOR event, VPOR<VDD<VBOR, Reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins function frozen in their present state until either VDD falls to VPOR or VDD returns to above VBOR.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note 1: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An 'X' indicates the issue is present in this revision of silicon.
- Shaded cells with an Em dash ('—') indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

1. Module: Primary Oscillator

The POSC supports only specific crystal operation. as provided in Table 3.

Work around 1

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented and the operating conditions provided in Table 3 are met.

FIGURE 1: POSC CRYSTAL CIRCUIT

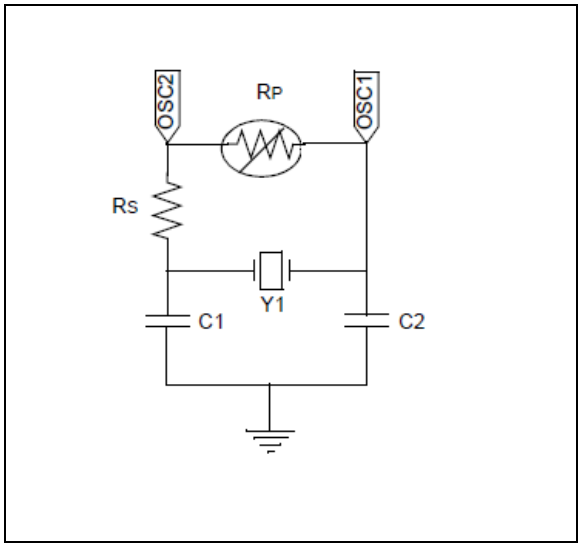


TABLE 3: CRYSTAL SPECIFICATIONS

Crystal Frequency (See Note 1)	Series Resistor Rs	Posc Gain Setting POSCGAIN<1:0> (DEVCFG0<20:19>)	Posc Boost Setting POSCBOOST (DEVCFG0<21>)
8 MHz	2 kΩ	'0b00 (GAIN_0)	'0b1
12 MHz	1 kΩ	'0b00 (GAIN_0)	'0b1
24 MHz(3)	0	'0b00 (GAIN_0)	'0b1

Note 1: Using any other crystal frequency will require special component selection and characterization.

2: A parallel register (RP) should not be used to increase the gain of the POSC.

3: Only 24MHz crystals with a Mfg ESR ≤ 40Ω.

Work around 2

Alternatively, use an external clock or the Internal FRC Oscillator. Note that communication interfaces, such as CAN, USB, etc., with tighter clock accuracy requirements will not function with the FRC as clock source.

Affected Silicon Revisions

A1							
X							

2. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins, SOSCI and SOSCO.

Work around

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC pin is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

Affected Silicon Revisions

A1							
X							

3. Module: Clocks

The PB6DIV<PBDIV> defaults to 0b0000001 (i.e. 1:2) instead of 0b0000011 (i.e. 1:4). The max clock rate for the PBCLK6 bus is 30 MHz.

Work around

Set the PB6DIV<PBDIV> = 0b0000011 (i.e. 1:4) assuming a 120 MHz SYSCLK. This is a register that requires an unlock sequence.

Affected Silicon Revisions

A1							
X							

4. Module: FSCM

When the DEVCFG1<FSCM> = 0b1x, clock fail monitoring is enabled, and a clock fail is detected. The SYSCLK source switches to LPRC instead of FRC as intended.

Work around

If the user has clock software clock switching enabled, DEVCFG1<FSCM> = 0b11, they can perform a clock switch to FRC.

Affected Silicon Revisions

A1							
X							

5. Module: VBAT

The VBAT pin is non functional and it must be connected to VDD.

Work around

None.

Affected Silicon Revisions

A1							
X							

6. Module: VBAT

RTCC may lose Sosc clocks momentarily during a VDD to VBAT switch over event.

Work around

None.

Affected Silicon Revisions

A1							
X							

7. Module: ADC

The ADC level trigger, ADCTRGx=0b00010, will not perform burst conversions in Debug mode.

Work around

Do not use Debug mode with the ADC level triggers.

Affected Silicon Revisions

A1							
X							

8. Module: ADC

Turbo mode, ADCCON1<TRBEN>=1, is not functional when two channels are linked for increasing effective throughput.

Work around

The user can still increase the effective throughput rate by interleaving ADC cores and trigger sources by connecting multiple dedicated high-speed ADCs to the same analog input, see Table Affected Silicon Revisions.

TABLE 4: INTERLEAVED ADC PERFORMANCE VDD > 2.5V

# of Interleaved ADC (12-bit mode)	Minimum TAD Sampling Time (SAMC)	Maximum Effective Sampling Rate (in msps)
2	13	4.615
3	7	8.57
4	5	12
5	4	15
6	3	20

Affected Silicon Revisions

A1							
X							

9. Module: ADC

In Differential mode, code 3072 has a DNL of +3.

Work around

None.

Affected Silicon Revisions

A1							
X							

10. Module: ADC

ADC input AN26 is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

11. Module: ADC

Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and do not generate an ADCCON2<EOSRDY> end of scan interrupt status if a new trigger event from the ADCCON1<STRGSRC> trigger source occurs before the scan list completion on the shared ADC7 core.

Work around

Ensure that the ADCCON1<STRGSRC> trigger source repetition rate > (sample + conversion) time of the sum of all ANx inputs defined in the ADCCSS1/2 registers.

Affected Silicon Revisions

A1							
X							

12. Module: ADC

Shared ADC7 has high Offset and Gain Error up to 38 Lsb in ADC7 Scan mode as defined in the ADCCSS1/2 registers.

Work around

Increase the user defined ADCCON2<SAMC> sample time register value by (4) TAD. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less than 4 Lsb in 12-bit mode.

Affected Silicon Revisions

A1							
X							

13. Module: Op amp

Enabling the op amp output enable bit, CMxCON<OAO>=1, disables the respective comparators output pin function, CxOUT, on a different pin entirely if it was enabled CMxCON<COE>, but the comparator output status bit is still functional.

Work around

None. The same op amp/comparator outputs cannot be enabled simultaneously.

Affected Silicon Revisions

A1							
X							

14. Module: Op amp

When the CMxCON<AMPMOD>=1, the op amp is enabled, the op amp output pin is active regardless of the state of the CMxCON<OAO> op amp output pin enable.

Work around

If the user does not want the op amp output pin to be active, do not enable the op amp until required.

Affected Silicon Revisions

A1							
X							

15. Module: Op amp

Op amp when used in 1x unity gain buffer mode, op amp continues to function despite being disabled, AMPMOD = 0.

Work around

None.

Affected Silicon Revisions

A1							
X							

16. Module: Op amp

Op amps in unity gain mode
(i.e. CFGCON2<ENPGAx>=1) are non functional.

Work around

Do not use op amp unity gain mode or use external 8x resistor signal attenuation network to op amp input and then use op amp with 8x gain for net 1x signal gain.

Affected Silicon Revisions

A1							
X							

17. Module: Op amp

Op amp minimum PSRR electrical spec is -39db versus -75db typical.

Work around

None.

Affected Silicon Revisions

A1							
X							

18. Module: Op amp

Op amps do not meet common mode voltage range specification between 0.4V-0.9V, where CMRR is reduced to < 28db.

Work around

None.

Affected Silicon Revisions

A1							
X							

19. Module: Op amp

Op amps CMRR is <28db at input common mode voltages between 0.4V-0.9V, which is less than the electrical specification of 70db min.

Work around

None.

Affected Silicon Revisions

A1							
X							

20. Module: Op amp

Op amps do not meet the typical gain margin specification of 20, but are instead 15.

Work around

None.

Affected Silicon Revisions

A1							
X							

21. Module: DAC

DACs when sourcing $I_{OUT(MAX)}$ = -1.5mA, do not meet INL ±4Lsb specification when AV_{DD}<3.0V. and Ta>85oC.

Work around

Do not use DACs to source > -0.75mA at 2.6V<AV_{DD} < 3.0V.

Affected Silicon Revisions

A1							
X							

22. Module: DAC

DACs do not meet DNL -1Lsb min specification when AVDD<3.0V. Worst case is -1.5Lsb at 2.2V.

Work around

None.

Affected Silicon Revisions

A1							
X							

23. Module: Timer1

Timer1 in asynchronous external counter mode, (i.e., T1CON<TCS>=1, T1CON<TSYNC>=0, and T1CON<TECS>0b01) does not reflect the first count from an external ext T1CK input.

Work around

None.

Affected Silicon Revisions

A1							
X							

24. Module: Timer1

The TMR1 register of Timer1 in Asynchronous mode, (i.e., T1CON<TCS>=1, T1CON<TSYNC>=0, and T1CON<TECS>0b01), remains at initial set value for 5 external clock pulses after wake up from Sleep mode

Work around

None.

Affected Silicon Revisions

A1							
X							

25. Module: Timer1

Back-to-back writes to the TMR1 register are not allowed for (4) PBCLK2 cycles.

Work around

Wait for (4) PBCLK2 cycles before attempting a second write to the TMR1 register.

Affected Silicon Revisions

A1							
X							

26. Module: I/O

If the I/O function is configured for RTCC alarm output driver, it does not return to default/Reset input high–Z state on wakeup from deep sleep through MCLR.

Work around

None.

Affected Silicon Revisions

A1							
X							

27. Module: Deep Sleep

Deep-Sleep mode is non functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

28. Module: RCON

RCON register status bits VBPOR, PORIO, PORCORE, and VBAT are inconsistent and cannot be used.

Work around

None.

Affected Silicon Revisions

A1							
X							

29. Module: Sleep

If the PB5DIV<ON> = 0, and PBCLK5 is disabled, there is a 3mA increase in sleep IPD current.

Work around

Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

A1							
X							

30. Module: Sleep

There is a 170 uA increase in sleep IPD current if USB pins D+ and D- are unused and left floating.

Work around

Add 50k pull-downs on D+ and D-, and tie Vusb3v3 to Vdd.

Affected Silicon Revisions

A1							
X							

31. Module: PMP

PMP input buffer full flag IB0F and out buffer underflow OBUF are set as soon as PMP is turned ON in Slave mode, when TTLEN = 1.

Work around

After PMP initial initialization complete, and before PMP and interrupts are enabled, clear these bits in user software.

Affected Silicon Revisions

A1							
X							

32. Module: PMP

CS is de-asserting before RD in Slave mode. Slave mode is de-featured.

Work around

None.

Affected Silicon Revisions

A1							
X							

33. Module: CTMU

Edge Sequencing mode (EDGSEQEN(CTMUCON<2>)) and Edge mode are not functional.

Work around

Use level modes.

Affected Silicon Revisions

A1							
X							

34. Module: CTMU

When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit) from CTMU is not possible.

Work around

None.

Affected Silicon Revisions

A1							
X							

35. Module: ICAP

Debug breakpoints are not supported when using Input Capture with DMA.

Work around

None.

Affected Silicon Revisions

A1							
X							

36. Module: PWM

Leading edge blanking in XPRES mode, PWMCONx<XPRES>=1, is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

37. Module: PWM

The PWM module does not relinquish control of the PWM pins even if they are not enabled, (i.e., IOCONx<PENH> = 0 and IOCON<PENL> = 0).

Work around

Disable corresponding unused user PWM channels by setting the appropriate PMD4<PWMxMD> = 1.

Affected Silicon Revisions

A1							
X							

38. Module: PWM

Leading edge LEB trigger is not applied at correct time if dead time is enabled. The trigger is applied before the dead time when it should be applied after the dead time to coincide with the actual dead time delayed PWM signal transition.

Work around

Make leading LEB time (LEBDLYx<LEB[11:0]>) equal to desired LEB time plus respective dead time value.

Affected Silicon Revisions

A1							
X							

39. Module: PWM

Multiple PWM Interrupts occur for single TRGIF, PWMLIF and PWMHIF interrupt events. The ISR is re-executed multiple times if the PWM prescalar (i.e., PTCON<PCLKDIV> or STCON< SCLKDIV>) is greater than 5.

Work around

Insure PTCON<PCLKDIV> and STCON< SCLKDIV> is less than 5.

Affected Silicon Revisions

A1							
X							

40. Module: UART

UART transmit UxSTA<UTXISEL> = 0b00, interrupt is generated and asserted while the transmit buffer contains at least one empty space and the UART receiver UxSTA<URXISEL> = 0b00, interrupt flag bit is asserted while receive buffer is not empty is non functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

41. Module: UART

UART transmit UxSTA<UTXISEL> = 0b01 Interrupt is generated but does not remain asserted when all the characters have been transmitted, i.e., once the IFS bit is cleared by the user, it does not remain asserted even while all characters have been transmitted. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFS flag before writing a new value to TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1							
X							

42. Module: UART

UART transmit UxSTA<UTXISEL> = 0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty, i.e., once the IFS bit is cleared by the user, it does not remain asserted even while transmit buffer is empty. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFS flag before writing a new value to TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1							
X							

43. Module: UART

UART Receive UxSTA<URXISEL> = 0b01 interrupt flag bit is asserted only when receive buffer = ½ full and not when receive buffer > ½ full.

Work around

Before exiting the UART Rx ISR, ensure all the contents of RX Buffer have been read by reading the contents of RX Buffer in the ISR until UxSTA<URXDA> bit is cleared.

Affected Silicon Revisions

A1							
X							

44. Module: UART

UART receive UxSTA<URXISEL> = 0b10 interrupt flag bit is asserted only when receive buffer = ¾ full and not when receive buffer > ¾ full.

Work around

Before exiting the UART Rx ISR, ensure all the contents of RX Buffer have been read by reading the contents of RX Buffer in the ISR until UxSTA<URXDA> bit is cleared.

Affected Silicon Revisions

A1							
X							

45. Module: Temperature Sensor

Band gap Temperature Sensor is not functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

46. Module: CAN

CAN CxINT<WAKIF> (wake interrupt flag) bit is set even when the CAN module is disabled.

Work around

During CAN initialization, before enabling the CAN peripheral, clear the CAN CxINT<WAKIF> bit in user code.

Affected Silicon Revisions

A1							
X							

47. Module: DMT

The DMT module does not cause an NMI on a BAD1, BAD2, or DMTEVENT.

Work around

None.

Affected Silicon Revisions

A1							
X							

48. Module: WDT

Multiple valid key writes can be performed outside the WDT window before a Reset occurs instead of the required single write.

Work around

None.

Affected Silicon Revisions

A1							
X							

49. Module: ICSP

Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

Work around

None.

Affected Silicon Revisions

A1							
X							

50. Module: V_{IH}

$V_{IH(MIN)}$ does not meet the electrical specification of $(0.65*V_{DD})$, but is instead $V_{IH(MIN)}=(0.8*V_{DD})$.

Work around

Although V_{IH} is greater than $V_{OH(MIN)}$=2.4v, $V_{OH(MIN)}$ is a function of $I_{OH(MAX)}$. If the application does not load the V_{IH} input source signal by more than $I_{OH(MAX)}$ by 50%, there should be no issues.

Affected Silicon Revisions

A1							
X							

51. Module: Cache

Data Bus Error Exception can occur when pre-fetch cache is enabled, CHECON<PREFEN>=0b01.

Work around

Users must ensure predictive pre-fetch cache is disabled, CHECON<PREFEN>=0b00.

Affected Silicon Revisions

A1							
X							

52. Module: BOR

On a BOR event when DEVCFG2<BORSEL> = 0, RCON<POR> status may also be erroneously set.

Work around

None.

Affected Silicon Revisions

A1							
X							

53. Module: BOR

On a BOR event, VPOR<VDD<VBOR, a reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins function frozen in their present state until either VDD falls to VPOR or VDD returns to above VBOR. The user must assess if this VDD brownout condition and the resulting frozen I/O pin state has an adverse effect on their application (UART, PWM, I/O, OC, etc.,)

Work around 1

Use an external Reset supervisor/monitor, see Table 5. Some LDO regulators, as listed below, have an embedded reset supervisor included. The required minimum reset trip voltage of the supervisor should be at least (VBOR+0.5v) with DEVCFG0<SMCLR>=0 and DEVCFG2< BORSEL>=1 in the configuration words. This means that the minimum VDD operating voltage of the application needs to be above the reset supervisor maximum trip voltage at [Reset Trip (max) + 0.2v], (i.e. Application VDD(MIN) = ~(VBOR+0.5v+0.2v). The reset supervisor should have an open drain output so as not to interfere with the MPLAB programming/debug tools. This workaround assures that MCLR will generate an internal POR and reset the I/O pins before the VBOR trip point.

Note: For motor control applications utilizing the PWM module, **only Work around 1 is recommended**.

Work around 2

If the application can sustain frozen I/O states for ~2.1ms (UART, CAN, I/O, etc.,), then the application must enable Deep Sleep Watchdog Timer and Clock Fail Monitor, based on the details provided in Table 5 and Table 6. If implemented correctly, after ~2.1ms, a valid internal reset state is entered and the I/O pins are set to the device default reset state.

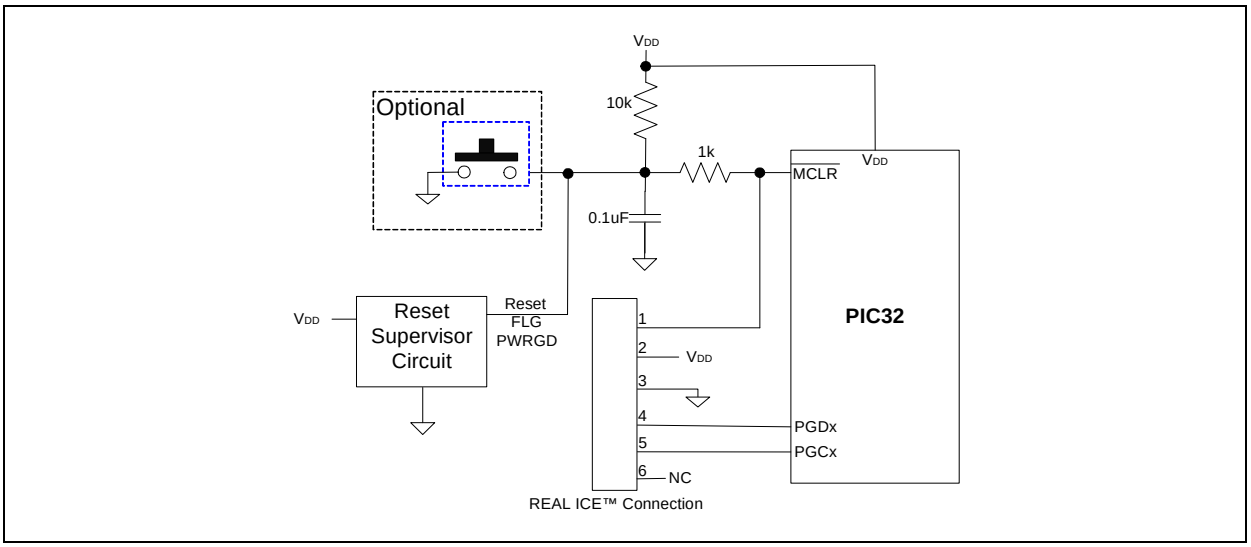
TABLE 5: RESET SUPERVISOR / VOLTAGE MONITOR

Part#	Reset Trip	CPU MCLR Source
MIC803-26D2VC3	2.63v	Reset pin (Open Drain)

TABLE 6: LDOS WITH EMBEDDED RESET SUPERVISOR

Part#	Topology	VIN(MAX)	VOUT	IOUT	Reset Trip	CPU MCLR Source
MIC5239-3.3YM	LDO	30V	3.3V	500mA	3.3V-5%	FLG pin (Open Drain)
MIC5239-3.3YMM						
MCP1725-3302E/MC	LDO	6V	3.3V	500mA	3.3V-10%	PWRGD pin (Open Drain)
MCP1727-3302E/MF	LDO	6V	3.3V	1500mA	3.3V-10%	PWRGD pin (Open Drain)

FIGURE 2: RESET SUPERVISOR CIRCUIT



Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001402**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues to report.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Added silicon issues 1. (Primary Oscillator), 2. (Secondary Oscillator), 3. (Clocks), 4. (FSCM), 5. (VBAT), 6. (VBAT), 7. (ADC), 8. (ADC), 9. (ADC), 10. (ADC), 11. (ADC), 12. (ADC), 13. (Op-Amp), 14. (Op-Amp), 15. (Op-Amp), 16. (Op-Amp), 17. (Op-Amp), 18. (Op-Amp), 19. (Op-Amp), 20. (Op-Amp), 21. (DAC), 22. (DAC), 23. (Timer1), 24. (Timer1), 25. (Timer1), 26. (I/O), 27. (Deep Sleep), 28. (RCON), 29. (Sleep), 30. (Sleep), 31. (PMP), 32. (PMP), 33. (CTMU), 34. (CTMU), 35. (ICAP), 36. (PWM), 37. (PWM), 38. (PWM), 39. (PWM), 40. (UART), 41. (UART), 42. (UART), 43. (UART), 44. (UART), 45. (Temperature Sensor), 46. (CAN), 47. (DMT), 48. (WDT), 49. (ICSP), 50. (VIH), 51. (Cache), 52. (BOR), 53. (BOR).

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