PIC18F66K80

PIC18F66K80 Family
Silicon Errata and Data Sheet Clarification

The PIC18F66K80 family devices that you have received conform functionally to the current Device Data Sheet (DS39977**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F66K80 silicon.

> **Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the Refresh Debug Tool Status icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the Output window.

> **Note:** If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F66K80 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A2	A3	A4	A6
PIC18F66K80	60E0	2h	3h	4h	6h
PIC18F65K80	6140				
PIC18F46K80	6100				
PIC18F45K80	6160				
PIC18F26K80	6120				
PIC18F25K80	6180				
PIC18LF66K80	61C0				
PIC18LF65K80	6220				
PIC18LF46K80	61E0				
PIC18LF45K80	6240				
PIC18LF26K80	6200				
PIC18LF25K80	6260				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of Configuration memory space. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC18FXXK80 Family Flash Microcontroller Programming Specification"* (DS39972) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A2	A3	A4	A6
Analog-to-Digital Converter (A/D)	A/D Performance	1.	The 12-bit A/D performance is outside the data sheet's A/D Converter specifications.	X	X	X	X
EUSART	Synchronous Transmit	2.	When using the Synchronous Transmit mode, transmitted data may become corrupted if using the TXxIF bit to determine when to load the TXREGx register.	X			
ECCP	Auto-Shutdown	3.	The tri-state setting of the auto-shutdown feature in the enhanced PWM will not successfully drive the pin to tri-state.	X	X	X	X
ECAN	CAN Clock Source Selection	4.	The CLKSEL bit in the CIOCON register is modifiable while the ECAN module is active.	X			
Ultra Low-Power Sleep	Sleep Entry	5.	Entering Ultra Low-Power Sleep mode by setting RETEN = 0 and SRETEN = 1, will cause the part to not be programmable through ICSP™.	X			
IPD and IDD	Maximum Limit	6.	Maximum current limits may be higher than specified in Table 31-2 of the data sheet.	X			
Reset (BOR)	Enable/Disable	7.	An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled and then re-enabled, when the High/ Low-Voltage Detection module (HLVD) is not enabled (HLVDCON<4> = 0).	X	X	X	X
ECAN	EWIN	8.	The enhanced window address feature, EWIN<4:0>, in the ECANCON register, will not move the BnCON 0≤n≤5 registers into the access window of RAM.	X			
MCLRE	Master Clear Enable	9.	The Master Clear pin will not be readable when MCLRE is set to off for all 28-pin part variants (PIC18F2XK80).	X	X	X	X
Timer1/Timer3	Gated Enable	10.	Timer1 and Timer3 gate control will not function up to the speed of FOSC when the TxCON is set to the system clock (TxCON<7:6> = 01).	X	X		
Timer1/Timer3	Interrupt	11.	When the timer is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur.	X	X	X	X
Primary Oscillator	XT Mode	12.	XT Primary Oscillator mode does not reliably function when the driving crystals are above 3 MHz.	X	X	X	
ECAN	Disable/Sleep mode	13.	Disable/Sleep mode reverts CANTX control to TRISx/LATx instead of going to Recessive state.	X	X	X	X
ECAN	CLKSEL bit	14.	Setting CLKSEL bit of CIOCON can occasionally lead to missed incoming CAN messages.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Analog-to-Digital Converter (A/D)

The 12-bit A/D performance is outside the data sheet's A/D Converter specifications. When used as a 12-bit A/D, the possible issues are: high offset error, up to a maximum of ±25 LSBs at 25°C, ±30 LSBs at 85°C, 125°C and -40°C; high DNL error, up to a maximum of +6.0/-4.0 LSBs; and multiple missing codes, up to a maximum of twenty. Users should evaluate the 12-bit A/D performance in their application using the suggested work around below. See Table 3 for guidance specifications.

The 12-bit A/D issues will be fixed in future revisions of this part. Reduced bit resolution specifications can be derived by dividing, as appropriate. For instance, 10-bit guidance is obtained by dividing the parameters in Table 3 by four.

A/D Offset

The A/D may have high offset error, up to a maximum of ±25 LSBs; it can be used if the A/D is calibrated for the offset.

Work around

Calibrate for offset in Single-Ended mode by connecting A/D +ve input to ground and taking the A/D reading. This will be the offset of the device and can be used to compensate for the subsequent A/D readings on the actual inputs.

TABLE 3: A/D CONVERTER CHARACTERISTICS

Param No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
A01	NR	Resolution	—	—	12	bit	ΔVREF ≥ 5.0V
A03	EIL	Integral Linearity Error	—	—	±10.0	LSb	ΔVREF ≥ 5.0V
A04	EDL	Differential Linearity Error	—	—	+6.0/-4.0	LSb	ΔVREF ≥ 5.0V
A06	EOFF	Offset Error	—	—	±25 ±30	LSb	ΔVREF ≥ 5.0V, TEMP = 25°C TEMP ≥ 85°C, -40°C
A07	EGN	Gain Error	—	—	±15	LSb	ΔVREF ≥ 5.0V
A10	—	Monotonicity(1)	—				VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	AVDD – AVSS	V	
A21	VREFH	Reference Voltage High	AVSS + 3.0V	—	AVDD + 0.3V	V	
A22	VREFL	Reference Voltage Low	AVSS – 0.3V	—	AVDD – 3.0V	V	
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

2. Module: EUSART

In Synchronous Transmit mode, data may be corrupted if using the TXxIF bit to determine when to load the TXREGx register. One or more of the intended transmit messages may be incorrect.

Work around

A fixed delay added before loading TXREGx may not be a reliable work around. When loading the TXREGx, check that the TRMT bit inside of the TXSTAx register is set instead of checking the TXxIF bit. The following code can be used:

```
while(!TXSTAxbits.TRMT);
// wait to load TXREGx until TRMT is set
```

Affected Silicon Revisions

A2	A3	A4	A6				
X							

3. Module: ECCP

The tri-state setting of the auto-shutdown feature, in the enhanced PWM will not successfully drive the pin to tri-state. The pin will remain an output and should not be driven externally. All tri-state settings will be affected.

Work around

Use one of the other two auto-shutdown states available, as outlined in the data sheet.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

4. Module: ECAN

The CLKSEL bit in the CIOCON register remains modifiable while the ECAN module is not in Configuration mode. Accidental state changes of this bit will result in immediate bit clock changes that will affect all nodes on the bus.

Work around

While the ECAN module is in Run mode, do not modify the state of the CLKSEL bit in the CIOCON register unless the CAN module is first changed into Configuration mode.

Affected Silicon Revisions

A2	A3	A4	A6				
X							

5. Module: Ultra Low-Power Sleep

Entering Ultra Low-Power Sleep mode by setting $\overline{\text{RETEN}}$ = 0 and SRETEN = 1 will cause the part to not be programmable through ICSP™. This issue occurs when the $\overline{\text{RETEN}}$ fuse bit in CONFIG1L<0> is cleared to '0', the SRETEN bit in the WDTCON register is set to '1' and a SLEEP instruction is executed within the first 350 µs of code execution. This happens after a Reset event, causing the part to enter Ultra Low-Power Sleep mode.

Work around

Use Normal Sleep and Low-Power Sleep modes only, or on any Reset, ensure that at least 350 µs pass before executing a SLEEP instruction when ULP is enabled. To ensure the Ultra Low-Power Sleep mode is not enabled, the $\overline{\text{RETEN}}$ fuse bit in CONFIG1L<0> should be set to a '1' and the SRETEN bit in the WDTCON register should be cleared to a '0'. The following code can be used:

```
//This will ensure the RETEN fuse is set to 1
#pragma config RETEN = OFF
//This will ensure the SRETEN bit is 0
WDTCONbits.SRETEN = 0;
```

If the Ultra Low-Power Sleep mode is needed, then the user must ensure that the minimum time, before the first SLEEP instruction is executed, is greater than 350 µs.

Affected Silicon Revisions

A2	A3	A4	A6				
X							

6. Module: IPD and IDD

The IPD and IDD limits do not match the data sheet. The IPD values, shown in **bold** in **Section 31.2 "DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/ Extended)"** (below), reflect the updated silicon maximum limits.

All IDD maximum limits will equal 2.8 times the value listed in the data sheet.

Affected Silicon Revisions

A2	A3	A4	A6				
X							

31.2 DC Characteristics: Power-Down and Supply Current PIC18F66K80 Family (Industrial/Extended)

PIC18F66K80 (Industrial/Extended)		Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	**Device**	**Typ.**	**Max.**	**Units**	**Conditions**	
	Power-Down Current (IPD)(1)					
	PIC18LFXXK80	0.008	**7**	µA	-40°C	VDD = 1.8V(4) (Sleep mode) Regulator Disabled
		0.013	**7**	µA	+25°C	
		0.035	**9**	µA	+60°C	
		0.218	**10**	µA	+85°C	
		3	**12**	µA	±125ºC	
	PIC18LFXXK80	0.014	**8**	µA	-40°C	VDD = 3.3V(4) (Sleep mode) Regulator Disabled
		0.034	**8**	µA	+25°C	
		0.092	**9**	µA	+60°C	
		0.312	**10**	µA	+85°C	
		4	**16**	µA	±125ºC	
	PIC18FXXK80	0.2	**9**	µA	-40°C	VDD = 3.3V (Sleep mode) Regulator Enabled
		0.23	**9**	µA	+25°C	
		0.32	**10**	µA	+60°C	
		0.51	**11**	µA	+85°C	
		5	**18**	µA	±125ºC	
	PIC18FXXK80	0.22	**10**	µA	-40°C	VDD = 5V(5) (Sleep mode) Regulator Enabled
		0.24	**10**	µA	+25°C	
		0.34	**11**	µA	+60°C	
		0.54	**12**	µA	+85°C	
		5	**20**	µA	±125ºC	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS, and all features that add delta current disabled (such as WDT, SOSC oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

3: Standard, low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

4: For LF devices, RETEN (CONFIG1L<0>) = 1.

5: For F devices, SRETEN (WDTCON<4>) = 1 and $\overline{\text{RETEN}}$ (CONFIG1L<0>) = 0.

7. Module: Reset (BOR)

An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled, when the High/Low-Voltage Detection module (HLVD) is not enabled (HLVDCON<4> = 0). This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the HLVD (HLVDCON<4> = 1) prior to entering Sleep. If power consumption is an issue and low power is desired, do not use BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN (RCON<6> = 0).
   ```
   WDTCONbits.SBOREN = 0;
   ```
2. Enter Sleep mode (if desired).
   ```
   Sleep();
   ```
3. After exiting Sleep mode (if entered), enable the HLVD bit (HLVDCON<4> = 1).
   ```
   HLVDCONbits.HLVDEN = 1;
   ```
4. Wait for the internal reference voltage (TIRVST) to stabilize (typically 25 μs).
   ```
   while(!HLVDCONbits.IRVST);
   ```
5. Re-enable BOR by setting SBOREN (RCON<6> = 1).
   ```
   WDTCONbits.SBOREN = 1;
   ```
6. Disable the HLVD by clearing HLVDEN (HLVDCON<4> = 0).
   ```
   HLVDCONbits.HLVDEN = 0;
   ```

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

8. Module: ECAN

The enhanced window address feature, EWIN<4:0>, in the ECANCON register, will not move the BnCON 0≤n≤5 registers into the access window of RAM. The rest of the registers in B0 through B5 will be transferred into the access bank successfully. This feature is only available in Mode 1 and Mode 2; Mode 0 applications will not be affected.

Work around

1. Set the ECANCON register EWIN bits to the desired buffer.
   ```
   ECANCONbits.EWIN = Buffer_Selection;
   ```
2. Decode the desired buffer to each individual Buffer Control register, BnCON 0≤n≤5.
   ```
   switch (Buffer_Selection)
   {
   //EWIN code for Buffer B0
   case 18:
         break;

   //EWIN code for Buffer B5
   case 23:
         break;
   default:
         break;
   }
   ```
3. Process information in the selected buffer control register. Note that the BnCON 0≤n≤5 Control registers can be set up for either transmit or receive operations.
   ```
   case 18:
         //Save B0CON and clear flags
   being processed
         temp = B0CON;
         //clear any flags
         break;
   ```
4. Continue processing the rest of the buffer in the windowed location.

Affected Silicon Revisions

A2	A3	A4	A6				
X							

9. Module: MCLRE

The Master Clear pin will not be readable when MCLRE is set to off for all 28-pin part variants (PIC18F2XK80). When the MCLRE bit, CONFIG3H<7>, is cleared on the 28-pin devices, the $\overline{MCLR}$ pin will be disabled but input data will not be available on RE3.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

10. Module: Timer1/Timer3

Timer1 and Timer3 gate control will not function up to the speed of FOSC when the TxCON is set to the system clock (TxCON<7:6> = 01). Results will always be at the resolution of FOSC/4, although the internal FOSC has been selected as the clock source.

Work around

Use the external clock input pin setting, TxCON<7:6> = 10 and TxCON<3> = 0.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X						

11. Module: Timer1/Timer3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the Timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to 0x0000 when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 1.

EXAMPLE 1: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2T_CY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for timer 1
```

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

12. Module: Primary Oscillator (XT Mode)

On some parts, using the XT oscillator at the top end of its specified frequency range (3.0-4.0 MHz) may cause the part to cease driving the oscillator.

Work around

Use the XT mode only for frequencies lower than 3.0 MHz.

Use the HS mode if frequencies greater than 4.0 MHz on a crystal oscillator are required.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X					

13. Module: ECAN

When the ECAN module is placed into Disable/ Sleep mode, the CANTX pin will revert to being controlled by the PORTx/TRISx/LATx registers, instead of staying in the recessive state as intended.

Work around

If Disable/Sleep mode of the ECAN is to be used, set the TRIS bit associated with the TX pin (either TRISB2 if the CANMX Configuration bit is set, TRISC6 if the CANMX Configuration bit is cleared on the 28-pin and 40/44-pin packages, or TRISE4 if the CANMX Configuration bit is cleared on 64-pin packages) and ensure that the CANTX line has a proper pull up to V_{DD}. This will ensure that, when the pin is controlled by TRIS/LAT settings, it will be pulled to the CAN Recessive state and not cause issues on the CAN bus.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

14. Module: ECAN

A very small number of CAN applications are experiencing a low-failure rate when the microcontroller core is clocked by an oscillator through a PLL (either the PLLCFG bit is cleared or the PLLEN bit of OSCTUNE is set) and the ECAN module is clocked by the same clock without a PLL (the CLKSEL bit of CIOCON is set). This failure mechanism is characterized by incoming CAN messages rarely being missed, with the ECAN module acknowledging the incoming message on the bus but not triggering interrupts or transferring the incoming data into the receive buffers.

Work around

If it is essential that the application never misses a message, it is recommended that both the ECAN module and the microcontroller be clocked either through the PLL or without a PLL. This can be achieved by ensuring that the CLKSEL bit of CIOCON remains cleared.

Affected Silicon Revisions

A2	A3	A4	A6				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39977**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: A/D Converter Characteristics

The values in Table 31-25 reflect the updated A/D Converter Characteristics. The new information is shown in **bold** text.

TABLE 31-25: A/D CONVERTER CHARACTERISTICS: PIC18F66K80 FAMILY (INDUSTRIAL/EXTENDED)

Param No.	Sym.	Characteristic	Min.	Typ.	Max.	Units	Conditions
A01	NR	Resolution	—	—	12	bit	**ΔVREF ≥ 5.0V**
A03	EIL	Integral Linearity Error	—	<±1	±6.0	LSB	**ΔVREF ≥ 5.0V**
A04	EDL	Differential Linearity Error	—	<±1	+3.0/-1.0	LSB	**ΔVREF ≥ 5.0V**
A06	EOFF	Offset Error	—	<±1	±9.0	LSB	**ΔVREF ≥ 5.0V**
A07	EGN	Gain Error	—	<±1	±8.0	LSB	**ΔVREF ≥ 5.0V**
A10	—	Monotonicity(1)	**—**			—	VSS ≤ VAIN ≤ VREF
A20	ΔVREF	Reference Voltage Range (VREFH – VREFL)	3	—	VDD – VSS	V	For 12-bit resolution
A21	VREFH	Reference Voltage High	AVSS + 3.0V	—	AVDD + 0.3V	V	For 12-bit resolution
A22	VREFL	Reference Voltage Low	AVSS – 0.3V	—	AVDD – 3.0V	V	For 12-bit resolution
A25	VAIN	Analog Input Voltage	VREFL	—	VREFH	V	
A28	AVDD	Analog Supply Voltage	VDD – 0.3	—	VDD + 0.3	V	
A29	AVSS	Analog Supply Voltage	VSS – 0.3	—	VSS + 0.3	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	2.5	kΩ	
A50	IREF	VREF Input Current(2)	— —	— —	5 150	μA μA	During VAIN acquisition. During A/D conversion cycle.

Note 1: The A/D conversion result never decreases with an increase in the input voltage.

2: VREFH current is from the RA3/AN3/VREF+ pin or VDD, whichever is selected as the VREFH source. VREFL current is from the RA2/AN2/VREF-/CVREF pin or VSS, whichever is selected as the VREFL source.

2. Module: Electrical Characteristics

Parameter **D041** in **Section 31.3 "DC Characteristics: PIC18F66K80 Family (Industrial)"** on page 555 of the data sheet lists its minimum value as 0.8. This should be 0.8 **VDD**.

3. Module: A/D Converter

Bits 5-4 of Register 23-2: ADCON1 (VCFG<1:0>) should have the following note attached:

Note 1: When CHS<4:0> = 11111, a VCFG<1:0> value of 10 or 11 is not allowed.

4. Module: I/O Ports

4.1 Open-Drain Outputs Description

Page 173 **Section 11.1.3 'Open-Drain Outputs'** will be revised to:

The output pins for several peripherals are also equipped with a configurable, open-drain output option. **This allows the peripherals to communicate with external pull-up voltage**.

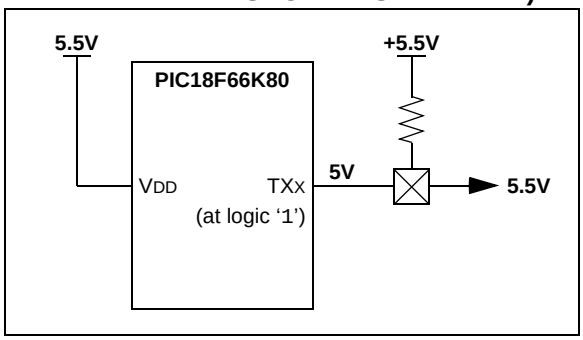
The open-drain option is implemented on port pins specifically associated with the data and clock outputs of the USARTs, the MSSP module (in SPI mode) and the CCP modules. This option is selectively enabled by setting the open-drain control bits in the ODCON register.

When the open-drain option is required, the output pin must also be tied through an external pull-up resistor provided by the user.

4.2 Open-Drain Outputs Diagram

Figure 11-2: **Using the Open-Drain Output (Usart Shown as Example)** on page 173 should be as follows:

FIGURE 11-2: USING THE OPEN-DRAIN OUTPUT (USARTx SHOWN AS EXAMPLE)



5. Module: A/D Converter

Bits 2-0 of Register 23-2 ADCON1 (CHSN<2:0>) should be as follows:

REGISTER 23-2: ADCON1: A/D CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-x	R/W-x	R/W-x	R/W-x
TRIGSEL1	TRIGSEL0	VCFG1	VCFG0	VNCFG	CHSN2	CHSN1	CHSN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **TRIGSEL<1:0>:** Special Trigger Select bits
11 = Selects the special trigger from the CCP2
10 = Selects the special trigger from the Timer1
01 = Selects the special trigger from the CTMU
00 = Selects the special trigger from the ECCP1

bit 5-4 **VCFG<1:0>:** A/D V_{REF}+ Configuration bits
11 = Internal V_{REF}+ (4.1V)
10 = Internal V_{REF}+ (2.0V)
01 = External V_{REF}+
00 = AV_{DD}

bit 3 **VNCFG:** A/D V_{REF}- Configuration bit
1 = External V_{REF}
0 = AV_{SS}

bit 2-0 **CHSN<2:0>:** Analog Negative Channel Select bits
111 = **Reserved**
110 = Channel 06 (AN5)
101 = Channel 05 (AN4)
100 = Channel 04 (AN3)
011 = Channel 03 (AN2)
010 = Channel 02 (AN1)
001 = Channel 01 (AN0)
000 = Channel 00 (AV_{SS})

6. Module: ECCP Compare Mode

The following text should be added to the Compare Mode section of the data sheet.

19.3.5 COMPARE MODE INTERRUPT TIMING

For all Compare modes, an interrupt may be triggered when the selected TIMER register pair matches the value in the CCPRx register pair. This interrupt will be triggered upon the timer transitioning from the value of the CCPRx register pair to the next value.

7. Module: Product Identification System

The Product Identification System is missing a few package type codes. The correct list is as follows:

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device[1,2]	PIC18F65K80, PIC18F46K80, PIC18F45K80, PIC18F26K80, PIC18F25K80, PIC18LF66K80 VDD range 1.8V to 5V PIC18LF25K80, PIC18LF26K80, PIC18LF45K80, PIC18LF46K80, PIC18F25K80, PIC18LF66K80 VDD range 1.8V to 3.6V	
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)	
Package	P = PDIP Plastic Dual In-Line **MR = 64-Pin QFN Plastic Quad Flat, No Lead Package** ML = 44-Pin QFN Plastic Quad Flat, No Lead Package **MM = 28-Pin QFN Plastic Quad Flat, No Lead Package** SO = SOIC Plastic Small Outline SP = SPDIP Skinny Plastic Dual In-Line SS = SSOP Plastic Shrink Small Outline PT = TQFP Plastic Thin Quad Flatpack	
Pattern	a) QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC18LF66K80-I/MR 301 = Industrial temp., QFN package, Extended VDD limits, QTP pattern #301.

b) PIC18LF66K80-I/PT = Industrial temp., TQFP package, Extended VDD limits.

Note 1: F = Standard Voltage Range
LF = Low Voltage Range
2: T = in tape and reel, TQFP packages only.

8. Module: ECAN

In Register 27-55, CIOCON: CAN I/O Control Register, Bit 4 has an incorrect description for its settings. The correct description is as follows:

bit 4	**CANCAP**: CAN Message Receive Capture Enable bit 1 = Enable CAN capture; CAN message receive signal replaces input in RC2/**CCP2** 0 = Disable CAN capture; RC2/**CCP2** input to **CPP2** module

9. Module: Power-Managed Modes

In Table 4-1: Power-Managed Modes, the column “IDLEN<7>” under “OSCCON Bits” should instead read ‘IDLEN”.

10. Module: DC Characteristics (Comparator Specifics)

Parameter D303, Comparator Response Time is incorrect. The correct specifications are as follows:

TABLE 31-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 1.8V ≤ VDD ≤ 5.5V, -40°C ≤ TA ≤ +125°C							
Param. No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	40	mV	
D301	VICM	Input Common Mode Voltage	—	—	AVDD	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time(1)	—	**675**	**1200**	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid*	—	—	10	µs	

Note 1: Response time is measured with one comparator input at (AVDD – 1.5)/2, while the other input transitions from VSS to VDD.

11. Module: A/D Converter

Adding Note 4 for acquisition time requirements when measuring the FVR. The new text is highlighted in bold.

REGISTER 31-3: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CHS4	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **CHS<4:0>:** Analog Channel Select bits

00000 = Channel 00 (AN0)	10000 = (Reserved)(2)
00001 = Channel 01 (AN1)	10001 = (Reserved)(2)
00010 = Channel 02 (AN2)	10010 = (Reserved)(2)
00011 = Channel 03 (AN3)	10011 = (Reserved)(2)
00100 = Channel 04 (AN4)	10100 = (Reserved)(2)
00101 = Channel 05 (AN5)(1,2)	10101 = (Reserved)(2)
00110 = Channel 06 (AN6)(1,2)	10110 = (Reserved)(2)
00111 = Channel 07 (AN7)(1,2)	10111 = (Reserved)(2)
01000 = Channel 08 (AN8)	11000 = (Reserved)(2)
01001 = Channel 09 (AN9)	11001 = (Reserved)(2)
01010 = Channel 10 (AN10)	11010 = (Reserved)(2)
01011 = (Reserved)(2)	11011 = (Reserved)(2)
01100 = (Reserved)(2))	11100 = (MUX disconnect)(3)
01101 = (Reserved)(2))	11101 = Channel 29 (temperature diode)
01110 = (Reserved)(2))	11110 = Channel 30 (V_{DDCORE})
01111 = (Reserved)(2)	11111 = Channel 31 (1.024V band gap)(4)

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit

1 = A/D cycle is in progress. Setting this bit starts an A/D conversion cycle. The bit is cleared automatically by hardware when the A/D conversion is completed.

0 = A/D conversion has completed or is not in progress

bit 0 **ADON:** A/D On bit

1 = A/D Converter is operating

0 = A/D conversion module is shut off and consuming no operating current

Note 1: These channels are not implemented on 28-pin devices.

2: Performing a conversion on unimplemented channels will return random values.

3: Channel 28 turns off analog MUX switches to allow for minimum capacitive loading of the A/D input, for finer resolution CTMU time measurements.

4: Allow greater than 15 µs acquisition time when measuring the Fixed Voltage Reference.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2011)

Initial release of this document; issued for revision, A2. Includes silicon issues 1 (Analog-to-Digital Converter), 2 (EUSART), 3 (ECCP), 4 (ECAN), 5 (Ultra Low-Power Sleep) and 6 (I_{PD} and I_{DD}).

Rev B Document (4/2011)

Added silicon issues 7 (Reset – BOR) and 8 (ECAN). Added data sheet clarifications 1, 2 (RXFCON Registers) and 3 (Listen Only Mode).

Rev C Document (9/2011)

Added Table 3, 10-Bit A/D Converter Characteristics to silicon issue 1 (Analog-to-Digital Converter). Added silicon issues 9 (MCLRE) and 10 (Timer1/Timer3). Added data sheet clarifications 4 (A/D Converter Characteristics) and 5 (HLVD).

Rev D Document (12/2011)

Added silicon revision A4; includes issues 1 (Analog-to-Digital Converter – A/D), 3 (ECCP), 7 (Reset – BOR) issues 9 (MCLRE). Added data sheet clarification 6 (Power-up Timer Period).

Updated data sheet revision level to “D”. All previous clarifications carried into this revision.

Rev E Document (12/2013)

Added MPLAB X IDE; Updated silicon issue 1 (Analog-to-Digital Converter); Added silicon issue 11 (Primary Oscillator); Other minor corrections;

Data Sheet Clarifications: Added Module 7 (Electrical Characteristics) and Module 8 (A/D Converter).

Rev F Document (2/2014)

Added Silicon Revision A6; Data Sheet Clarification: Added Module 9 and 10; Other minor corrections.

Rev G Document (4/2014)

Data Sheet Clarifications: Added Module 11; Other minor corrections.

Rev H Document (7/2014)

Added Module 11, Timer1/Timer3 to Silicon errata Issues section.

Rev J Document (7/2015)

Data Sheet Clarifications:
Removed the following modules, data sheet has been updated: Module 1: RXFCON Registers; Module 2: RXFCON Registers; Module 3: Listen Only Mode; Module 5: HLVD; Module 6: Power-up Timer Period. Renumbered remaining modules.

Rev K Document (04/2016)

Added Silicon Errata Issues 13 and 14. Other minor corrections.

Data Sheet Clarifications: Added Module 9 (ECAN) and Module 10 (Power-Managed Modes).

Rev L Document (01/2017)

Data Sheet Clarifications: Added Module 11 (DC Characteristics); Other minor corrections.

Rev M Document (7/2017)

Data Sheet Clarifications: Added Module 11 (A/D Converter).

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