One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD7606C-18 and AD7606C-16 8-Channel DASs with 18-Bit/16-Bit, 1 MSPS Bipolar Input, Simultaneous Sampling ADCs

FEATURES

- Fully featured evaluation board for the AD7606C-18 and the AD7606C-16
- On-board power supplies
- Standalone capability
- SDP-H1 compatible
- PC software for control and data analysis
- Time and frequency domain

EVALUATION KIT CONTENTS

EVAL-AD7606C18FMCZ or EVAL-AD7606C16FMCZ

ADDITIONAL EQUIPMENT NEEDED

- EVAL-SDP-CH1Z (SDP-H1) high speed controller board
- PC running Windows Vista SP2 (32-bit or 64-bit), Windows 7 SP1 (32-bit or 64-bit), Windows 8.1 (32-bit or 64-bit), or Windows 10 (32-bit or 64-bit) with a USB 2.0 port
- DC and ac signal source
- SMB and USB cables
- External supply (optional)

DOCUMENTS NEEDED

AD7606C-18 or AD7606C-16 data sheet

ONLINE RESOURCES

- ACE software
- AD7606C-18 or AD7606C-16 ACE plugin (provided in ACE)
- AD7606x Family Software Model

EVALUATION BOARD DESCRIPTION

The EVAL-AD7606CFMCZ is a fully featured evaluation board that allows users to evaluate the features of the AD7606C-18 and AD7606C-16 analog-to-digital converters (ADCs). The EVAL-AD7606CFMCZ is controlled by the EVAL-SDP-CH1Z (SDP-H1) system demonstration platform (SDP). The SDP-H1 controls the EVAL-AD7606CFMCZ through the USB port of a PC using the Analysis | Control | Evaluation (ACE) software, which is available to download from the ACE software page or the AD7606C-18 or the AD7606C-16 product page.

The on-board components include the ADP7118 5 V and 3.3 V low noise, low dropout (LDO) linear regulators and an ADR4525 high precision, band gap voltage reference.

Figure 1 shows the evaluation board photograph. The printed model number on the evaluation board is EVAL-AD7606CFMCZ.

For full details on the AD7606C-18 and the AD7606C-16, see the AD7606C-18 and AD7606C-16 data sheets, which must be consulted in conjunction with this user guide when using the EVAL-AD7606CFMCZ. In addition, full details on the SDP-H1 are available on the SDP-H1 product page.

Throughout this user guide, the EVAL-AD7606CFMCZ refers to either the EVAL-AD7606C18FMCZ or the EVAL-AD7606C16FMCZ.

EVALUATION BOARD PHOTOGRAPH

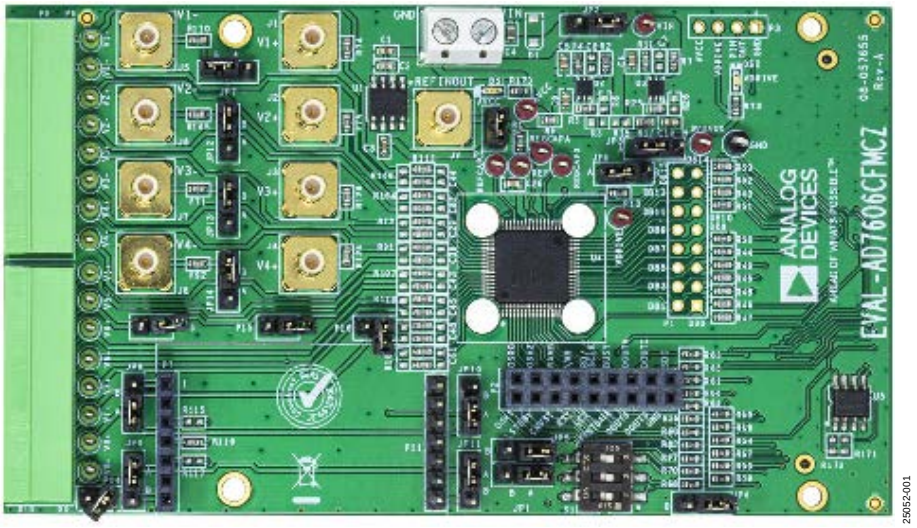


Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

1/2021—Rev. 0 to Rev. A

Added AD7606C-16 ... Universal
Added EVAL-AD7606C16FMCZ ... Universal
Changed EVAL-AD7606C18FMCZ to EVAL-AD7606CFMCZ ... Throughout
Changes to User Guide Title ... 1
Change to ACE Software Operation Section ... 10
Change to Description of Analysis Window Section ... 13

10/2020—Revision 0: Initial Version

EVALUATION BOARD QUICK START GUIDE

To quickly evaluate the AD7606C-18 and AD7606C-16 ADCs, take the following steps:

1. Download and install the ACE software from the AD7606C-18 or AD7606C-16 product page or the ACE software page. When installing the ACE software, ensure that the SDP-H1 is disconnected from the USB port of the PC. Restart the PC after the installation process completes. For complete software installation instructions, see the Software Installation section.
2. Ensure that the link options are configured as detailed in Table 2.
3. Connect the SDP-H1 to the EVAL-AD7606CFMCZ. By default, the power for the EVAL-AD7606CFMCZ is supplied by the SDP-H1. See the Power Supplies section for the available power options.
4. Connect the SDP-H1 to the 12 V supply (included in the SDP-H1 kit) and to the PC via the USB cable. If prompted by the operating system, choose to automatically search for the drivers for the SDP-H1.
5. Launch the ACE software from the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
6. Connect an input signal via the Channel 1 to Channel 8 terminal blocks or the Subminiature Version B (SMB) connectors, J1 to J8.

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The 18-bit AD7606C-18 and the 16-bit AD7606C-16 are 8-channel, simultaneous sampling, successive approximation register (SAR) ADCs. The devices operate from a single 4.75 V to 5.25 V power supply and feature throughput rates of up to 1 MSPS. The devices have 1 MΩ input impedance for direct connection from the user sensor outputs to the ADC.

HARDWARE LINK OPTIONS

Table 2 details the link option functions and the default power link options. The EVAL-AD7606CFMCZ can be powered by different sources, as described in the Power Supplies section. By default, the power supply required for the EVAL-AD7606CFMCZ comes from the SDP-H1. The power supply is regulated by the on-board ADP7118 LDO linear regulators, which generate the 5 V and 3.3 V supplies.

CONNECTORS AND SOCKETS

The connectors and sockets on the EVAL-AD7606CFMCZ are detailed in Table 1.

Table 1. On-Board Connectors

Connector	Function
J1 to J8	Analog input SMB connectors to Channel 1 through Channel 8
J9	Analog input SMB connector to external reference
P1, P2, P3	General connectors for debugging purposes or to connect an external controller
P4	External power terminal block, 7 V to 9 V dc input
P5	External reference connection
P6, P8	8-pin connectors for input to Channel 1 through Channel 4
P7, P11	Channel 8 surfboard evaluation headers
P9, P10	8-pin connectors for input to Channel 5 through Channel 8
P12	FMC connector

The default interface to the EVAL-AD7606CFMCZ is achieved via the field programmable gate array (FPGA) mezzanine card (FMC) connector, which connects the EVAL-AD7606CFMCZ to the SDP-H1.

POWER SUPPLIES

Before applying power and signals to the EVAL-AD7606CFMCZ, ensure that all link positions are set according to the required operating mode. See Table 2 for the complete list of link options.

The supply required for the EVAL-AD7606CFMCZ comes from the SDP-H1. Alternatively, the EVAL-AD7606CFMCZ can also be supplied with a dc power supply connected to the P4 terminal block. Select the external power supply or the SDP-H1 supply through JP2. The power supply is then connected to the on-board ADP7118 5 V and 3.3 V LDO linear regulators that supply the proper bias to each of the various sections on the EVAL-AD7606CFMCZ.

CHANNEL INPUT

The J1 to J8 connectors allow the user to connect external signals to the ADC channel inputs through the SMB inputs. The EVAL-AD7606CFMCZ is supplied with the AD7606C-18 or AD7606C-16 mounted (U4, see Figure 1). The AD7606C-18 and the AD7606C-16 are 8-channel data acquisition systems (DASs) with simultaneous sampling ADCs. External signals can be applied to the P6, P8, P9, and P10 connectors on the EVAL-AD7606CFMCZ.

Table 2. Link Options

Link	Default Position	Function
JP1	A	The ACE software controls the $\overline{\text{STBY}}$ pin. When using the EVAL-AD7606CFMCZ in standalone mode without running the ACE software, JP1 allows the selection of standby mode. In this case, change the R8 and R10 resistors to 0 Ω links. In Position A, the $\overline{\text{STBY}}$ pin is tied to V_{DRIVE}. In Position B, the $\overline{\text{STBY}}$ pin is tied to AGND.
JP2	A	JP2 selects the power supply source for the EVAL-AD7606CFMCZ. In Position A, the unregulated supply to the on-board LDOs is taken from the SDP-H1 12 V supply. In Position B, the unregulated external supply to the on-board LDOs is taken from the P4 terminal block connector.

Link	Default Position	Function
JP3	A	Use JP3 to select the V_{DRIVE} source for the AD7606C-18 and the AD7606C-16. In Position A, the AD7606C-18 or the AD7606C-16 is supplied with 3.3 V from the ADP7118. In Position B, the AD7606C-18 or the AD7606C-16 is supplied with 3.3 V from the SDP-H1.
JP4	A	The ACE software controls the RANGE pin. If using the EVAL-AD7606CFMCZ in standalone mode, JP4 allows the selection of the analog input range in hardware mode. In this case, change the R20 resistor to a 0 Ω link. In Position A, the RANGE pin is tied to V_{DRIVE}, and the ±10 V range is selected. In Position B, the RANGE pin is tied to AGND, and the ±5 V range is selected. In software mode, the RANGE pin is ignored.
JP5	A	The ACE software controls the $\overline{PAR}$/SER SEL pin. If using the EVAL-AD7606CFMCZ in standalone mode, JP5 allows the selection of the digital interface. In this case, change the R19 and R21 resistors to 0 Ω links In Position A, the $\overline{PAR}$/SER SEL pin is tied to V_{DRIVE}, and the serial interface is selected. In Position B, the $\overline{PAR}$/SER SEL pin is tied to AGND, and the parallel interface is selected.
JP6	A	The ACE software controls the REF SELECT pin. By default, the internal reference is selected. If switching to the external reference is required through the ACE software, P5 must be inserted. If using the EVAL-AD7606CFMCZ in standalone mode, JP6 allows the selection of the reference. In this case, change the R13 resistor to a 0 Ω link. In Position A, the REF SELECT pin is tied to V_{DRIVE}, and the internal reference is enabled and selected. P5 must be unpopulated. In Position B, the REF SELECT pin is tied to AGND, the internal reference is disabled, and the external reference is selected. P5 must be inserted if using the on-board U1 devices, and must not be inserted if using the J9 SMB connector.
JP7	B	JP7 selects the V1− line to be connected to ground (single-ended operation) or to the SMB connector (differential operation). Position A connects the V1− line to ground for single-ended operation. Position B connects the V1− line to the J5 SMB connector and disconnects the V1− line from ground.
JP8, JP10	A	Position A bypasses the amplifier mezzanine card (AMC). Position B enables the AMC to be connected on the P7 and P11 headers.
JP9, JP11	A	Position A bypasses the AMC. Position B enables the AMC to be connected on the P7 and P11 headers.
JP12	B	JP12 selects the V2− line to be connected to ground (single-ended operation) or to the SMB connector (differential operation). Position A connects the V2− line to ground for single-ended operation. Position B connects the V2− line to the J6 SMB connector and disconnects the V2− line from ground.
JP13	B	JP13 selects the V3− line to be connected to ground (single-ended operation) or to the SMB connector (differential operation). Position A connects the V3− line to ground for single-ended operation. Position B connects the V3− line to the J7 SMB connector and disconnects the V3− line from ground.
JP14	B	JP14 selects the V4− line to be connected to ground (single-ended operation) or to the SMB connector (differential operation). Position A connects the V4− line to ground for single-ended operation. Position B connects the V4− line to the J8 SMB connector and disconnects the V4− line from ground.
P13	Not inserted	Inserting P13 connects the V5− line to ground.
P14	Not inserted	Inserting P14 connects the V8− line to ground.
P15	Not inserted	Inserting P15 connects the V6− line to ground.
P16	Not inserted	Inserting P16 connects the V7− line to ground.
S1	Open	The ACE software controls the OS0, OS1, and OS2 pins. If using the EVAL-AD7606CFMCZ in standalone mode, these switches select the logic level on the OS0, OS1, and OS2 pins.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

Download the ACE software from the ACE software page or the AD7606C-18 or AD7606C-16 product page. Both the ACE software and the SDP-H1 board drivers must be installed.

Warning

The ACE software and SDP-H1 drivers must be installed before connecting the EVAL-AD7606CFMCZ and the SDP-H1 to the USB port of the PC to ensure that the evaluation system is properly recognized when it is connected to the PC.

Installing the ACE Software

To install the ACE software, take the following steps:

1. Download the ACE software to a Windows® based PC.
2. Double click the **ACEInstall.exe** file to begin the installation. By default, the software is saved to the following location: **C:\Program Files (x86)\Analog Devices\ACE**.
3. A dialog box opens asking for permission to allow the program to make changes to the PC. Click **Yes** to begin the installation process.
4. In the **ACE Setup** window, click **Next >** to continue the installation (see Figure 2).

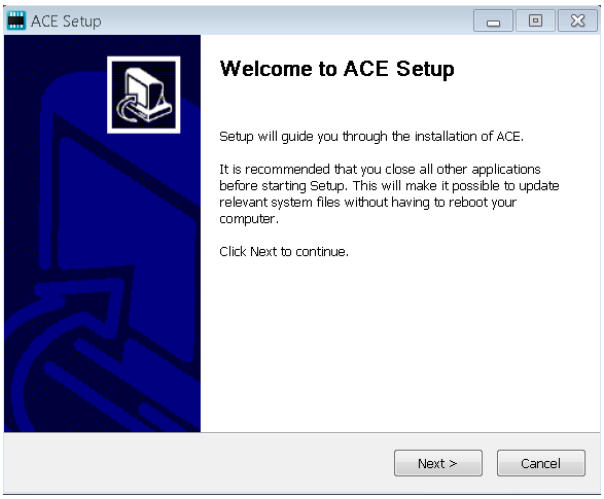


Figure 2. ACE Software Installation Confirmation

5. Read the software license agreement and click **I Agree** (see Figure 3).

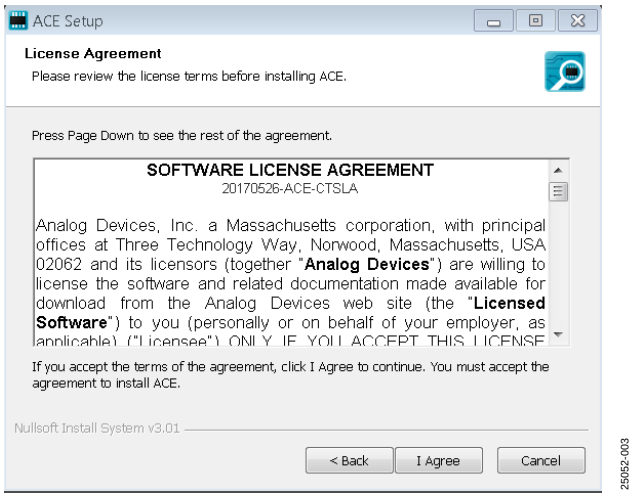


Figure 3. License Agreement

6. Click **Browse…** to choose the installation location and then click **Next >** (see Figure 4).

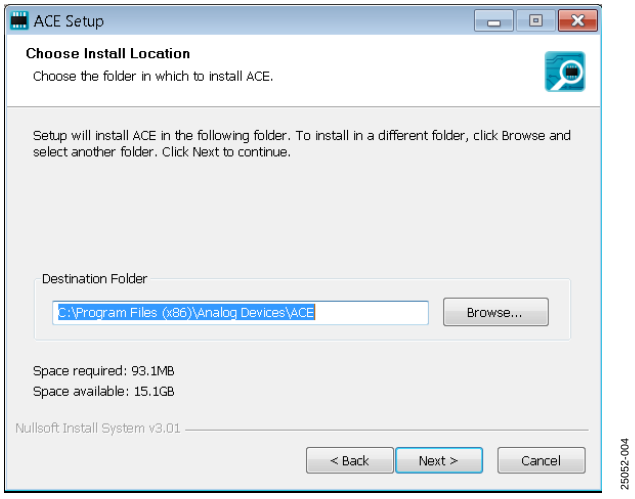


Figure 4. Choose Installation Location

7. The ACE software components to install are preselected (see Figure 5). Click **Install.**

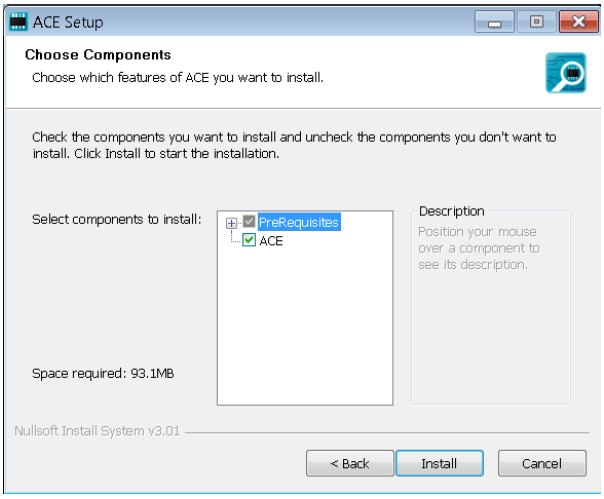


Figure 5. Choose Components

8. The **Windows Security** window opens (see Figure 6). Click **Install**. Figure 7 shows the installation in progress. No action is required.

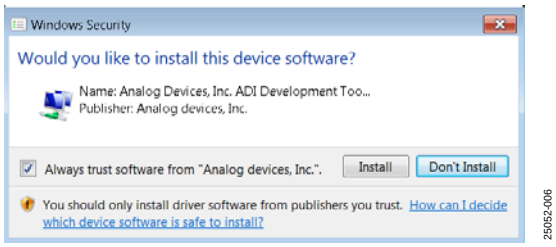


*Figure 6. **Windows Security** Window*

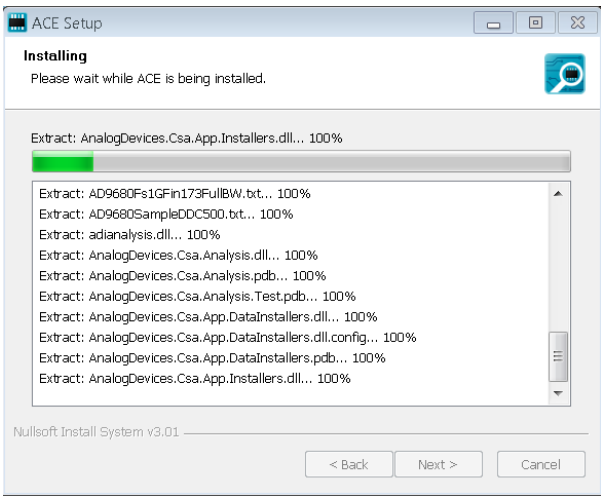


Figure 7. Installation in Progress

9. When the installation is complete, click **Next >** (see Figure 8), and then click **Finish** to complete the installation process.

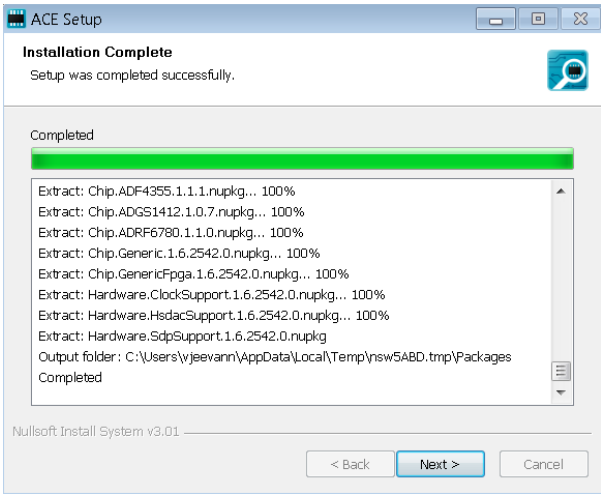


Figure 8. Installation Complete

EVALUATION BOARD SETUP PROCEDURES

The EVAL-AD7606CFMCZ connects to the SDP-H1. The SDP-H1 is the communication link between the PC and the EVAL-AD7606CFMCZ.

Connecting the EVAL-AD7606CFMCZ and the SDP-H1 to a PC

After the ACE software is installed, take the following steps to set up the EVAL-AD7606CFMCZ and the SDP-H1:

1. Ensure that all configuration links are in the appropriate positions, as detailed in Table 2.
2. Connect the EVAL-AD7606CFMCZ to the 160-way connector on the SDP-H1. The EVAL-AD7606CFMCZ does not require an external power supply adapter.
3. To power up the SDP-H1, insert the 12 V, dc barrel jack (provided in the SDP-H1 kit) into the barrel connector labeled +12V_VIN on the SDP-H1.
4. Connect the SDP-H1 to the PC via the USB cable included in the SDP-H1 kit.

Verifying the Board Connection

After connecting the power and the USB cable from the SDP-H1 to the PC, take the following steps to verify the SDP-H1 connection:

1. After connecting the SDP-H1 to the PC, allow the **Found New Hardware Wizard** to run. Choose to automatically search for the drivers for the SDP-H1 if prompted by the operating system.
2. Navigate to the **Device Manager** window on the PC (see Figure 9).
3. A dialog box may open asking for permission to allow the program to make changes to the computer. Click **Yes**.
4. The **Computer Management** window opens. From the list labeled **System Tools**, click **Device Manager**. If the SDP-H1 driver is installed and the SDP-H1 is properly connected to the PC, **Analog Devices SDP-H1** is shown in the **ADI Development Tools** list in the **Device Manager** window, as shown in Figure 9.

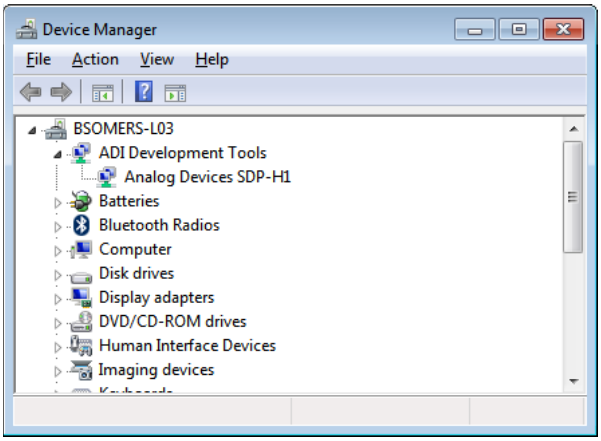


*Figure 9. **Device Manager** Window*

Disconnecting the EVAL-AD7606CFMCZ

Disconnect power from the SDP-H1, or press the reset tact switch located alongside the mini USB port on the SDP-H1 before disconnecting the EVAL-AD7606CFMCZ from the SDP-H1.

ACE SOFTWARE OPERATION

This section details the ACE software operation when evaluating the AD7606C-18. Follow the same steps when evaluating the AD7606C-16.

LAUNCHING THE SOFTWARE

After the EVAL-AD7606CFMCZ and SDP-H1 are properly connected to the PC, launch the ACE software by taking the following steps:

1. From the **Start** menu of the PC, select **All Programs > Analog Devices > ACE> ACE.exe** to open the ACE software main window shown in Figure 10.
2. If the EVAL-AD7606CFMCZ is not connected to the USB port via the SDP-H1 when the ACE software launches, the **AD7606C-18 Board** icon does not appear in the **Attached Hardware** section in ACE (see Figure 10). To make the **AD7606C-18 Board** icon appear, connect the EVAL-AD7606CFMCZ and the SDP-H1 to the USB port of the PC, wait a few seconds, and then follow the instructions in the dialog box that opens.
3. Double click the **AD7606C-18 Board** icon to open the **AD7606C-18 Board** view window shown in Figure 11.
4. Double click the **AD7606C-18** chip icon in the **AD7606C-18 Board** view window to open the **AD7606C-18** chip view window shown in Figure 12.
5. Click **Software Defaults** and then click **Apply Changes** to apply the default settings to the AD7606C-18.

DESCRIPTION OF CHIP VIEW WINDOW

After completing the steps in the Software Installation section, set up the system for data capture.

Block icons that are dark blue are programmable blocks. Clicking a dark blue block icon opens a configurable pop-up window that allows customization for the data capture, as shown for the Channel 1 input range in Figure 13.

The available programmable blocks in the **AD7606C-18** chip view window are as follows:

- Analog input range, on a per channel basis, through the icon located on each **PGA** block.
- Bandwidth mode, on a per channel basis, through each low-pass filter (LPF) block.
- System gain, offset, and phase calibration settings, on a per channel basis.
- Diagnostic multiplexer.
- Oversampling ratio lines. By setting all the oversampling ratio lines high, the AD7606C-18 enters software mode, and the oversampling ratio is set through the memory map. In hardware mode, these lines select the oversampling ratio.
- Data interface, either serial or parallel.
- Reference selection, either internal or external, through the REF SELECT switch.

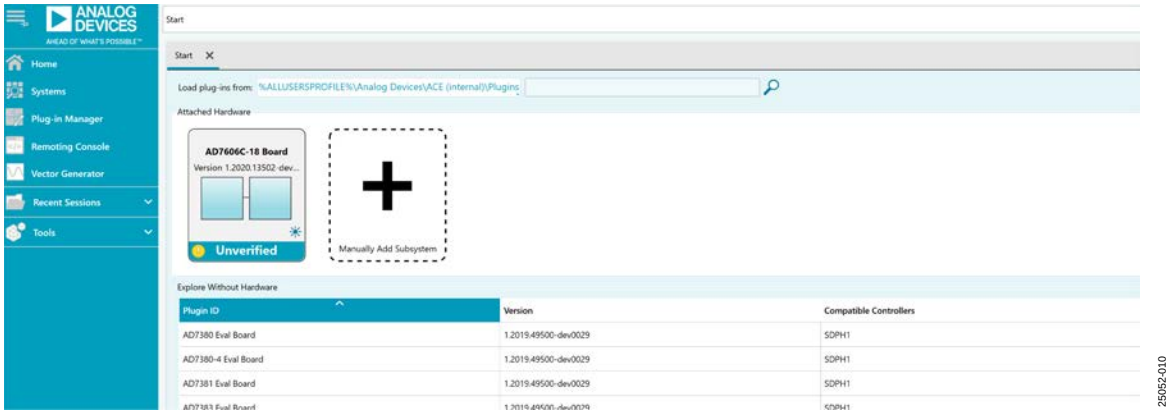
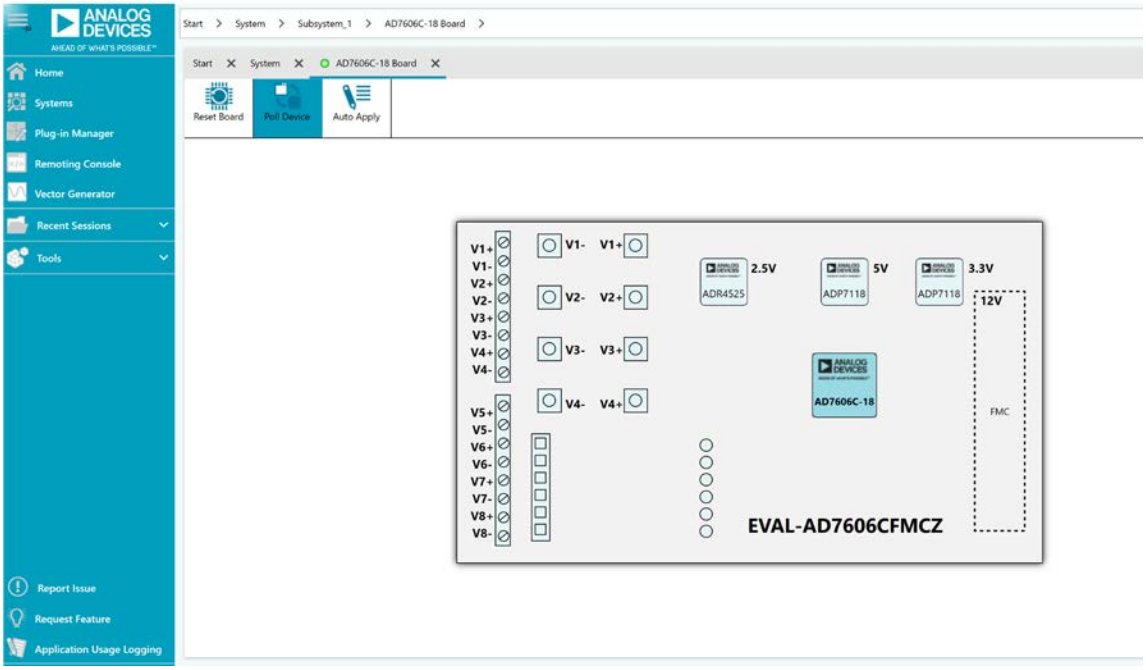
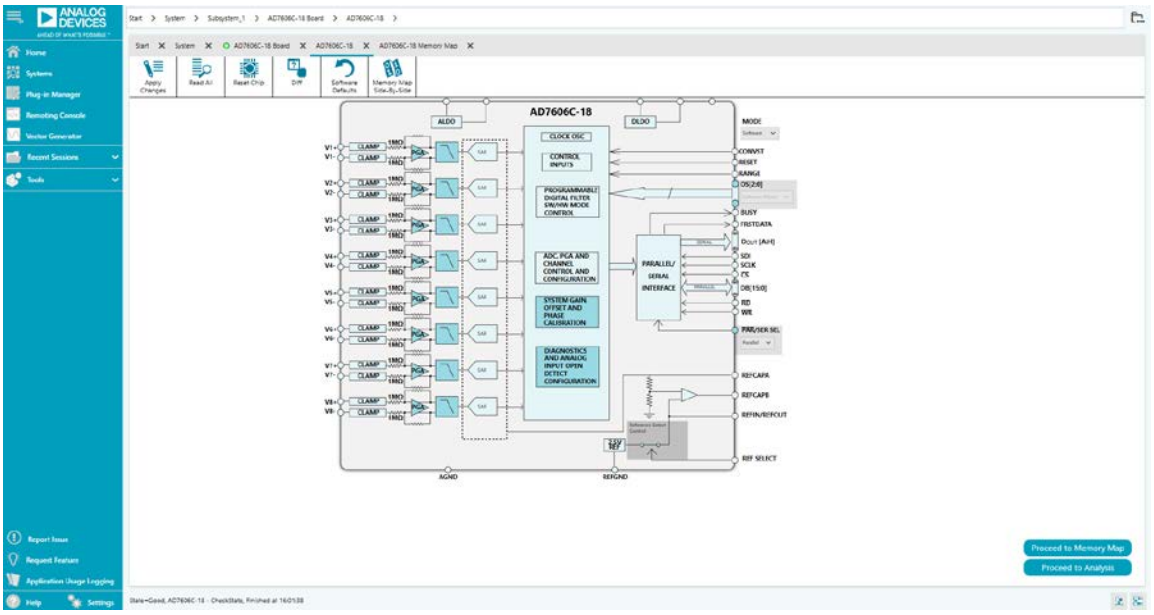


Figure 10. ACE Software Main Window



25052-011

*Figure 11. **AD7606C-18 Board** View*



25052-012

*Figure 12. **AD7606C-18** Chip View Window*

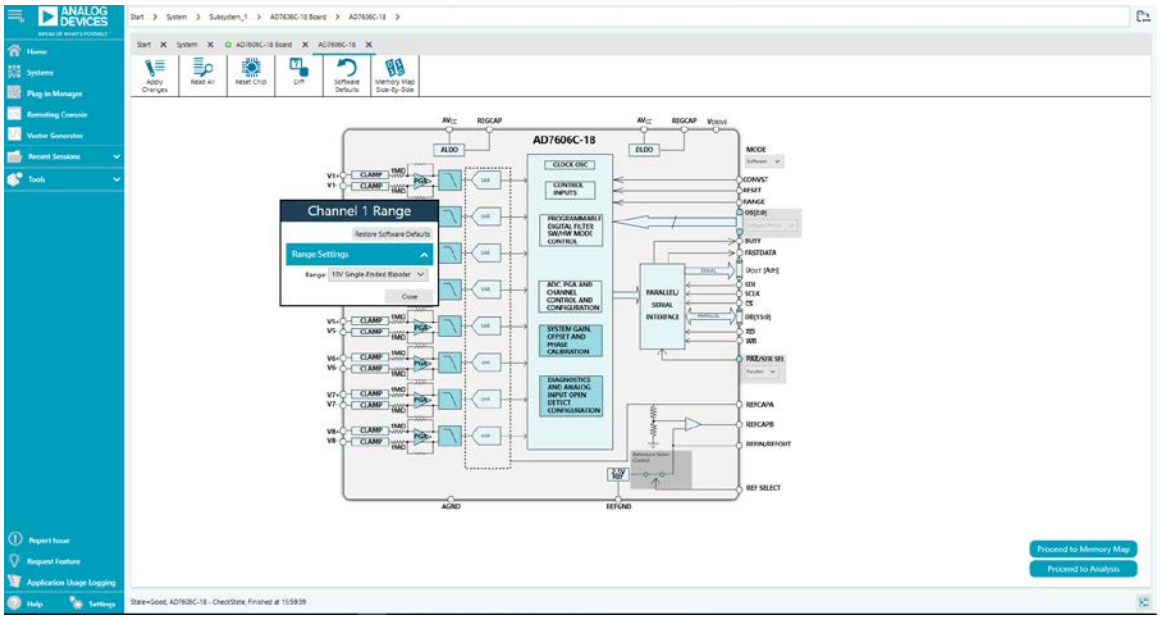


Figure 13. Configurable Pop-Up Window

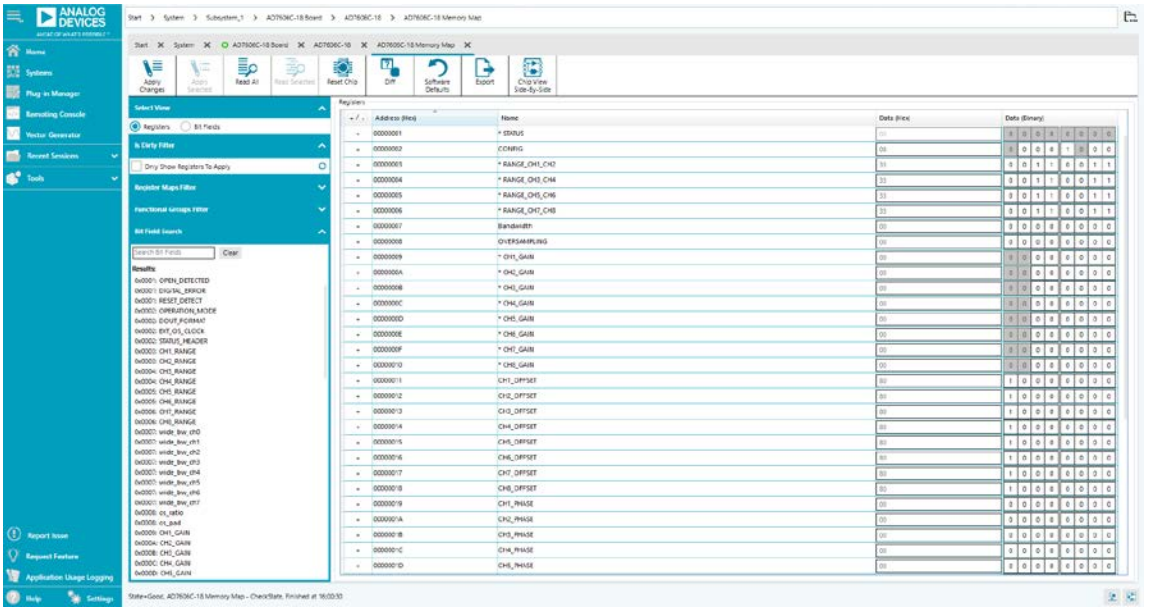


*Figure 14. **AD7606C-18 Memory Map** View Window*

DESCRIPTION OF MEMORY MAP VIEW WINDOW

Click **Proceed to Memory Map** in the **AD7606C-18** chip view window (see Figure 12) to open the **AD7606C-18 Memory Map** view window shown in Figure 14. The **AD7606C-18 Memory Map** view window shows all registers of the AD7606C-18.

The registers of the AD7606C-18 are populated with default values when powered up. To implement the values changed in all of the registers, click **Apply Changes** to write to the registers.

In some cases, the values of every register have been changed, but the user wants to implement changes on a selected register only. Click **Apply Selected** to write the new value on the selected register to the AD7606C-18.

Click **Read All** to read the values of all the registers from the chip.

Click **Read Selected** to read the selected register from the chip.

Click **Reset Chip** to prompt the software to reset the AD7606C-18.

Click **Diff** to check for differences in register values between the software and the chip.

To revert all the register values back to their defaults, click **Software Defaults**, and then click **Apply Changes** to write to the AD7606C-18.

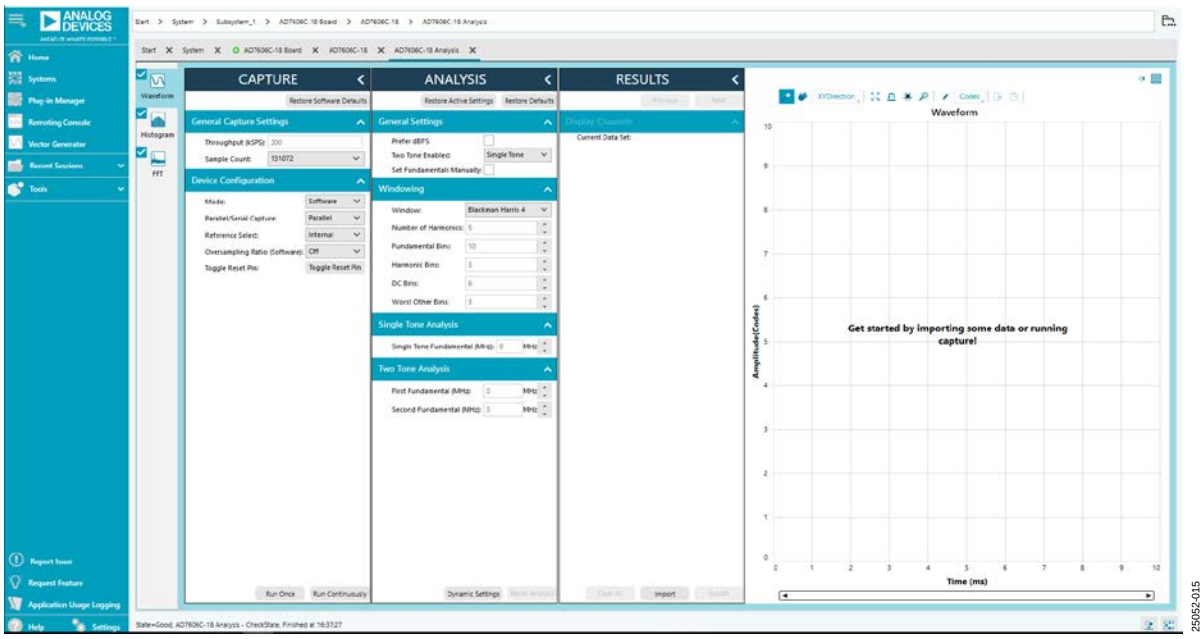


*Figure 15. **AD7606C-18 Analysis** View Window*

DESCRIPTION OF ANALYSIS WINDOW

Click **Proceed to Analysis** in the **AD7606C-18** chip view window (see Figure 12) to open the **AD7606C-18 Analysis** view window shown in Figure 15. The analysis view window contains the **Waveform** tab, **Histogram** tab, and **FFT** tab. The same features are available when evaluating the AD7606C-16.

WAVEFORM TAB

The **Waveform** tab displays data in the form of time vs. discrete data values with the results, as shown in Figure 16.

CAPTURE Pane

The **CAPTURE** pane contains the capture settings, which reflect onto the registers automatically before data capture.

The **Sample Count** pulldown menu in the **General Capture Settings** section allows the user to select the number of samples per channel per capture (see Figure 16).

The user can enter the input sample frequency in kSPS in the **Throughput (kSPS)** box in the **General Capture Settings** section (see Figure 16). Refer to the AD7606C-18 or AD7606C-16 data sheet to determine the maximum sampling frequency for the selected oversampling ratio and data interface mode.

The **Mode** pulldown menu in the **Device Configuration** section can be set as either **Hardware**, meaning that the device is configured through digital input pins, or **Software**, which allows reading and writing of the memory map and enables a wider range of features (see Figure 16). Refer to the AD7606C-18 or AD7606C-16 data sheet to determine the benefits of hardware and software mode.

The **Parallel/Serial Capture** pulldown menu in the **Device Configuration** section allows the user to select the data interface as either **Parallel** or **Serial** (see Figure 16). If **Serial** is selected, the number of data lines can be selected through the **DOUT Configuration** pulldown menu.

The **Oversampling Ratio (Software)** pulldown menu in the **Device Configuration** section can be set between 2 and 64 (in hardware mode) or 256 (in software mode) and provides improved signal-to-noise ratio (SNR) performance (see Figure 16). Refer to the AD7606C-18 or AD7606C-16 data sheet to determine the maximum oversampling ratio for the selected oversampling mode.

When hardware mode is enabled, the **Input Range** pulldown menu allows the user to select an input span between ±10 V and ±5 V. In software mode, the input span is selected either in the **AD7606C-18 Memory Map** or a configurable pop-up window in the **AD7606C-18** chip view window, as shown in Figure 13.

The **Toggle Reset Pin** button in the **Device Configuration** section issues a full reset to the AD7606C-18 (see Figure 16). Refer to the AD7606C-18 or AD7606C-16 data sheet for the different reset options available on the AD7606C-18 and the AD7606C-16.

Click **Run Once** to start a data capture of the samples at the sample rate specified in the **Throughput (kSPS)** pulldown menu for the number of samples specified in the **Sample Count** pulldown menu (see Figure 16). These samples are stored on the FPGA device and are only transferred to the PC when the sample frame is complete.

Click **Run Continuously** to start a data capture that gathers samples continuously with one batch of data at a time (see Figure 16). This operation runs the **Run Once** operation continuously.

RESULTS Pane

The **Display Channels** section allows the user to select the channels to capture (see Figure 16). The channel data is shown only if that channel is selected before the capture.

The **Waveform Results (Codes)** and **Waveform Results (Volts)** sections display the amplitude, sample frequency, and noise analysis data for the selected channels (see Figure 16).

Click **Export** to export the captured data (see Figure 16). The waveform, histogram, and FFT data is stored in .xml files along with the values of parameters at capture.

The data **Waveform** graph shows each successive sample of the ADC output (see Figure 16). The user can zoom in and out and pan over the **Waveform** graph using the embedded waveform tools above the graph. Select the channels to display in the **Display Channels** section.

Under the **Display Units** pulldown menu, select **Codes** above the **Waveform** graph (see Figure 16) to select whether the **Waveform** graph displays in units of **Codes**, **Hex**, or **Volts**. The axis controls are dynamic.

When selecting either **y-scale dynamic** or **x-scale dynamic**, the corresponding axis width automatically adjusts to show the entire range of the ADC results after each batch of samples. Select the dynamic using the **XYDirection** tool (see Figure 16).

HISTOGRAM TAB

The **Histogram** tab contains the **Histogram** graph and the **RESULTS** pane, as shown in Figure 17.

The **RESULTS** pane displays the information related to the dc performance.

The **Histogram** graph displays the number of hits per code within the sampled data (see Figure 17). The **Histogram** graph is useful for dc analysis and indicates the noise performance of the AD7606C-18 or the AD7606C-16.

FFT TAB

The **FFT** tab displays the fast Fourier transform (FFT) information for the last batch of samples gathered (see Figure 18).

ANALYSIS Pane

The **General Settings** section allows the user to set up the preferred configuration of the FFT analysis, including how many tones are analyzed. The fundamental is set manually.

The **Windowing** section allows the user to select the windowing type used in the FFT analysis, the number of **Harmonic Bins**, and the number of **Fundamental Bins** that must be included.

The **Single Tone Analysis** and **Two Tone Analysis** sections allow the user to select the fundamental frequency included in the FFT analysis. Use the **Two Tone Analysis** settings when analyzing two frequencies.

RESULTS Pane

The **Signal** section displays the **Fund Frequency** and **Fund Power** (see Figure 18).

The **Noise** section displays the **SNR** and other noise performance results (see Figure 18).

The **Distortion** section displays the harmonic content of the sampled signal and dc power when viewing the FFT analysis (see Figure 18).

AUTOMATED TEST OPERATION

To perform the automated test for the AD7606C-18 or the AD7606C-16, see the AD7606C ACE Remote Control page on the Analog Devices, Inc., website and follow the instructions to operate the hardware and software, set up the Python/MATLAB environment, and begin communication between the ACE software and the Python/MATLAB script.

EXITING THE SOFTWARE

To exit the software, click **File** and then click **Exit**.

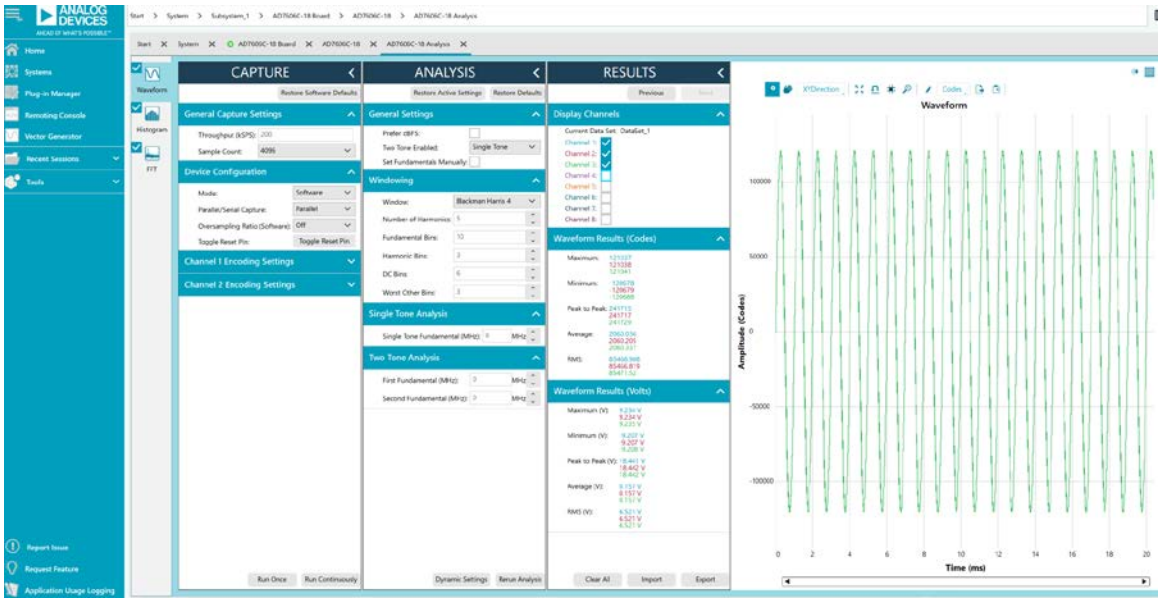


*Figure 16. **Waveform** Tab*

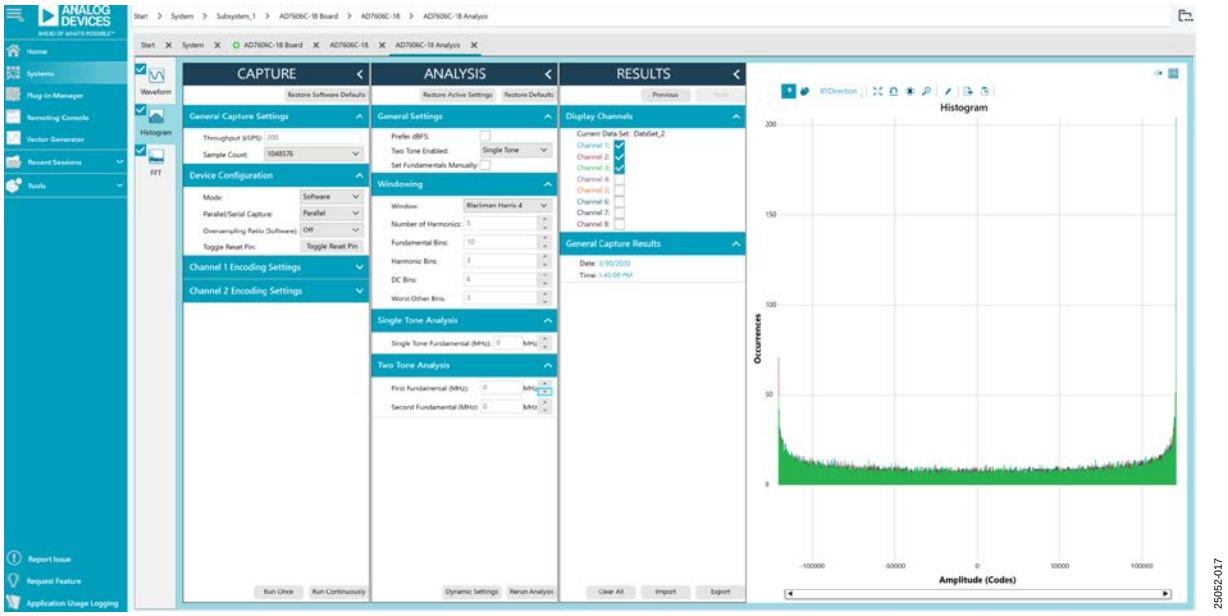


*Figure 17. **Histogram** Tab*

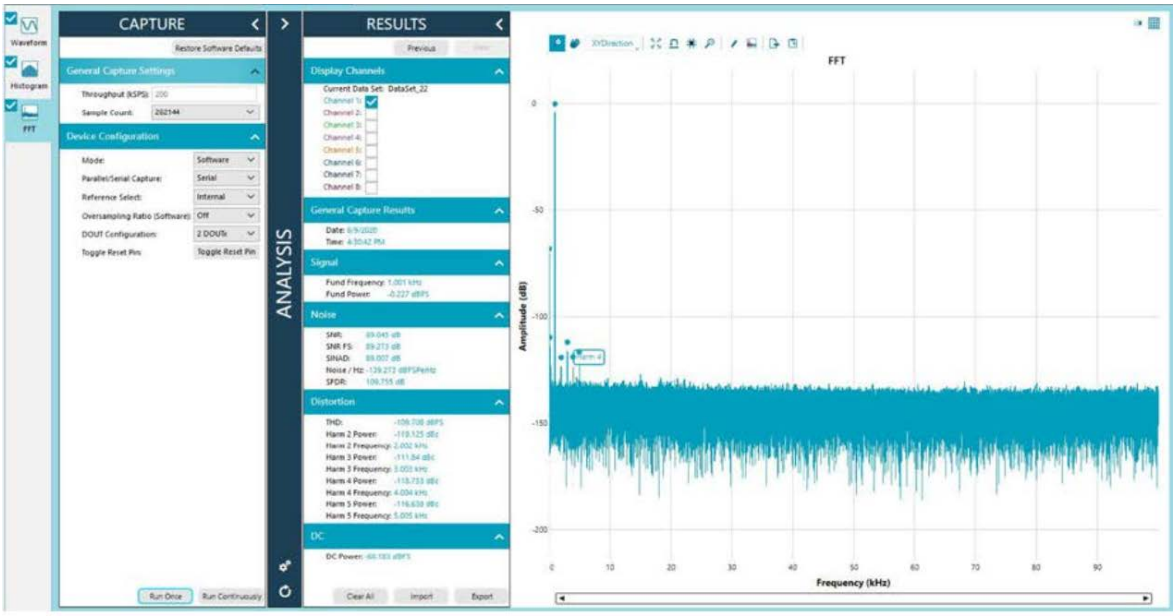


*Figure 18. **FFT** Tab*