ICL88xx flyback design guide

For high power factor flyback converter with constant voltage output

About this document

Scope and purpose

The ICL88xx family of single-stage power factor correction (PFC)/flyback controllers for constant voltage (CV) output is tailored to meet LED lighting regulatory requirements and satisfy LED lighting applications, including LED drivers with dim-to-off requirements.

This document is a design guide to using ICL88xx as a single-stage PFC flyback converter at 43 W.

It has features such as low standby power consumption (**ICL8810** and **ICL8820**) and outstanding PFC and low total harmonic distortion (THD) at full load as well as at low load conditions.

The PWM jitter feature (ICL8820) allows for ease of EMI compliance, and reduces the size, count and cost of external components for emergency lighting application in DC operation.

The evaluation board regulates a CV output, and is intended to be used with a constant current (CC) converter for LED lighting applications.

The design guide takes the reader step by step through the design process of high power factor (HPF) flyback converters and explains each step using a 52 V/43 W converter as an example.

Intended audience

This design guide is intended for power supply design engineers and field application engineers.

Table of contents

1 Introduction

The ICL88xx family is optimized for secondary-side regulated (SSR) HPF flyback converters. The simplified schematic is shown in **Figure 1**.

The ICL88xx family can also be used in a primary-side regulated (PSR) configuration – please visit **Infineon** to find more information on this topic.

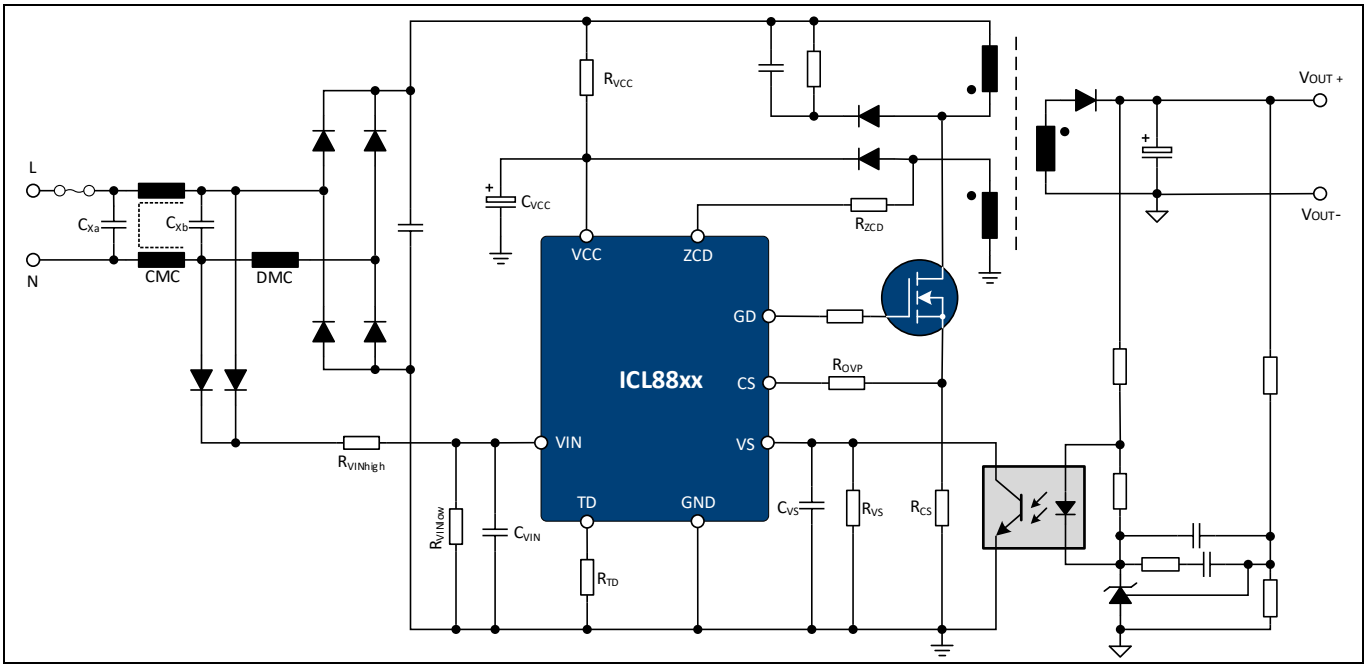

Figure 1 ICL88xx flyback converter – simplified circuitry with secondary-side regulated CV output

ICL88xx is a quasi-resonant (QR) controller operating in a critical conduction mode (CrCM) at full load and minimum input voltage. The IC will try to stay in CrCM for as long as possible. QR control helps to minimize switching noise and increases efficiency by turning on the main power MOSFET at the lowest possible drain-source voltage during transformer demagnetization.

The IC regulates the CV output, according to its feedback (FB) pin current signal, which is controlled by the secondary-side regulation FB circuit via an optocoupler.

For LED lighting applications, the ICL88xx flyback CV output is usually converted to a CC output by a second-stage DC-DC converter, which is either a switching or linear regulator.

1.1 Pin configuration and description

The ICL88xx comes in a PG-DSO-8 package with eight pins. The main functions of each pin are shown in **Table 1** and **Figure 2**.

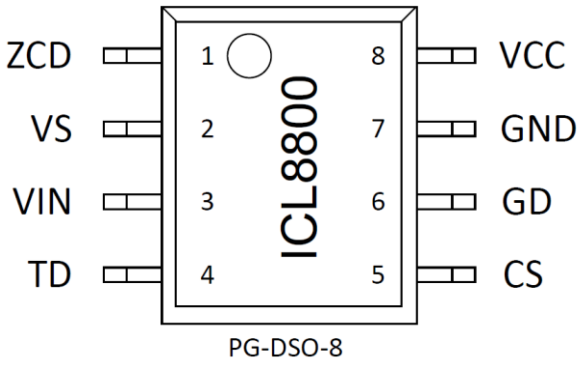

Figure 2 Pin-out of ICL88xx

Table 1 Pin definitions and functions

Name	Pin	Function
ZCD	1	**Zero crossing detection** Connected to an auxiliary winding via a resistor to detect the zero crossing of the switching current. When the zero crossing is detected, the controller initiates a new switching cycle. The resistor from the ZCD pin to the auxiliary winding is used to set the maximum on-time and therefore tune the output power limit.
VS	2	**Voltage sense** Connected to the feedback circuit. The current drawn out of this pin determines the on-time. A resistor R_{vs} of 12k is mandatory to set the correct operation point.
VIN	3	**Input voltage detection** Measure the AC or DC input voltage for power limitation, input overvoltage protection (OVP), brown-in (BI) and brown-out (BO).
TD	4	**THD correction** Sets the THD correction using a resistor to GND. The voltage on this pin can be used to control an external start-up circuit.
CS	5	**MOSFET current sense and output voltage protection** Primary-side overcurrent protection (OCP). A series resistance to the shunt resistor is used to tune a secondary OVP for the flyback topology.
GD	6	**Gate driver** PWM gate drive for the main power MOSFET.
GND	7	**Ground** Connected to ground, and represents the ground level of the IC for the supply voltage, gate driver and sense signals.
VCC	8	**Power supply** Supplies the IC.

1.2 Design process

Figure 3 shows the design guide and design step sequence for the ICL88xx family of devices.

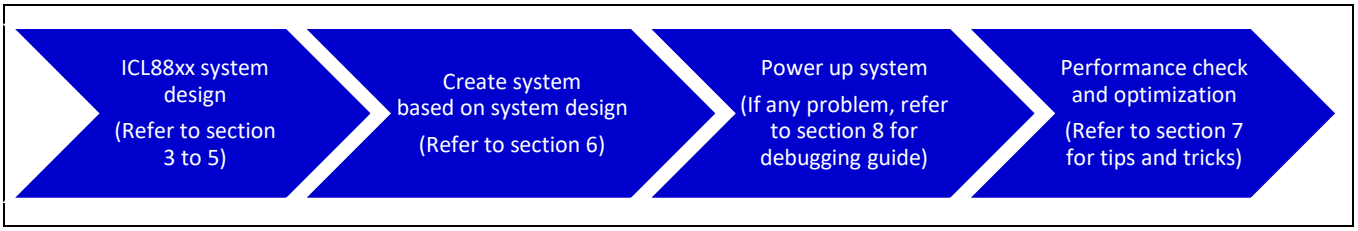

Figure 3 ICL88xx design guide document outline for each step of the recommended design flow

2 Design specifications

The ICL88xx PFC flyback converter design guide describes a step-by-step process for creating a 43.2 W CV converter. By following the step-by-step process, an engineer can develop a similar ICL88xx controlled converter with their own target specification.

2.1 Specification of a 43 W PFC flyback reference design for LED lighting applications

A front-stage HPF flyback converter with CV output set-point $V_{OUT\text{-}SET}$ of 52 V at 0.8 A was selected as a design example. The design specifications are shown in **Table 2**.

Table 2 Design specifications

Specification	Symbol	Value	Unit
Maximum AC input voltage	V_{AC}	90 to 305	V_{RMS}
Normal operational AC input voltage	$V_{AC,max}$	100 to 277	V_{RMS}
Normal operational AC input frequency	F_{line}	47 ~ 63	Hz
Secondary-side regulated CV output set-point	V_{out}	52	V
Steady-state output load current	I_{out}	0 ~ 800	mA
Steady-state full-load output power	P_{out}	43	W
Minimum efficiency at $P_{out,full}$	$\eta_{min,at,P,out}$	91	%
Target minimum switching frequency at $P_{out,full}$	$f_{sw,min,at,P,out}$	52	kHz
Standard compliance			
Harmonics	–	EN 61000-3-2 class C	-
EMI	–	EN55015	-
Board dimensions			
Size	L × B	Main board: 171 × 27	mm
Size	L × B	PlugIN-TL: 36.5 × 27	mm

Note: $P_{OUT\text{-}FULL}$ of 43.2 W is defined in this design example, to be able to supply a second-stage CC converter which has minimum efficiency of 93 percent (or maximum 3.2 W loss) at full load, for a 40 W LED driver design.

Note: The recommended $f_{sw,min,at,P,out}$ is between 50 kHz and 65 kHz. In general, a higher $f_{sw,min,at,P,out}$ value would result in a smaller flyback transformer with lower efficiency, while a lower $f_{sw,min,at,P,out}$ value would result in a larger flyback transformer with higher efficiency.

3 PFC flyback converter design

The primary function of a PFC converter is to shape and synchronize the AC-line current with the AC-line voltage. This enables maximization of real power drawn from the AC mains. In an ideal PFC circuit, the input current follows the input voltage as a pure resistor, without any input current harmonics.

On the other hand, the input current of the converter consists of the triangular currents through MOSFET Q1 (**Figure 1**), filtered and smoothed by the EMI filter consisting of C_{Xa}, C_{Xb}, the differential-mode choke (DMC) and the leakage inductance of the common-mode choke (CMC).

The relationship between the MOSFET and the input current is shown in **Figure 4**.

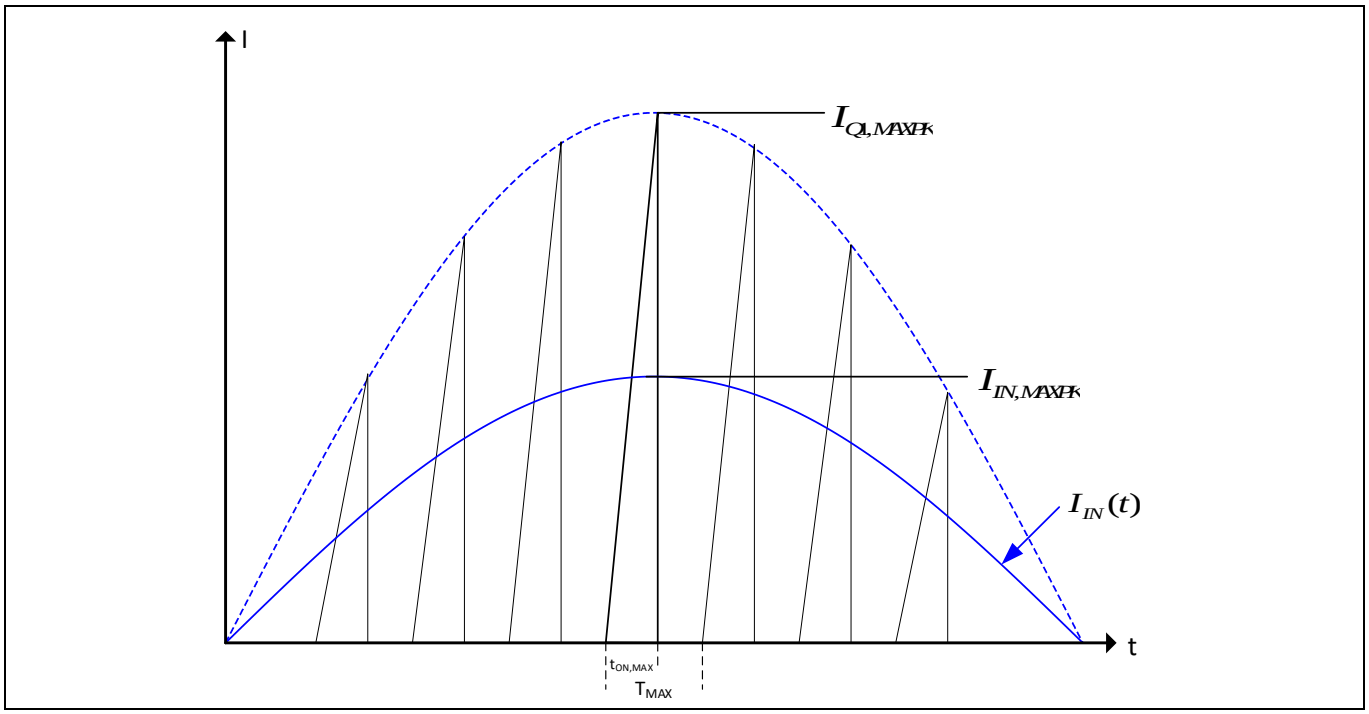

Figure 4 Flyback input current and MOSFET current (simplified)

As explained earlier, the converter operates in CrCM at the peak of the lowest line voltage, which is 90 V_{RMS} in our example. The highest peak currents at the input as well as in the MOSFET occur under this condition and consequently, this point is essential for the design. Since real and apparent power are virtually identical, the expression for $I_{IN,MAXPK}$ is simple:

$$I_{IN.MAXPK} = \frac{P_{OUT}}{\eta \cdot V_{IN,MINRMS}} \cdot \sqrt{2} \quad (1)$$

$$= \frac{43.2\ W}{0.9 \cdot 90\ V} \cdot \sqrt{2} = \underline{0.75\ A}$$

This must, by definition, be identical to the maximum peak current of the MOSFET averaged over one switching cycle:

$$\frac{I_{Q1.MAXPK}}{2} \cdot \frac{t_{ON,MAX}}{T_{MAX}} = I_{IN.MAXPK} \quad (2)$$

Definitions:

- t_{ON} – power MOSFET on-time
- T – period of switching cycle ($T = 1/f_{SW}$)

Neither t_{ON} nor T are constant in this application but vary through the line half-wave. This behavior is needed in order to achieve good THD and PF. As the above equation implies, maximum on-time $t_{ON,MAX}$ and maximum switching period T_{MAX} occur in the maximum of the lowest input voltage.

Now these two parameters, T_{MAX} and $t_{ON,MAX}$, have to be chosen. Because the maximum switching period equates to the minimum switching frequency, this parameter needs to be looked at first. A higher switching frequency can lead to a smaller transformer size on the one hand, but increases switching losses on the other.

3.1 Transformer design

To achieve both high efficiency and high power quality in quasi-resonant mode (QRM) with first valley switching (QRM1), the flyback transformer primary main winding to secondary main winding turns ratio, N, should be large. A larger turns ratios (N) will equate to a larger V_{DS} MOSFET requirement. Design trade-offs between efficiency, size and cost are considered.

To reduce transformer leakage inductance for low MOSFET voltage spike $V_{SPIKE-FET}$, transformer design with interleaved construction as shown in **Figure 5** is highly recommended. The voltage seen by the drain of the MOSFET is illustrated in **Figure 6**.

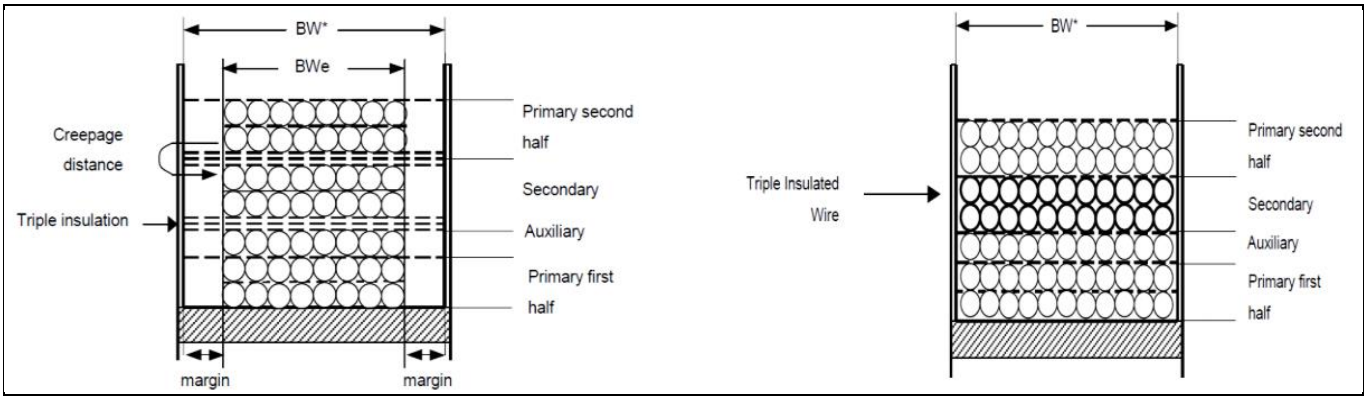

Figure 5 Transformer design with sandwich construction

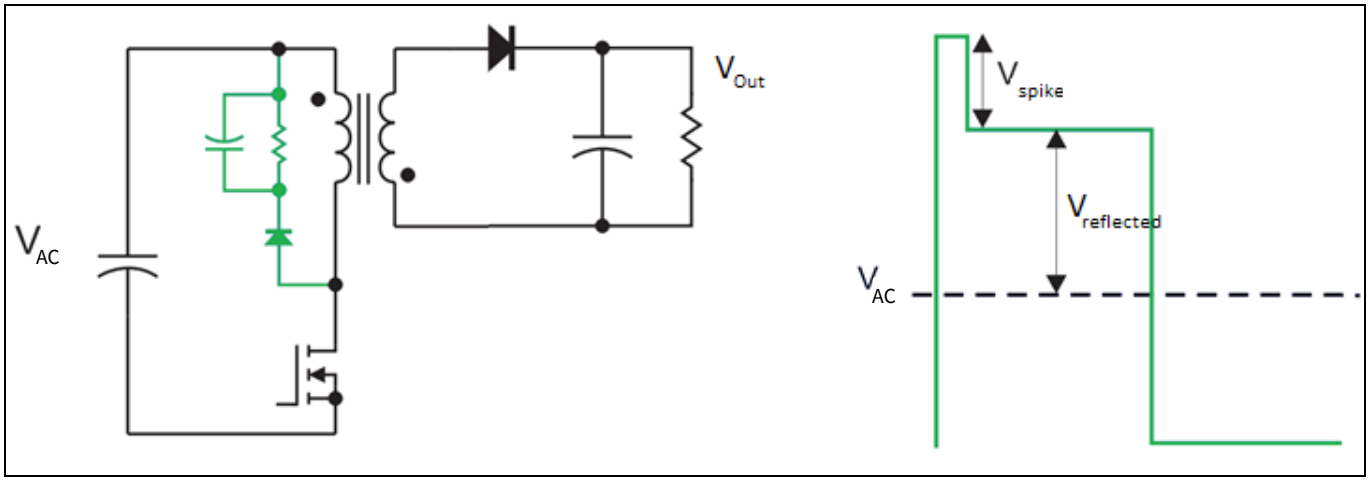

Figure 6 Snubber and MOSFET drain voltage during off-time

For this design, a minimum switching frequency at full load of 54 kHz was selected. In general, a frequency between 50 kHz and 70 kHz is recommended for wide input voltage range designs.

This minimum frequency range selection balances:

- Higher efficiency (lower f_{sw})
- Smaller transformer size (larger f_{sw})
- EMI compliance (second harmonic less than 2 × min. f_{sw})

The second step in the design process is the winding ratio of the transformer (N). A duty-cycle ratio (DCR) has to be specified, and it is recommended to choose a value between 50 and 70 percent for wide-input AC-line designs, and a range of 50 to 60 percent for narrow AC-line designs. The increased on-time in the wide-range design allows the system to remain for longer in the first valley, as it is designed around the operating point with the lowest input voltage.

The system has to operate there on the boundary of DMC/CMC operation and has to be able to deliver full power. The duty cycle has a direct impact on the magnitude of the reflected voltage as well as the secondary- and primary-side current. This duty cycle has to be chosen with these values in mind.

QR flyback efficiency increases as the reflected voltage is increased. The larger reflected voltage causes the voltage across the drain-source of the main power MOSFET to ring lower after the transformer demagnetization, allowing for less voltage across the MOSFET during turn-on transitions. Larger reflected voltages develop greater voltage stress on the MOSFET, and this must be considered. The winding ratio N is a compromise between minimizing the switching losses and the capability of the selected MOSFET.

A large duty-cycle ratio develops a higher reflected voltage across the drain-source of the main MOSFET and reduces the magnitude of the primary MOSFET and transformer current. The benefit is a reduction in both conduction losses and EMI signature. By carefully choosing the duty cycle, it is possible to balance the MOSFET performance and cost.

Larger duty cycles also reduce the off-time of the converter, resulting in higher secondary-side peak currents.

A common first attempt to determine a proper transformer winding ratio (N) is to choose a MOSFET with a given V_{DS} rating, and then determine the duty cycle and other parameters given the MOSFET chosen.

Or, define a duty-cycle ratio and perform the calculations to see which MOSFET blocking voltage is required to keep this ratio. Both ways to find a proper winding ratio N are described in this document.

The winding ratio N (and in turn $t_{ON,MAX}$) is a compromise between minimizing the switching losses and the maximum breakdown voltage $V_{(BR)DSS}$ of the selected MOSFET.

This can be seen in the volt-second balance of the transformer that yields in an equation for $t_{ON,MAX}$:

$$N \cdot (V_{OUT} + V_D) \cdot t_{OFF} = V_{IN,MINPK} \cdot t_{ON,MAX} \quad (3)$$

In this equation, N is the turns ratio of the transformer and V_D is the forward voltage of the output rectifier. Because $t_{OFF} = T_{MAX} - t_{ON,MAX}$ it becomes obvious that $t_{ON,MAX}$ and N can't be chosen independently.

The term $N \cdot (V_{OUT} + V_D)$ is the output voltage reflected to the input or short "reflected voltage" V_R. It occurs across the primary side of the transformer during the off-time of the MOSFET and adds to the input voltage as shown in **Figure 6**, increasing the maximum V_{DS}.

Option 1: Calculation of N based on DCR

With fixed-frequency (FF) flyback controller design, it is common to start the design with a defined DCR. With this ICL88xx design, it is important to mention that the DCR is determined at the operating condition where the input AC-line is at its lowest operating point, and full output power. The ICL88xx family of devices are not FF controllers, therefore the DCR is not fixed in this system and the ratio adjusts as the AC-line voltage level changes in magnitude.

Here 57 percent was selected as the DCR. This value was found after three iterations of this calculation. Based on this input and output specification, a duty cycle larger than 57 percent led to high reflected voltages, which resulted in too-small margins for the desired 800 V MOSFET and to too-high secondary currents. On the other hand, a smaller duty cycle would result in high primary current. This current would require a more expensive MOSFET with smaller $R_{DS(on)}$ in order to not overheat. Furthermore, because the on-time at low-line and full load is not as long as before, the change from the first valley to the second will happen earlier, meaning at larger loads. The effect of a larger and smaller DCR can be seen in **Figure 7**.

The selected DCR of 57 percent offers a good compromise between a high reflected voltage, a cost effective MOSFET, proper on-time and reasonably sized transformer.

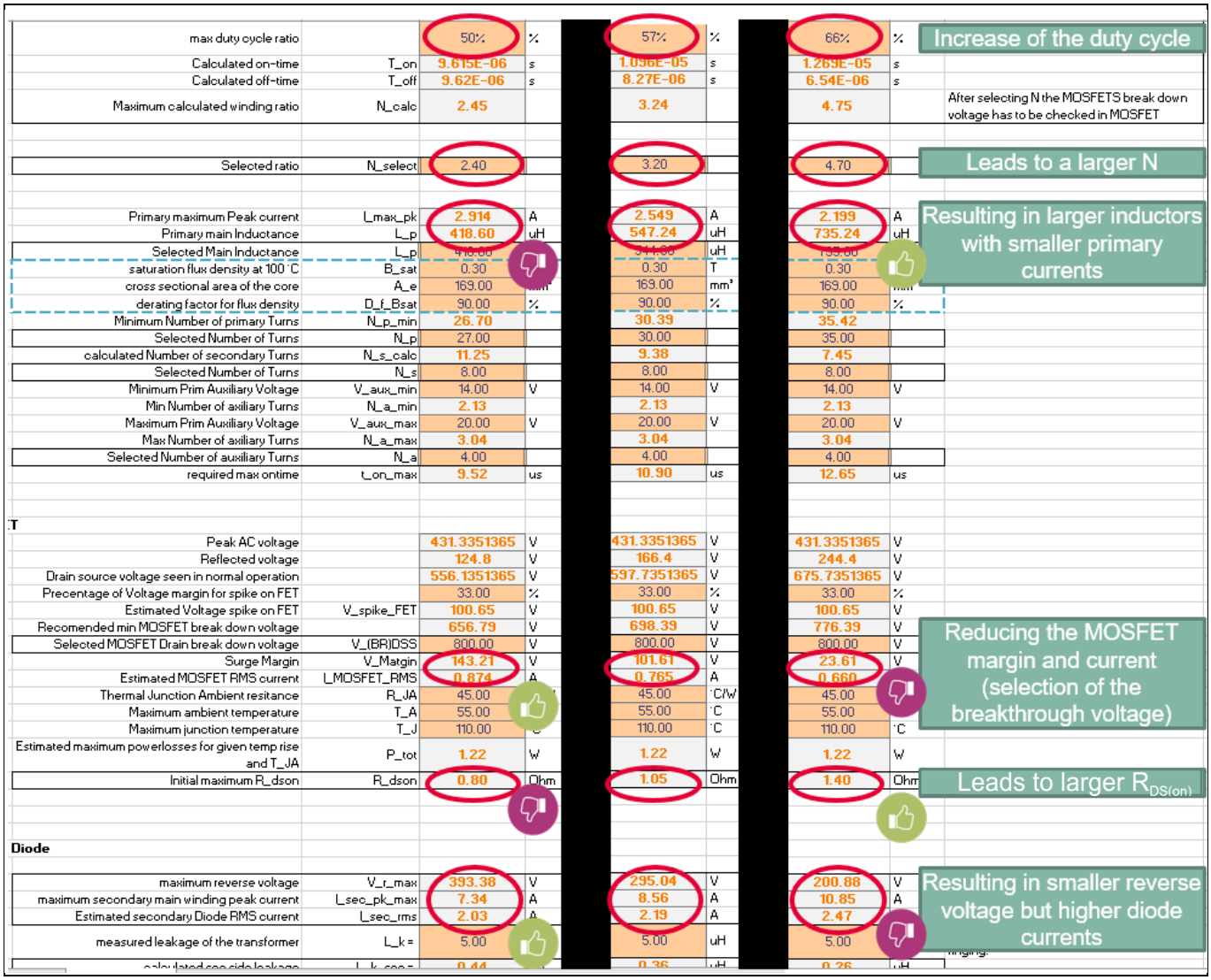

Figure 7 Effect of the duty cycle on the system, showing the trade-offs

With this information, the required winding ratio of the transformer can be calculated. First the estimated on-time and off-time of the converter are calculated:

$$t_{ON,MAX} = \frac{DCR_{MAX}}{f_{SW,MIN}} \quad (4)$$

$$t_{off} = \frac{1}{f_{SW,MIN}} - t_{ON,MAX} \quad (5)$$

$$t_{on,max} = \frac{57\%}{52\ kHz} = 10.96\ \mu s \quad (6)$$

$$t_{off} = \frac{1}{52\ kHz} - 12.7\ \mu s = 6.5\ \mu s$$

Based on the (3), N can be defined as:

$$\frac{V_{in}}{V_{out}} = N \times \frac{t_{ON}}{t_{OFF}} \quad (7)$$

$$N \leq \frac{V_{AC,MIN,PK}}{V_{OUT}} \times \frac{t_{ON,MAX}}{t_{OFF}} \quad (8)$$

$$N \leq \frac{90\ \text{V} \times \sqrt{2}}{52\ V} \times \frac{10.96\ \mu s}{6.5\ \mu s} = 3.23 \quad (9)$$

Based on the above, **N = 3.2** is selected.

Determine the drain-source voltage rating (with margin) of the main switching power MOSFET using the selected turns ratio:

$$V_{AC,MAX,PK} = V_{AC,MAX} \times \sqrt{2} = 300\ V \times \sqrt{2} = 431\ \text{V} \quad (10)$$

$$V_R = V_{OUT} \times N = 52\ V \times 3.2 = 166.4\ \text{V} \quad (11)$$

$$V_{DS} = V_R + V_{AC,MAX,PK} = 431\,V + 166.4\,V = 597.4\,\text{V} \quad (12)$$

With an RCD snubber network positioned across the primary main winding (see **Figure 10**), V_{SPIKE} can be estimated to be around 30 to 45 percent of $V_{AC,max}$. $V_{AC,max}$ is 305 V_{RMS}; V_{SPIKE} is assumed to be ≈ 100 V.

Minimum MOSFET breakdown voltage V_{DS} can be calculated as:

$$V_{DS} = V_{DS} + V_{spike} = 597.4\,V + 100\,V = 697.4\,V \quad (13)$$

It is good design practice to select a power MOSFET with a V_{DS} rating above the worst-case normal operation.

Based on the calculation above, a MOSFET with **V_{DS} = 800 V** can be selected. Here we have

$$800\,V - 697.4\,V = 102.6\,V \quad (14)$$

margin for input overvoltage or surge events.

For additional information on lightning surge and for a simulation circuit, you can read the **Lightning surge discharge design for SMPS application note**.

Option 2: Calculation of turns ratio (N) based on MOSFET V_{DS} rating

An alternative way to determine both the turns ratio and the V_{DS} rating of the power MOSFET is to first declare the MOSFET V_{DS} rating. In this example, an 800 V MOSFET was selected. In narrow-range designs and low output voltage designs a 700 V MOSFET might also be suitable. If the design comprises a large output voltage, or a greater voltage margin on the main power MOSFET is desired, a MOSFET with a V_{DS} rating of 950 V is possible.

$$V_{DS,max} = V_{AC,max} \times \sqrt{2} + N \times V_{OUT} + V_{SPIKE} + V_{MARGIN} \quad (15)$$

$$N \leq \frac{V_{DS,max} - V_{AC,max} \times \sqrt{2} - V_{SPIKE} - V_{MARGIN}}{V_{OUT} + V_D} \quad (16)$$

Where $V_{AC,max,pk}$ is $\sqrt{2}$ times $V_{AC,max}$ and V_D is the secondary main output diode forward voltage (0.70 V).

N can then be calculated as:

$$N \leq \frac{800\,V\ -\ \sqrt{2}\ \times\ 300\,V\ -\ 100\,V\ -\ 100\,V}{52\,V\ +\ 0.7\,V} = 3.21 \quad (17)$$

Finally, **N = 3.2** has been selected. From volt-second balance we finally get:

$$t_{ON,MAX} = \frac{V_R}{V_R + V_{AC,MIN,PK}} \cdot T_{MAX} \quad (18)$$

$$T_{\max} = \frac{1}{f_{sw,min}} = \frac{1}{52\ kHz} = 19.23\ \mu s \quad (19)$$

$$V_R = 3.2 \cdot (52\,V + 0.7\,V) = 168.64\,V \quad (20)$$

$$t_{ON,MAX} = \frac{168.64\,V}{168.64\,V + 127.28\,V} \cdot 19.23\ \mu s = 0.57 \cdot 19.23\ \mu s = 10.96\ \mu s \quad (21)$$

Calculation of the peak currents

After finding the winding ratio by one of the two methods, the maximum primary-side currents have to be calculated.

The maximum primary peak current $I_{Q1.MAXPK}$ can then be calculated as:

$$I_{Q1.MAXPK} = \frac{2 \cdot I_{AC.MAXPK}}{d_{MAX}} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{\eta \cdot V_{AC,MINRMS} \cdot DCR_{MAX}} \quad (22)$$

$$I_{Q1.MAXPK} = \frac{2 \cdot \sqrt{2} \cdot 43.2\ W}{0.9 \cdot 90\ V \cdot 0.57} = 2.605\ A$$

As a result, the primary main winding inductance L_p can be defined and calculated as:

$$L_P = \frac{V_{AC,MINPK}}{I_{Q1.MAXPK}} \cdot t_{ON,MAX} \quad (23)$$

$$L_P = \frac{\sqrt{2} \cdot 90\ V \cdot 11.13\ \mu s}{2.605\ A} = 544\ \mu H$$

An inductance of $\boldsymbol{L_P = 544\ \mu H}$ is selected for this design.

Based on core cross-sectional area, A_e = 120.3 mm^2 and saturation flux density at 100°C, $B_{SAT(T=100°C)}$ = 0.390 Tesla for PQ26/20 core, the transformer primary main winding turns N_p can be defined as:

$$N_p \geq \frac{L_p \cdot I_{Q1,MAXPK}}{A_e \cdot B_{SAT(T=100°C)} \cdot D_{F,SAT}} \quad (24)$$

Where $D_{F,SAT}$ is the derating factor to ensure the designed transformer maximum flux density, B_{MAX} is below $B_{SAT(T=100°C)}$ by a margin of (100 percent - $D_{F\text{-}BSAT}$) from saturation, and it is typical to set $D_{F\text{-}BSAT}$ in the range of 85 to 95 percent for a margin of 5 to 15 percent from transformer core saturation.

$D_{F\text{-}BSAT}$ = 90 percent, N_p can then be calculated as:

$$N_p \geq \frac{544 \times 10^{-6}\ H \times 2.605\ A}{120.1 \times 10^{-6} m^2 \times 0.39\ T \times 90\%} = 30.39 \quad (25)$$

N_p = 32 is selected.

The transformer secondary main winding turns N_s can then be calculated as:

$$N_s = \frac{N_p}{N} = \frac{32}{3.2} \quad (26)$$

$$\boldsymbol{N_s = 10}$$

Auxiliary winding ratio determination

Define a minimum and maximum turns ratio based on good design choices.

To ensure fast start-up of the system, and to eliminate restart, the V_{CC} supply powering the ICL88xx device is chosen as 14 V. As a result, the recommended minimum primary auxiliary winding turns $N_{A,MIN}$ can be defined and calculated as:

$$N_{A,MIN} = \frac{V_{A,MIN} \times N_s}{(V_{OUT} + V_D)} = \frac{14\,V \times 10}{(54\,V + 0.7\,V)} = 2.56 \quad (27)$$

To ensure high efficiency, V_{CC} voltage should remain less than 19 V; $V_{A,MAX}$ is therefore defined as 19 V.

$N_{A,MAX}$ can be defined and calculated as:

$$N_{A,MAX} = \frac{V_{A,MAX} \times N_s}{(V_{OUT} + V_D)} = \frac{19\,V \times 10}{(54\,V + 0.7\,V)} = 3.47 \quad (28)$$

Based on the calculation results of equations (27) and (28), primary auxiliary winding turns **N_A = 3** is selected.

An additional auxiliary winding on the secondary side is added to power the SSR feedback circuit, as its op-amp or shunt regulator's maximum operating voltage is considerably less than $V_{OUT-SET}$ of 54 V.

The recommended minimum secondary auxiliary winding turns $N_{A,SEC,MIN}$ and recommended maximum secondary auxiliary winding turns $N_{A,SEC,MAX}$ can be defined respectively as per $N_{A,MIN}$ and $N_{A,MAX}$, as shown below:

$$N_{A,SEC,MIN} = N_{A,MIN} = 2.56 \quad (29)$$

$$N_{A,SEC,MAX} = N_{A,MAX} = 3.47 \quad (30)$$

$N_{A,SEC}$ = 3 is selected.

3.2 Flyback MOSFET and secondary main output diode selection

The CoolMOS™ P7 MOSFET series from Infineon is well suited to ICL88xx applications, due to its balance of high performance and reasonable cost.

Through optimizing key parameters (C_{oss}, E_{oss}, Q_g, C_{iss} and $V_{GS(th)}$), integrating a Zener diode for ESD protection and other measures, this product family fully addresses market concerns in performance, ease of use and price/performance ratio.

The 700 V, 800 V and 950 V CoolMOS™ P7 MOSFET series have been specifically designed for flyback and PFC topologies (hard-switching).

MOSFET drain-source breakdown voltage **$V_{(BR)DSS}$ = 800 V** is selected in this design example based on $V_{AC,max}$ of 300 V_{RMS} and transformer design in chapter **3.1**.

On-resistance ($R_{DS(on)}$) of the MOSFET should be considered next to ensure power dissipation under all operating conditions.

MOSFET $R_{DS(on)}$ and maximum primary RMS current $I_{PRI\text{-}RMS\text{-}MAX}$ must be estimated based on:

$$I_{Q1,MAX(RMS)} \approx I_{Q1.MAXPK} \times x \quad (31)$$

In a HPF flyback converter, the peak current occurs at the peak of the sinusoidal input voltage. The waveform of the current through the MOSFET is triangular in shape and flows only during the constant on-time of the MOSFET. Connecting all the peaks of the currents during one half-cycle of the input voltage would lead to a sinusoidal shape. Unfortunately, it is not easy to calculate the accurate average primary current, because the off-time is not fixed. These relationships are illustrated in **Figure 8**.

The value x, which helps to calculate the average current out of the peak current in a HPF flyback, is dependent on the ratio between the minimum peak input voltage and the reflected output voltage. Although these values vary from design to design, this value can be approximated by 0.3. If the DCR were fixed, e.g., due to DC input, x could be calculated as:

$$x = \sqrt{\frac{DCR}{6}} \quad (32)$$

With the initially chosen DCR_{MAX} of 0.57, x would be 0.31, which shows that 0.3 is a fair approximation. $I_{PRI-MAX(RMS)}$ can then be calculated as:

$$I_{Q1,MAX(RMS)} \approx 2.605 \times 0.3 \quad (33)$$

$$I_{Q1,MAX(RMS)} \approx \mathbf{0.765\ A}$$

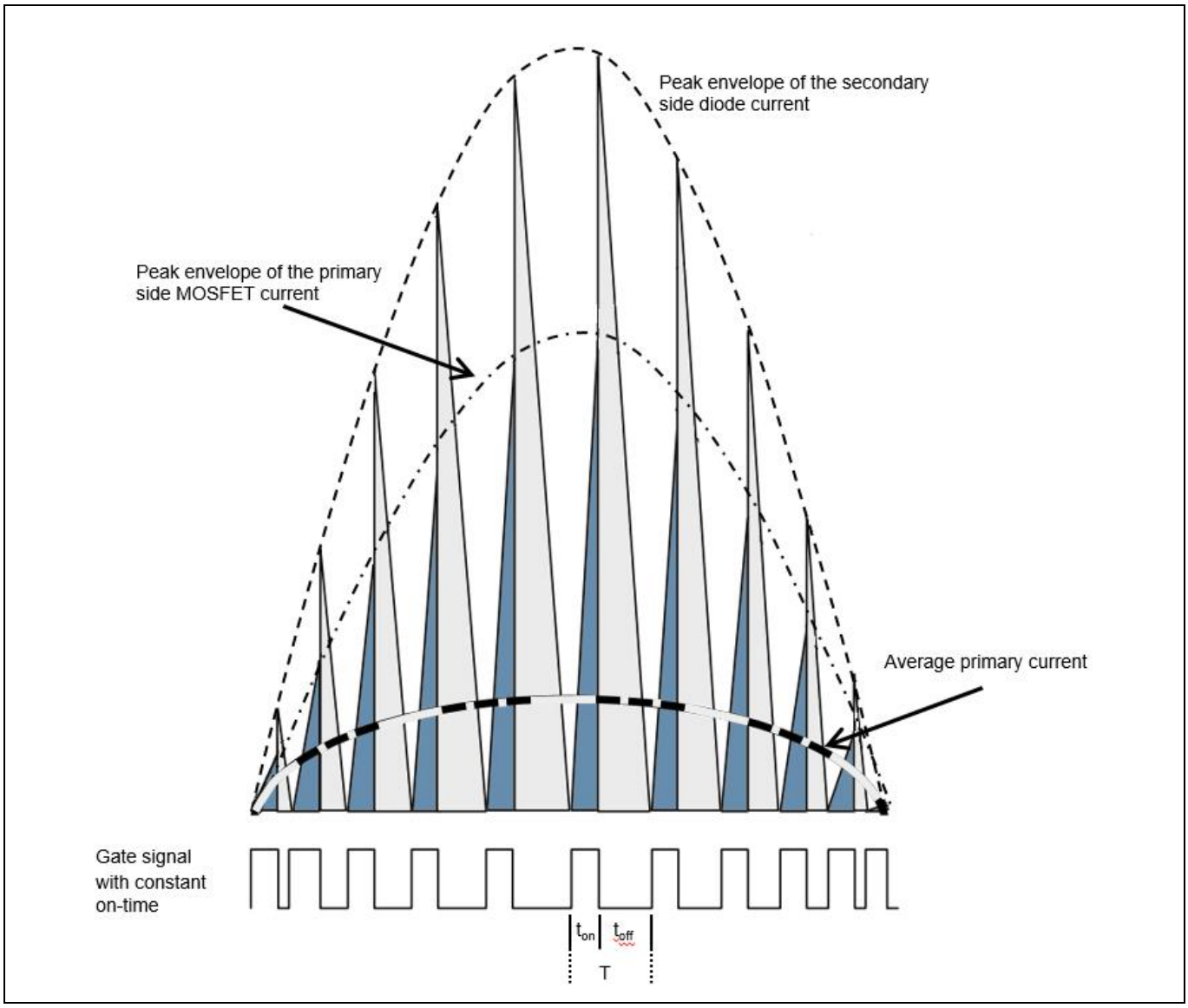

Figure 8 Relationship of the main flyback currents with regard to the input voltage

MOSFET $R_{DS(on)}$ selection

A critical electrical parameter when selecting a power MOSFET is the on-state resistance. The limit for the on-state resistance is the maximum allowable power dissipation of the application and the maximum junction temperature of the MOSFET.

A starting point for selecting the proper on-resistance of a power MOSFET is packaging and cost. For sub-100 W flyback converters, a TO-220, DPAK or SOT-223 package is likely to be selected.

Once a MOSFET package has been chosen, an estimate of on-state resistance is determined. During bench analysis, the MOSFET can be optimized for lower on-resistance, or higher residence (to save cost) if required. Infineon offers dozens of on-state resistance options for a given package and rated drain-source voltage.

The power losses of the MOSFET can be divided into the conduction losses and the switching losses. An easy first-pass guideline is to assume 50 percent conduction losses and 50 percent switching losses.

$$P_{TOT} = P_{COND} + P_{SW}, \tag{34}$$

$$P_{COND} = \frac{1}{2} P_{TOT}$$

$R_{DS(on)}$ determination and process

- Package choice: DPAK
- Typical $R_{\theta JA}$ for this package ranges from 30°C/W to 50°C/W
- MOSFET RMS current is determined to be 0.765 A
- Maximum allowed junction temperature is 100°C
- Maximum operating ambient air temperature is 45°C

$$R_{\theta JA} = \frac{T_J - T_C}{P_{TOT}} \tag{35}$$

$$P_{TOT} = \frac{100°C - 45°C}{45\frac{°C}{W}} \approx 1.25\ W \tag{36}$$

$$P_{COND} = \frac{1}{2} P_{TOT} = 0.625\ W \tag{37}$$

$$R_{DSON-MAX} = \frac{P_{COND}}{{I_{RMS}}^2} \quad (38)$$

$$R_{DSON-MAX} = \frac{0.625\ W}{(0.765\ A)^2} = 1\ \Omega$$

Referring to the calculation results of equation (38) and **Table 3** below, $R_{DS(on),25°C}$ **= 900 mΩ** is selected.

Table 3 800 V CoolMOS™ P7 MOSFET selection table

$R_{DS(on)}$ [mΩ]	TO -220	TO-220 FullPAK	TO-247	TO-252 (DPAK)	TO-251 (IPAK)	TO-251 (IPAK Short Lead)	SOT-223	TO-220 FullPAK narrow lead
280	IPP80R280P7	IPA80R280P7	IPW80R280P7	IPD80R280P7				IPAN80R280P7
360	IPP80R360P7	IPA80R360P7	IPW80R360P7	IPD80R360P7				IPAN80R360P7
450	IPP80R450P7	IPA80R450P7		IPD80R450P7				IPAN80R450P7
600	IPP80R600P7	IPA80R600P7		IPD80R600P7	IPU80R600P7	IPS80R600P7	IPN80R600P7	
750	IPP80R750P7	IPA80R750P7		IPD80R750P7	IPU80R750P7	IPS80R750P7	IPN80R750P7	
900/950	IPP80R900P7	IPA80R900P7		IPD80R900P7	IPU80R900P7	IPS80R900P7	IPN80R950P7	
1200	IPP80R1K2P7	IPA80R1K2P7		IPD80R1K2P7	IPU80R1K2P7	IPS80R1K2P7	IPN80R1K2P7	
1400	IPP80R1K4P7	IPA80R1K4P7		IPD80R1K4P7	IPU80R1K4P7	IPS80R1K4P7	IPN80R1K4P7	
2000				IPD80R2K0P7	IPU80R2K0P7	IPS80R2K0P7	IPN80R2K0P7	
2400				IPD80R2K4P7	IPU80R2K4P7	IPS80R2K4P7	IPN80R2K4P7	
3300				IPD80R3K3P7	IPU80R3K3P7		IPN80R3K3P7	
4500				IPD80R4K5P7	IPU80R4K5P7		IPN80R4K5P7	

Secondary-side diode selection

The first step is to estimate the maximum reverse voltage $V_{RD,MAX}$ and maximum secondary main winding peak current $I_{SEC-MAX(PK)}$, based on:

$$V_{RD,MAX} = V_{D,SPIKE} + V_{OUT} + \frac{V_{AC,MAX.PK} + V_{MARGIN}}{N} \quad (39)$$

Where $V_{D,SPIKE}$ is the diode reverse voltage spike.

Assuming:

$$V_{D,SPIKE} \approx 35\% \times \left(V_{OUT} + \frac{V_{AC,MAX,PK} + V_{MARGIN}}{N}\right) \quad (40)$$

$$V_{RD,MAX} \approx 135\% \times \left(V_{OUT} + \frac{V_{AC,MAX,PK} + V_{MARGIN}}{N}\right) = 135\% \times \left(54\,V + \frac{\sqrt{2} \times 305\,V + 100\,V}{3.2}\right) \quad (41)$$

$$V_{RD,MAX} \approx 295.04\,V$$

$$I_{SEC-MAX(PK)} \approx I_{Q1.MAX,PK} \cdot \frac{N_p}{N_s} = 2.55 \cdot \frac{32}{10} \quad (42)$$

$$I_{SEC-MAX(PK)} \approx \mathbf{8.56\,A}$$

Based on the above, a secondary main output diode with repetitive reverse voltage rating $\boldsymbol{V_{RRM}}$ **= 300 V** is selected. To minimize its switching and conduction losses, the selected diode also has the properties of hyper-fast recovery speed and low forward voltage drop at $I_{SEC-MAX(PK)}$.

In addition, a RC secondary snubber network, for example a 10 Ω resistor in series with 150 pF capacitor, is deployed across the secondary main output diode, to suppress the diode reverse voltage spike and the EMI.

3.3 Output capacitor

$V_{ripple,out(pk-pk),max}$ denotes the maximum allowable secondary main output voltage peak-to-peak ripple level. Assuming the flyback output in this design example is connected to a second-stage CC buck regulator, which has a maximum LED voltage load $V_{LED,max}$ of 48 V and maximum allowable duty cycle $D_{buck,max}$ of 95 percent, $V_{ripple,out(pk-pk),max}$ can be defined and calculated as:

$$V_{rippleout(pk-pk),\max} = 2 \times \left(V_{out} - \frac{V_{LEDmax}}{D_{buckmax}}\right) = 2 \times \left(54\,V - \frac{48\,V}{0.95}\right) = 6.95\,V \quad (43)$$

The secondary main output capacitor $C_{out,main}$ value can then be defined and calculated as:

$$C_{out,main} \geq \frac{P_{out}}{2 \times \pi \times F_{line,min} \times V_{ripple,out(pk-pk),\max} \times V_{out}} = \frac{41.6W}{2 \times \pi \times 47Hz \times 6.95V \times 52V} = 387\,\mu F \quad (44)$$

Considering the electrolytic capacitor value tolerance, $C_{out,main}$ = 470 µF is selected in this design example. For switching noise filtering, low-ESR ceramic capacitors $C_{out,main,lowESR1}$ = 1 µF and $C_{out,main,lowESR2}$ = 0.1 µF are also added in parallel with $C_{out,main}$.

The secondary auxiliary output capacitor $C_{out,aux,sec}$ is recommended to be at least 47 µF, to ensure stable operating voltage supply of the SSR FB circuit, during burst mode.

$C_{out,aux,sec}$ = 100 µF is selected in this design example.

3.4 MOSFET snubber design

The voltage across the drain-source of the power MOSFET is ideally a square wave with a plateau determined by the AC input voltage and the reflected output voltage.

During the turn-off transition of the power MOSFET, the MOSFET switch stops the current flow through the leakage inductance of the transformer. This causes a spike voltage at the drain of the MOSFET. Together with the stray capacitance of the circuit, this produces high-frequency, high-amplitude oscillation. This high-frequency voltage spike is seen rising above the plateau mentioned earlier and needs to be considered when determining the V_{DS} rating of the power MOSFET.

Many flyback design application notes ignore the snubber; it is sometimes difficult to optimize, and no clear guideline/optimum calculation can be given as each circuit is different and the stray inductances and capacitances vary. But there are three major issues if this waveform is ignored:

- The excessive voltage spike can lead to an avalanche breakdown of the MOSFET if the margin is too small.
- Ringing energy is radiated and conducted throughout the system (power supply and load), which causes noise issues and can cause mis-triggering.
- The ringing shows up in the conducted and radiated EMI measurement.

There are numerous methods to dampen the oscillation and reduce the voltage spike magnitude. In this document the RCD circuit is explained, which can be seen in **Figure 10**.

First the leakage inductance of the transformer must be measured, because it has the dominant role in the oscillation. Furthermore, it is the easiest to measure. The ringing capacitance is a combination of inter-winding capacitance, non-linear semiconductor capacitances and other stray capacitances in the system. Luckily, the resonance is in the low MHz region, so most of the oscilloscopes should be able to measure and display it.

The voltage spike at the MOSFET can be clamped to a desired maximum V_{SPIKE} value by selecting an appropriate valued capacitor. The resistor in parallel to the capacitor has to dissipate the charge stored in it.

The design of the clamping network for a PFC flyback is a bit more complicated than that for one with constant input voltage. This is because the peak drain current is modulated by a sinusoidal half-wave and thus the energy stored in the leakage inductance has a modulation of the form $(\sin(2 \times \pi \times f_L \times t))^2$, with f_L being the line frequency. Consequently, the **average** energy that needs to be dissipated in the clamping network is half of that calculated by means of $I_{Q1.MAXPK}$:

$$P_{Snub} = \frac{1}{4} \times L \times {I_{Q1.MAXPK}}^2 \times f_{SW} \times \frac{V_R + V_{SPIKE}}{V_{SPIKE}} \quad (45)$$

The factor $(V_R + V_{SPIKE})/V_{SPIKE}$ results from the fact that the voltage across the leakage inductance (V_{SPIKE}) and the reflected voltage (V_R) are in series together conduct the demagnetization current of the leakage inductor.

In this design example, a MOSFET with a breakdown voltage of 800 V has been selected and this limit should not be exceeded and V_{SPIKE} has been selected to be 100 V. Then the calculated dissipation of the clamp network would be:

$$P_{Snub} = \frac{1}{4} \times 5\ \mu H \times (2.605\ A)^2 \times 52\ kHz \times \frac{166\ V + 100\ V}{100\ V} = \mathbf{1.17\ W} \quad (46)$$

The actual power dissipation will be lower than that since part of the energy is transferred to the output capacitance of the MOSFET and parasitic capacitances of the system.

The value of the resistor is based on P_{Snub} that needs to be dissipated by the latter. Assuming that the voltage across the clamp network is reasonable constant, its value can be determined by:

$$R_{Snub} = \frac{(V_R + V_{SPIKE})^2}{P_{Snub}} \quad (47)$$

$$R_{Snub} = \frac{(166\ V + 100\ V)^2}{1.17\ W} = 60.4\ k\Omega$$

In order to calculate the value of the capacitor, we must specify how large the maximum ripple of the snubber capacitor is allowed to be. Let's assume it to be 30 percent in this calculation:

$$C_{Snub} = \frac{V_{SPIKE} + V_R}{V_{ripple} \times R_{Snub} \times f} \quad (48)$$

$$C_{snub} = \frac{100\ V + 166\ V}{\left(30\% \times (100\ V + 166\ V)\right) \times 60\ k\Omega \times 52\ kHz} = 1.1\ nF$$

Due to parasitic capacitances mentioned earlier, the actual power dissipation will be smaller which means the optimum resistance will be higher and the capacitance smaller than the values calculated above.

Furthermore, a small capacitor is beneficial for the THD performance, since close to the zero crossing of the input voltage, less energy is required to charge up the capacitor to V_R if it gets discharged below this voltage. In addition, a small capacitor is also beneficial for the efficiency of the burst mode for the same reason.

The resistor has a similar impact on the system. The smaller the losses of the snubber due to a larger resistor, the better the THD performance and the efficiency.

These measures, smaller capacitor and larger resistor, increase the drain voltage of the MOSFET. A trade-off has to be made between a higher V_{DS} MOSFET voltage versus the losses in the snubber.

This calculation offers a good starting point for the optimization.

Further guidelines for a proper RCD snubber design:

- The snubber diode is crucial. It must be able to withstand the occurring peak voltages, and it needs to be able to handle the currents. It is strongly advised to use a fast diode in order to achieve good THD and PF.
- The voltage across the snubber capacitor should be very stable. If the voltage is triangular or shows spikes, either the selected diode has a too-low voltage rating, the selected resistor is too small or the capacitor is too small.
- When optimizing the snubber, a compromise must be found between spike voltage and power dissipation. The lower the spike voltage, the higher the losses.
- The voltage across the snubber circuit is high, so care should be taken when selecting the voltage rating of the capacitor.
- Adjust the clamping voltage by raising or lowering the resistance of the snubber resistor, with all other snubber components fixed.

After some testing, 630 pF and 200 kΩ were used in the final design, since these values clamp the voltage sufficiently. For stronger clamping and a more stable voltage between the capacitor and the diode, a larger capacitor can be used.

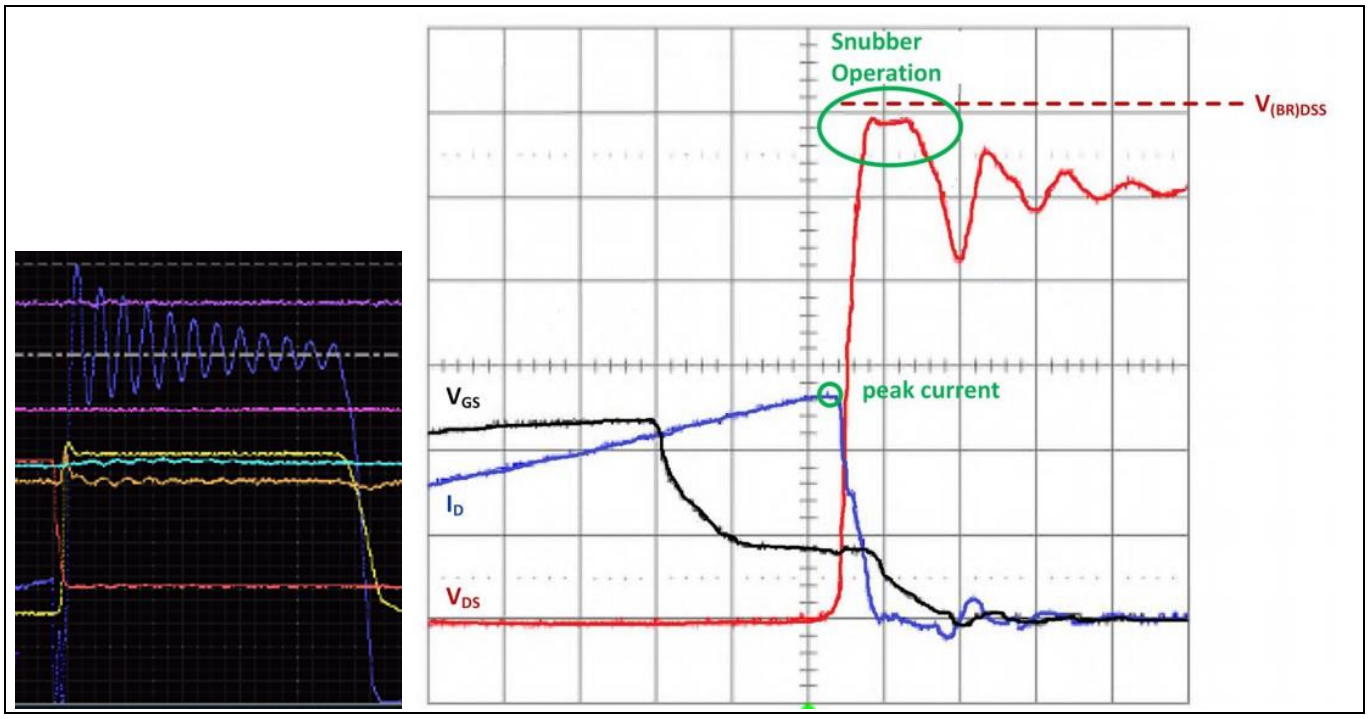

Figure 9 Oscillating drain-source voltage without snubber

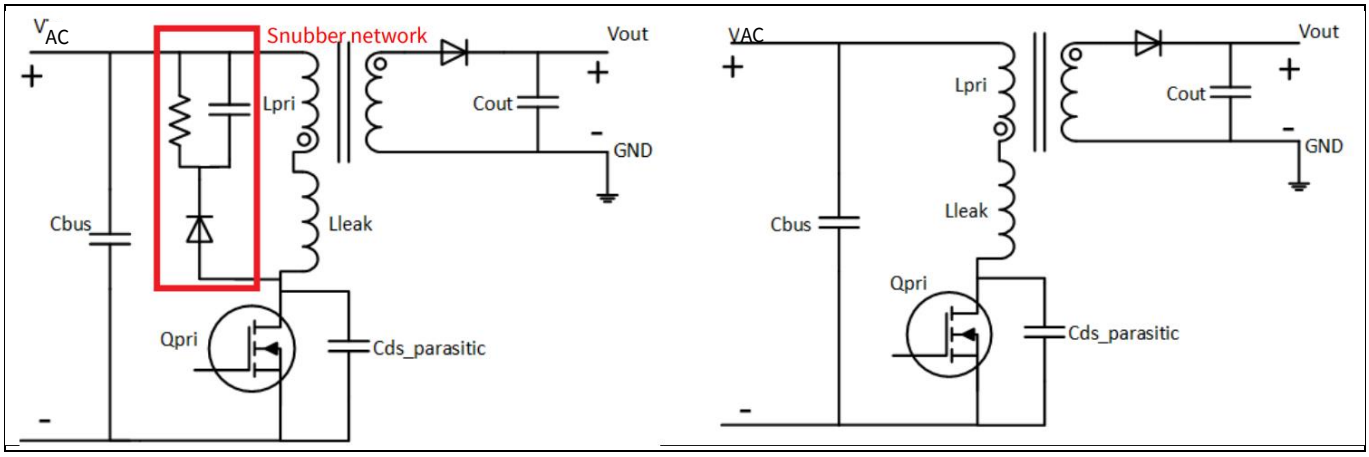

Figure 10 The typical RCD (in red) snubber vs. snubberless configuration

Design consideration: Snubberless design

The new 950 V variant of the CoolMOS™ P7 MOSFET enables a more efficient standard flyback without RCD snubber.

By removing the snubber network and switching to a snubberless design, the overall system efficiency can be improved. Switching losses and snubber losses play a large role in the losses of this supply due to the HV operation. In addition to improving the system efficiency, the snubberless flyback converter also reduces the necessary PCB area and removes the cost of the RCD network.

The losses of the system are reduced in a snubberless design (see **Figure 9**) due to removing two key loss mechanisms.

The first is that the RCD network charges up to the reflected voltage every switching cycle regardless of the system load. The leakage inductance energy also increases this voltage, leading to further losses across the snubber resistor.

The second loss mechanism comes from the additional capacitance added to the switching node from the RCD network, as well as needing to charge the capacitance across the RCD diode junction. These loss mechanisms are eliminated by removing the RCD snubber network.

To keep the MOSFET V_{DS} from getting too high, an additional drain-source capacitance is added across the drain node of the MOSFET. This leads to a higher C_{DS} switching loss when compared to the design with a snubber network, as shown above in red. The energy that is stored in the transformer leakage inductance gets dissipated in the high-frequency copper loss of the transformer rather than in the RCD network.

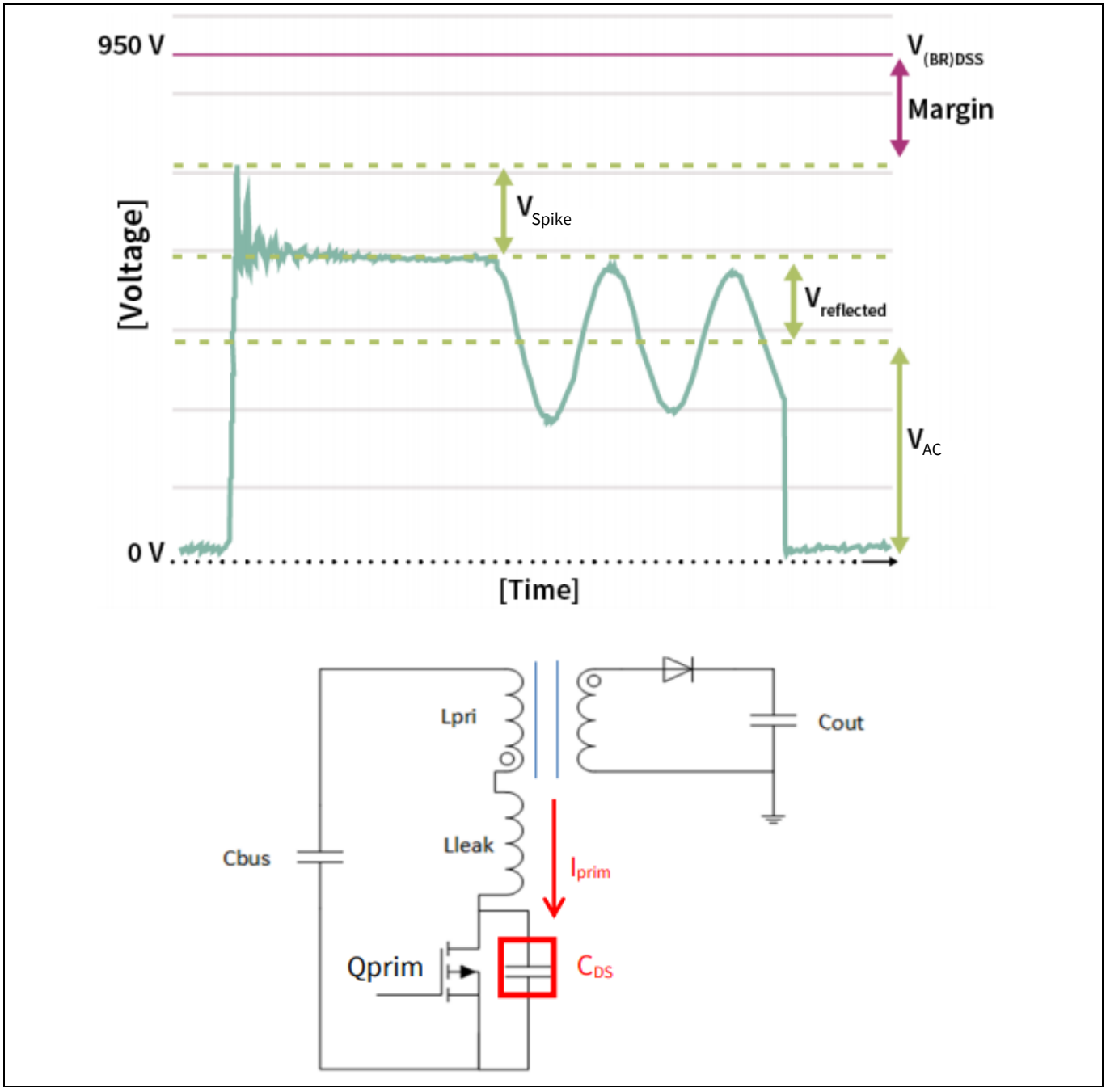

Figure 11 The MOSFET V_{DS} margin needs consideration for snubberless operation

In designing a snubberless flyback converter, it is critical to make sure the $V_{(BR)DSS}$ of the MOSFET is not exceeded. The V_{DS} of a MOSFET consists of three main sections, as shown in **Figure 29**. The V_{DS} is the total of the bus voltage (V_{AC}), the reflected voltage (V_R) and the ringing voltage (V_{SPIKE}). The ringing voltage of the MOSFET is the only portion that is affected in the transition from an RCD snubber to a snubberless design. To understand how to remove the snubber, the mechanism behind the drain-source ringing needs to be understood.

When the MOSFET is turned on in a flyback converter, the current through the primary side of the transformer begins to ramp. When the MOSFET turns off, this energy gets transferred to the secondary of the flyback converter. Not all of this energy gets transferred to the secondary, and the leakage inductance is the energy that cannot couple to the secondary. This energy then transfers to the total output capacitance of the MOSFET, which consists of the MOSFET C_{DS}, transformer parasitic capacitance, trace capacitance and any other

capacitance on the drain node. An LC ringing occurs with the period set by the C_{DS} total and the leakage. To control the peak voltage of the drain-source ringing, an external capacitance can be added in parallel to the drain source of the MOSFET. Furthermore, cold start-up sequences must be considered.

As a recommendation, a minimum of 10 percent margin should be kept from the drain-source breakdown voltage with worst-case component tolerances.

More information about the snubberless design can be found in the **950 V CoolMOS™ P7 MOSFET** application note.

3.5 CS resistor and GD pin-related design

Figure 12 shows the connections of the current sense (CS) resistor R_{CS}, gate resistor R_G and gate source resistor R_{GS}.

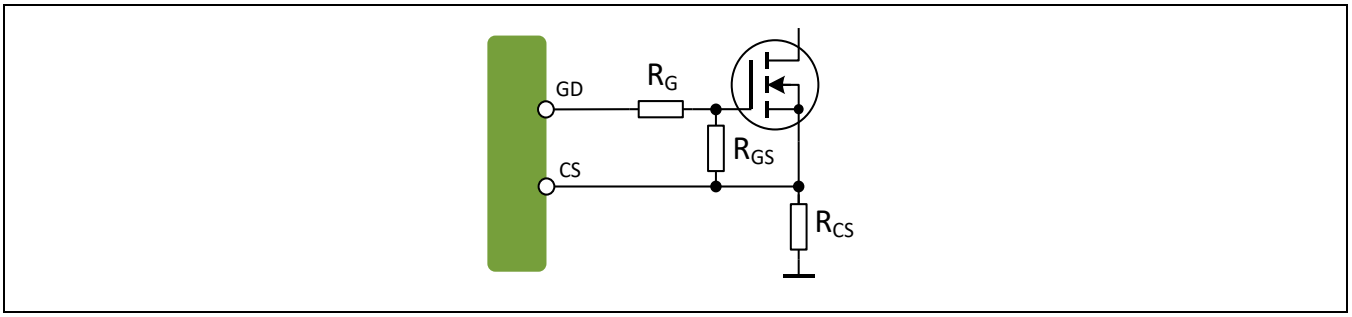

Figure 12 GD pin, CS pin, R_{CS}, R_G and R_{GS} connections

Current through the main power MOSFET is sensed across resistor R_{CS}, as illustrated above.

The recommended minimum CS resistor $R_{CS\text{-}MIN}$ based on the datasheet value $V_{OCP1\text{-}MIN}$ value is defined and calculated as:

$$R_{CS-MIN} = \frac{V_{OCP1-MIN}}{I_{PRI-MAX(PK)}} = \frac{0.57\ V}{2.605\ A} = 0.224\ \Omega \quad (49)$$

The recommended maximum CS resistor $R_{CS\text{-}MAX}$ based on the datasheet value $V_{OCP1\text{-}MIN}$ value is defined and calculated as:

$$R_{CS-MAX} = \frac{V_{OCP1-MIN}}{I_{PRI-MAX(PK)}} = \frac{0.65\ V}{2.605\ A} = 0.255\ \Omega \quad (50)$$

Based on the calculation results above, CS resistor $\boldsymbol{R_{CS} = 0.22\ \Omega}$ is selected as a starting point in this design example.

Even when not intending to use the second OVP feature described in chapter **4.1**, it is advised to connect a resistor from the CS pin to the R_{CS}. The size of the resistor should be a view 100 ohms smaller than the calculated resistor. This helps to limit the occurring voltage spikes on this pin.

After some measurements at low-line and maximum load, the value of the resistor can be adjusted to limit the primary-side current. Keep in mind that some margin to the normal full load operation has to be kept to allow a quick regulation in case of load changes.

Resistor R_G is placed in series with the main power MOSFETs' gate pin to damp the gate-rise oscillation, and R_{GS} is to ensure the MOSFET remains in an off-state when AC input is applied, with the IC not being activated yet. **R_G = 47 Ω** and **R_{GS} = 47 kΩ** are selected in this design example.

The gate-drive peak voltage $V_{GD,pk}$ is typically 11 V with sufficient V_{CC} voltage supply. To achieve a good balance of switching loss and EMI, the gate voltage rising and falling slope can be modified by using external components around the MOSFET, including the gate resistance. More information can be found in the **CoolMOS™ P7 MOSFET** application note.

With the high-speed switching characteristics of CoolMOS™ P7 MOSFET, which reduce the switching losses, it is recommended to start with a gate resistor R_G of 20 to 50 Ω.

3.6 VIN pin-related design

The rectified input voltage is sensed through an external resistor divider which consists of $R_{VINhigh}$ and R_{VINlow} at the VIN pin as shown in **Figure 13**. This input voltage sensing function enables BI and BO protection as well as input OVP and AC-DC detection.

A capacitor C_{VIN} should also be connected between the HV pin and ground in parallel to R_{VINlow}.

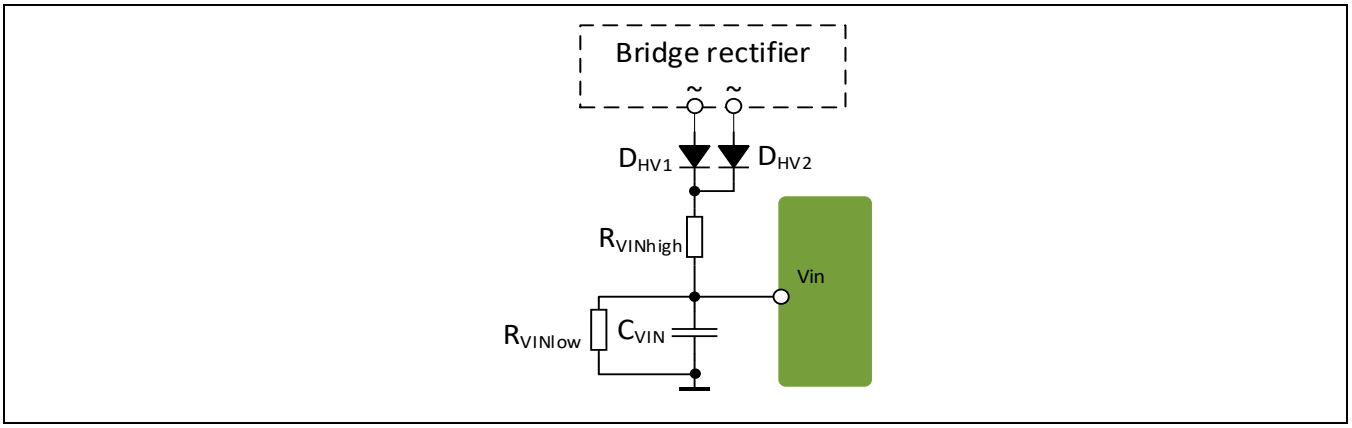

Figure 13 HV pin, $R_{VINhigh}$, R_{VINlow}, C_{VIN}, D_{HV1} and D_{HV2} connections

Brown-in – At the initial start-up (AC plug-in), the voltage at the VIN pin must exceed the 0.63 V threshold to initiate PFC start-up; this is defined as brown-in (BI).

- AC RMS line voltage at BI is defined as V_{IN_BI}.
- VIN pin BI threshold is 0.63 V, noted as V_{BI}.

Brown-out – Once the converter is operating, brown-out (BO) is detected when the voltage at the VIN pin drops below the 0.42 V threshold V_{BO}. ICL88xx stops PFC switching and enters auto restart. The normal system operation recovers if the average voltage at the VIN pin rises above V_{BI} (0.63 V).

- AC RMS line voltage at BO is defined as V_{IN_BO}.
- VIN pin BO threshold is 0.42 V, noted as V_{BO}.

Determining BI and BO voltages and sense resistor values:

1. Set BI voltage value (V_{AC-Bi} = 85 V).
2. Determine $R_{VINhigh}$ and R_{VINlow} given BI value.
3. Calculate BO voltage with $R_{VINhigh}$ and R_{VINlow} values determined from the second step.

Set the lower resistor value to 43 kΩ (R_{B02}), declare the BI threshold at 85 V AC to make sure the system starts up at 90 V AC and calculate the upper resistor value. m is a correction factor for the internal averaging.

$$R_{VINhigh} = \left(\frac{V_{AC-BI} \times m}{V_{BI}} - 1\right) \times R_{VINlow} \quad (51)$$

$$R_{VINhigh} = \left(\frac{85\ V \times 1.11}{0.63\ V} - 1\right) \times 43\ k\Omega \approx 5.8\ M\Omega$$

The calculated R_{BO1} = 5.8 MΩ is divided into three parts to reduce the voltage and power stress of the resistor (SMT 1206 size). To improve the accuracy of the measurement, resistors with tolerance of less than 1 percent should be selected.

Rearrange the previous equation and now determine the BO voltage. For BO, a different correction factor must be considered:

$$V_{AC\text{-}BO} = \frac{\left(\frac{R_{VINhigh} + R_{VINlow}}{R_{VINlow}}\right) \times V_{BO}}{n} \quad (52)$$

$$V_{AC\text{-}BO} = \frac{\left(\frac{5.8\ M\Omega + 39\ k\Omega}{39\ k\Omega}\right) \times (0.42\ V)}{0.9} = 70\ V_{RMS}$$

The BI voltage can be calculated once $R_{VINHigh}$ and R_{VINlow} are determined:

$$V_{IN\_OVP} = \frac{\left(\frac{5.8\ M\Omega}{39\ k\Omega} + 1\right) \times (2\ V)}{0.9} = 332\ V_{RMS} \quad (53)$$

The BO detection function of the ICL88xx is based on a DC voltage on the VIN pin that represents the average value of the rectified mains voltage – see **Figure 14**.

The voltage sensed at the VIN pin of the ICL88xx becomes distorted when the converter is off, or has shut down due to a protection. This voltage distortion is due to the diode bridge not conducting, and common-mode (CM) voltages from the AC main to GND being present (refer to **Figure 14**).

It results in a shifting up of the average value of the RMS rectified voltage; see “Common mode distortion” in **Figure 14**. For this reason, the VIN divider calculations need two different correction values depending on the initial mode.

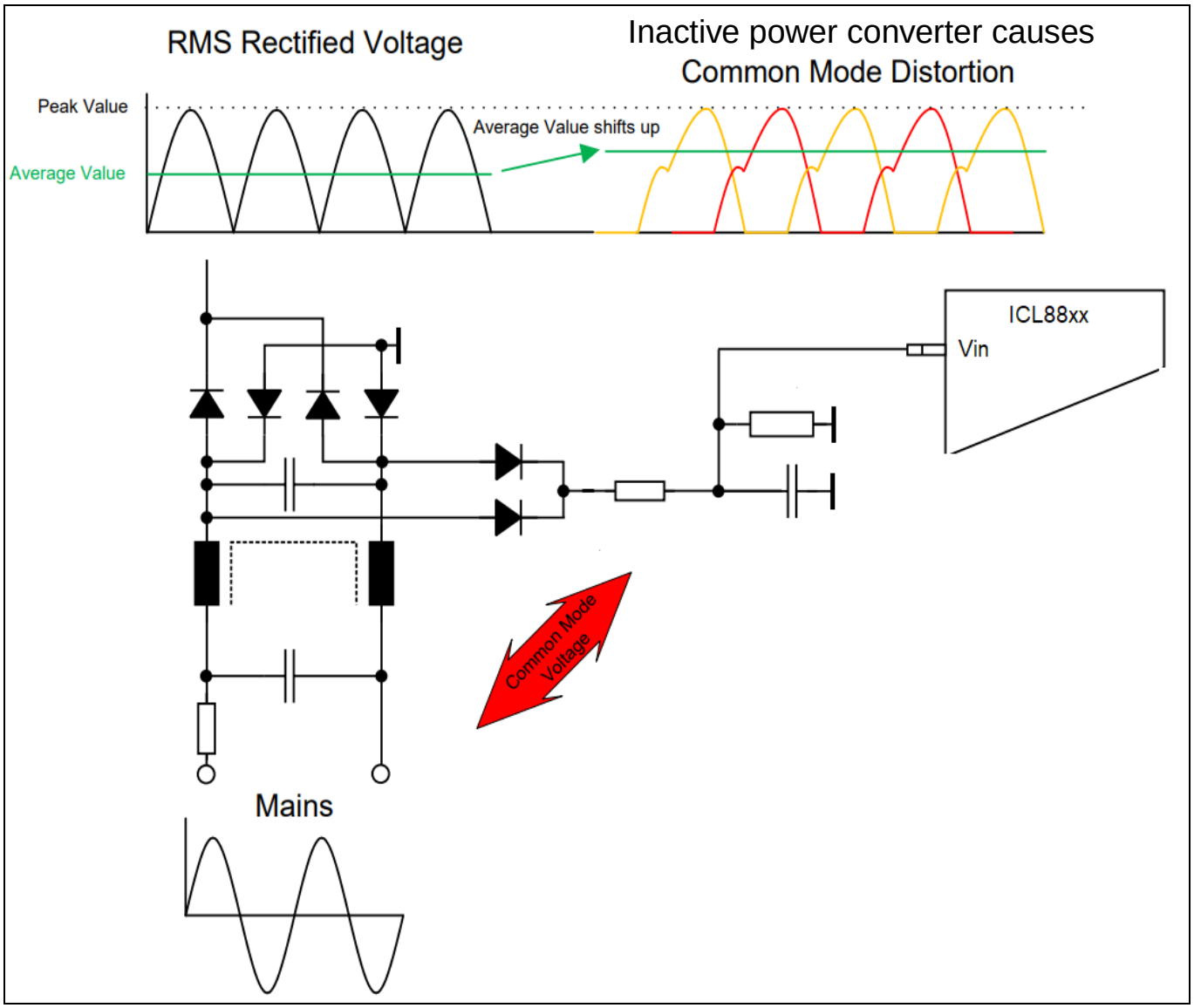

Figure 14 Impact of conducting vs. non-conducting (distortion)

AC input line sensing – A small filter capacitor needs to be placed close to the VIN pin of the ICL88xx. The value of the capacitor should be small enough to react quickly to line voltage changes and not trigger the short protection V_{VINUV} = 0.208 V, and not too large to safely detect an AC or DC voltage.

Determine VIN sense pin average voltage during the lowest AC-line operation (90 V AC):

$$V_{VIN_{AVG}} = V_{AC,min} \times n \times \frac{R_{VINlow}}{\mathrm{R_{VINhigh}} + R_{VINlow}} \quad (54)$$

$$V_{VIN_{AVG}} = 90\,V \times 0.9 \times \frac{39\,k\Omega}{5.8\,M\Omega + 39\,k\Omega} = 0.54\,V$$

$$V_{VIN_{ripple-\max}} = \left(V_{VIN_{AVG}} - V_{VIN_{UV}}\right) \times 2 = (0.540\,V - 0.208\,V) \times 2 = 0.664\,\mathrm{V} \quad (55)$$

The subtraction must be multiplied by two because the peak-to-peak value is needed.

Using the complex voltage divider, the minimum capacitor size for these resistors can now be calculated:

$$Z_{lower_{\max}} = \frac{\mathrm{R_{VINhigh}}}{\frac{4}{3 \times \pi} \times \frac{2}{V_{VIN_{ripple-\max}}} \times V_{AC-min} \times \sqrt[2]{2} - 1} = 30.8\,k\Omega \quad (56)$$

$$C_{VIN-MIN} = \left(\frac{\sqrt[2]{\frac{1}{Z^2_{lower_{\max}}} - \frac{1}{R_{VINlow}{}^2}}}{2 \times \pi \times 2 \times f_{AC}} \right) = 35.3\,nF \quad (57)$$

A maximum allowed VIN pin capacitance permissible ($C_{VIN-MAX}$) allowing for proper AC-line detection should also be calculated. This value is determined as the $C_{VIN-MIN}$ was, but now using the maximum AC-line voltage (305 V AC).

The voltage at the VIN pin V_{VINAVG} should be smaller than the V_{VINOVP} = 2 V that was the case for 305 V AC.

The worst case for ripple detection is at high-line and should be greater than 0.313 V.

The calculation results in:

$$V_{VIN_{AVG}} = V_{AC,max} \times n \times \frac{R_{VINlow}}{\mathrm{R_{VINhigh}} + R_{VINlow}} \quad (58)$$

$$V_{VIN_{AVG}} = 305\ V \times 0.9 \times \frac{39\ k\Omega}{5.8\ M\Omega + 39\ k\Omega} = 1.83\ V$$

$$V_{VIN_{ripple-\min}} = 0.313\ V \quad (59)$$

This value is an IC parameter.

Using the complex voltage divider, the maximum capacitor size for these resistors can now be calculated:

$$Z_{lower_{\min}} = \frac{\mathrm{R_{VINhigh}}}{\frac{4}{3 \times \pi} \times \frac{2}{V_{VIN_{ripple-\min}}} \times V_{AC,max} \times \sqrt[2]{2} - 1} = 4.6\ k\Omega \quad (60)$$

$$C_{VIN-max} = \left(\frac{\sqrt[2]{\frac{1}{Z^2_{lower_{\min}}} - \frac{1}{R\_VINlow^2}}}{2 \times \pi \times 2 \times f_{AC}} \right) = 262.9\ nF \quad (61)$$

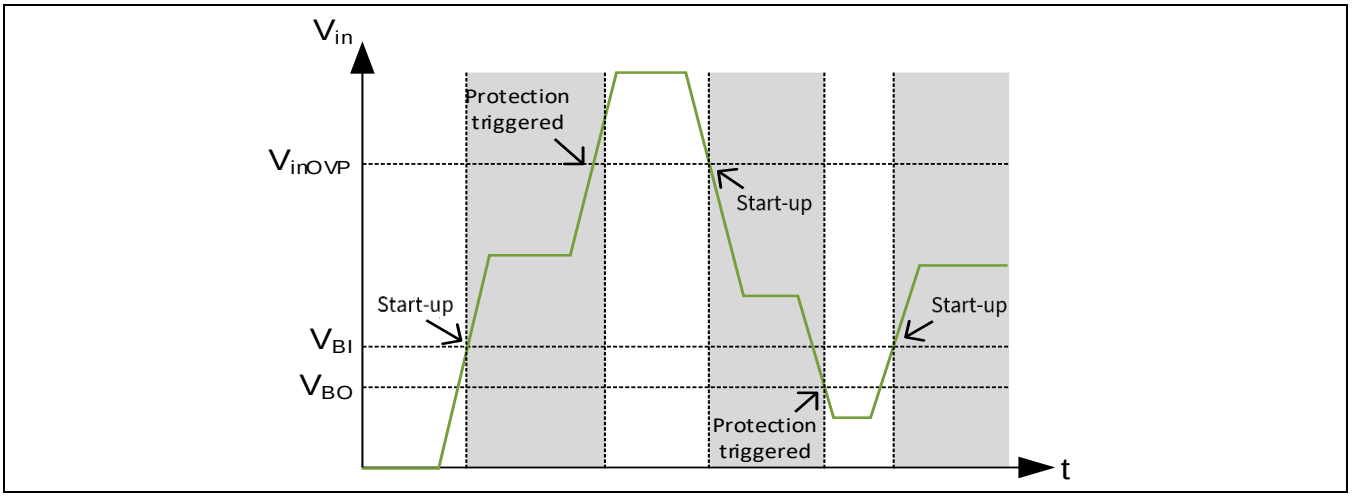

Figure 15 Input voltage levels for start-up and protection

If the capacitor is larger than the calculated value, there is the risk that the IC detects DC at high input voltages. This may cause a bad THD at PF, because the QR operation gets lost.

For ICL8820, the IC starts to introduce the jitter pattern to the otherwise constant operating frequency.

Fast restart

The VIN pin offers an additional fast restart feature. Where the normal restart takes 200 ms after a protection is triggered, the fast restart checks the start-up conditions every 25 ms as long as a V_{CC} is available.

This feature might be useful to turn the IC off for very low standby applications with additional auxiliary power supply. In this case, the response time to start-up is largely decreased from the worst-case 200 ms + start-up time to just 25 ms + start-up time.

R_{BO1} = 5.8 MΩ can be used for the first start-up of the board. Later optimization showed that a value of 6.31 MΩ is better suited to this board.

3.7 On-time adjustment

To limit the maximum power delivery at low AC-line input voltages, the ICL88xx limits the maximum on-time. This is accomplished with the resistor connecting the ZCD pin and the auxiliary winding. The on-time has a linear relationship to the current flowing in the pin, which is displayed in **Figure 16**. To get the best performance, it is advisable to design the on-time to be greater than 10 µs.

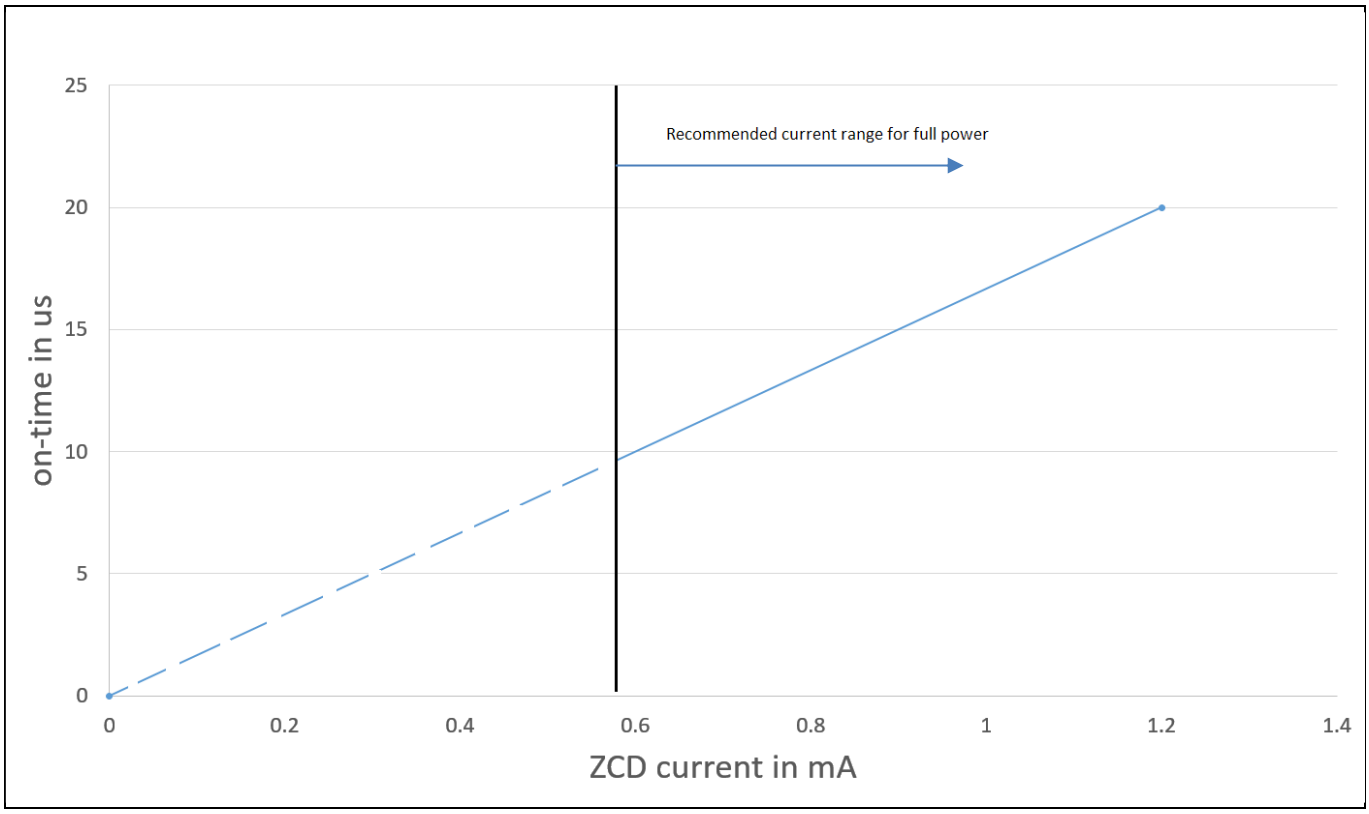

Figure 16 ZCD current vs. on-time

Maximum on-time for this design was calculated in chapter **3.1** (12.2 µs).

Where:

- $V_{ZCDClamp}$ = 55 mV
- ZCD_{coeff} = 60 A/s

According to the calculation, gate pulses with 12.2 µs are needed at 90 V and 800 mA. To generate these, the ZCD signal must have more than 0.7 mA peak-to-peak.

The aux voltage is:

$$V_{a_{pk}} \times \frac{N_{A,SEC}}{N_{prim}} = V_{auxneg} \quad (62)$$

$$V_{auxneg} = 90\,V \times \sqrt{2} \times \frac{3}{32} = 11.9\,V$$

in the negative direction, and:

$$(V_{out} + V_d) \times \frac{N_a}{N_{\text{sec}}} = V_{auxpos} \quad (63)$$

$$V_{auxpos} = (52\,V + 0.7\,V) \times \frac{3}{10} = 15.81\,V$$

in the positive direction.

The peak-to-peak voltage is 28.3 V. For a ZCD current of 0.6 mA peak-to-peak, the ZCD resistor may have a maximum of:

$$\frac{V_{auxpkpk}}{I_{ZCD}} = R_{ZCDmax} \quad (64)$$

$$R_{ZCDmax} = \frac{27.7\,V}{0.6\,mA} = 42\,k\Omega$$

Margin should be considered when setting the maximum on-time (selecting resistor R_{ZCD}). This takes into account abrupt AC-line and load changes, and ensures quick start-up.

Based on bench analysis, 15 percent margin on maximum on-time leads to good and stable results.

If resistor R_{ZCD} is selected to be too large, during certain operating conditions the output voltage may decrease enough to cause slow start-up times or possibly initiate multiple start/restart sequences.

With 15 percent margin added to the maximum on-time, the resistor is selected: R_{ZCD} = 33 kΩ.

With R_{ZCD} = 33 kΩ on the ZCD pin, there was still some reserve for the maximum pulse width.

The limit for the lowest R_{ZCD} is given by the maximum current and on-time handling capability of the ZCD pin. Inside the IC a deterioration of the THD due to too-high negative ZCD current occurs from approx. 2.5 mA; at 125°C it is approximately 1.8 mA.

At 300 V AC, the aux voltage in the negative direction is:

$$V_{AC,max,pk} \times \frac{N_a}{N_p} = V_{auxnegmax} \quad (65)$$

$$V_{auxnegmax} = 300\,V \times \sqrt{2} \times \frac{3}{32} = 39.8\,V$$

To stay below 1.8 mA, the R_{ZCD} must be at least:

$$\frac{V_{aux,pkpk}}{I_{ZCD}} = R_{ZCDmin} \quad (66)$$

For 1.8 mA:

$$R_{ZCDmin} = \frac{39.8\,V}{1.8\,mA} = 22\,k\Omega \quad (67)$$

For 2.5 mA:

$$R_{ZCDmin} = \frac{39.8\,V}{2.5\,mA} = 16\,k\Omega \quad (68)$$

Given these two conditions, the ZCD resistor may be selected without restriction between 22 kΩ and 33 kΩ.

Trade-off between power limitation and operating point

The on-time of the ICL88xx family of devices is determined by the current out of the ZCD pin and the R_{ZCD} resistor selected as described above. The R_{ZCD} value also affects the operating point of the system. To be clearer, the value of R_{ZCD} will have an effect on what valley number the converter uses to turn on the main power MOSFET.

As the value of resistor R_{ZCD} reduces, the ICL88xx moves to a higher valley number earlier. Bench analysis has shown the best trade-off between THD, power limitation and performance is achieved with a smaller R_{ZCD} than initially calculated. This is due to shorter gate pulses being avoided.

The adjustment of the resistor R_{ZCD} can be used to shift the operating point, and optimize the system for EMI compliance.

Keep in mind that the value chosen for R_{ZCD} impacts the secondary-side OVP value. Increasing the current out of the ZCD pin of the ICL88xx reduces the magnitude of the voltage where the OVP is triggered. The process of optimizing R_{ZCD} while setting the OVP value will be covered later.

Final optimization of R_{ZCD} considering start-up, load transient and OVP: 26 kΩ.

3.8 V_{CC} capacitance and output UVP design

When AC power is first applied to the system, the ICL88xx V_{CC} capacitors must charge to a minimum voltage threshold and have enough energy storage to allow the ICL88xx to start switching.

The ICL88xx V_{CC} start-up circuitry can be created by a variety of methods depending on requirements. The simplest of methods is to place resistor(s) in series from the rectified AC mains to the ICL88xx V_{CC} pin.

A more common approach is to create an external start-up circuit that optimizes start-up time, efficiency and cost.

The resistive start-up can be used for narrow voltage range designs or when the standby power is not a concern (on-off power supply). For wide-range designs and for the lowest standby power, external start-up circuitry is recommended.

The following high-voltage start-up circuit is prepared within the 43 W evaluation design, and its operation is described below.

The start-up circuit can be designed as illustrated in **Figure 17**:

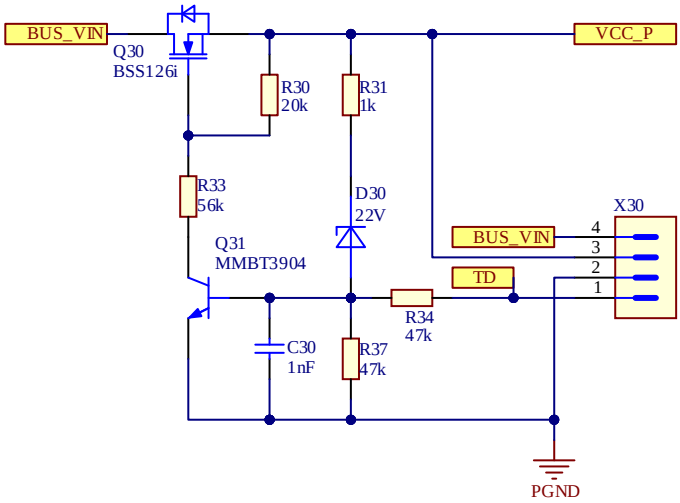

Figure 17 V_{CC} power supply from start-up circuit

The start-up circuit is connected to the rectified AC input after the bridge rectifier via the current limitation resistors R_{Vcc} in **Figure 1**. These resistors also limit the voltage drop over the depletion MOSFET BSS126i during the on-state, which is selected so that the V_{CC} charge occurs automatically.

First, the necessary minimum start-up capacitance needs to be calculated:

$$C_{VCC-MIN} = \frac{I_{CC} \times t_{START}}{V_{DROP}} = \frac{2\,mA \times 50\,ms}{5\,V} = 20\,\mu F \quad (69)$$

Where I_{CC} is the self-supply of the IC, $t_{start,self}$ is the estimated time until the self-supply is available at the auxiliary winding and V_{drop} is the minimum voltage drop that can occur from the start-up of the IC until the V_{CCmin} with the UVP.

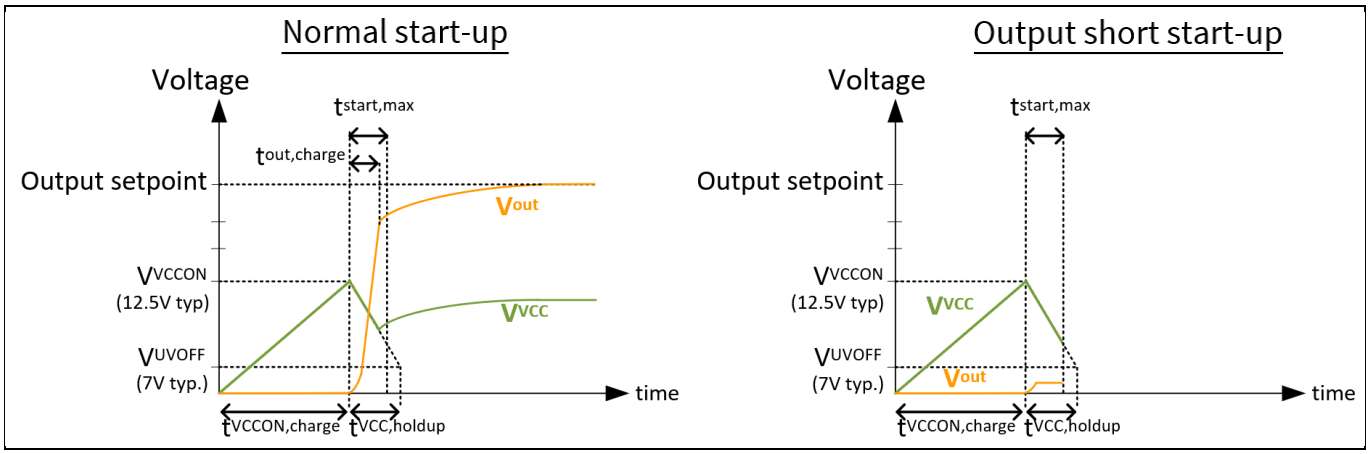

Figure 18 Start-up behavior

Once V_{VCCON} voltage is seen at the VIN pin, the ICL88xx starts to switch.

C_{VCCmin} is highly dependent on the $t_{start,self}$, which is just an assumption here. The capacitor value can later be further optimized to be sufficiently large to perform the start-up and function correctly during burst mode (only available with ICL8810 and ICL8820).

If the capacitor C_{VCC} is too small, the system continuously restarts. Each time the system is restarted, the output capacitor is charged a bit more until the system can fully start up and operate properly.

A too-large capacitor needs more time to charge. This might conflict with the time-to-light requirement. It is advisable to use a capacitor close to the necessary minimum value.

In case of an output short condition, the V_{CC} is not supplied over the auxiliary winding, since all the power flows to the shorted output. This behavior is displayed in **Figure 15**.

It is recommended to design the V_{CC} auxiliary turns ratio to reduce V_{CC} below 7 V (UVLO) to ensure the system shuts down during output conditions where the voltage reduces below its specified operating range. This ensures the main power MOSFET isn't being switched on while in its saturated operating region.

The V_{CC} charge current is limited by resistors R_{Vcc}, which are connected between the output of the diode bridge and the start-up circuit. The converter start-up time can be set by the values of these three resistors, and the size of the V_{CC} capacitor. Assuming the required system time-to-light is 300 ms, V_{CC} capacitor is 22 µF, PFC flyback and second-stage start-up time are each 50 ms, the minimum input voltage is 90 V AC and the turn on threshold is V_{VCCON} = 13 V the minimum charge current can be calculated as:

$$I_{Vcc\_charge\_min} = C_{Vcc} \times \frac{V_{Vcc\_on\_max}}{t_{time_{to_{light}}} - t_{PFC_{start}} - t_{HB_{start}}} \quad (70)$$

$$I_{Vcc\_charge\_min} = 22\ \text{uF} \times \frac{13\ V}{300\ \text{ms} - 50\ \text{ms} - 50\ \text{ms}} = 1.43\ mA$$

To ensure that this charge current can be provided at AC low-line, the maximum start-up current limitation resistor value is calculated as:

$$R_{HV} = \frac{\sqrt{2} \times V_{AC,min,rms}}{I_{Vcc\_charge\_min}} \quad (71)$$

$$R_{HV} = \frac{\sqrt{2} \times 90\ V_{RMS}}{1.43\ mA} = 89\ \text{k}\Omega$$

And the maximum charge current at high-line input is:

$$I_{Vcc\_charge\_max} = \frac{\sqrt{2} \times V_{AC,max,rms}}{R_{HV}} \quad (72)$$

$$I_{Vcc\_charge\_max} = \frac{\sqrt{2} \times 305\ V_{RMS}}{89\ \text{k}\Omega} = 4.85\ mA$$

The charging time can be calculated as:

$$V_{Vccon} \times \frac{C_{Vcc}}{I_{Vcc_{charge_{min}}}} = V_{Vccon} \times \frac{C_{Vcc}}{\left(\frac{V_{ACpk} - V_{VccON}}{R_{startup}}\right)} = t_{charge} \quad (73)$$

$$t_{charge} = \frac{13\ V \times 22\ uF}{\frac{90\ V \times \sqrt{2} - 13\ V}{89\ k\Omega}} = 222\ ms$$

It is recommended to split the R_{Vcc} into three series-connected resistors (R3, R4 and R5) to minimize the power and voltage stress of each current limitation resistor and the BSS126i.

To fulfill the Energy Star time-to-light requirement of 500 ms, the V_{CC} voltage maximum charging time for IC activation, t_{START} should not exceed 350 ms. Therefore, the maximum V_{CC} capacitance $C_{VCC,MAX}$ can be defined and calculated as:

$$C_{VCC,max} = \frac{V_{AC,120(rect,avg)} - V_{VCC-ON}}{R_{HV} \times V_{VCC-ON}} \times t_{START} \times \left[1 - \frac{2}{\pi} \times sin^{-1}\left(\frac{V_{VCC-ON}}{V_{AC,120(pk)}}\right)\right] \quad (74)$$

Where V_{VCCON} is the maximum V_{CC} turn-on threshold of 13 V, $V_{AC,120(AVG)}$ is the average value of rectified 120 V_{RMS} AC input, and $V_{AC,120(pk)}$ is the peak value of 120 V_{RMS} AC input.

$$C_{VCC,max} = \frac{0.9 \times 120\,V - 13\,V}{89 \times 10^3\,\Omega \times 13\,V} \times 350 \times 10^{-3} \times \left[1 - \frac{2}{\pi} \times sin^{-1}\left(\frac{13\,V}{\sqrt{2} \times 120\,V}\right)\right] = 43\,\mu F \quad (75)$$

$t_{START-SYS}$ refers to the maximum system start-up time. $t_{START-SYS}$ consists of the soft-start phase and output charging phase. It can be indirectly configured with V_{CC} capacitance parameter C_{VCC}, based on:

$$t_{START-SYS} = \frac{0.8 \times C_{VCC} \times (V_{VCC-ON} - V_{UV-OFF})}{I_{IC,avg,est}} = \frac{0.8 \times C_{VCC} \times (12-7)V}{2 \times 10^{-3}A} = 2000 \times C_{VCC} \quad (76)$$

Where V_{VCCON} is the typical V_{CC} turn-on voltage threshold of 12 V, V_{UV-OFF} is the typical V_{CC} turn-off voltage threshold of 7 V and I_{IC-AVG} is the typical IC current consumption (2 mA).

For proper start-up, C_{VCC} capacitance has to be large enough to ensure its corresponding $t_{START-MAX}$ calculated from equation (76) is greater than $t_{OUT-CHARGE}$, where $t_{OUT-CHARGE}$ is the time needed to charge the output voltage to the start-up output UVP level $V_{OUT-UV-START}$ or greater.

Based on the considerations above, the V_{CC} capacitor value of **C_{VCC} = 22 µF** is selected in this design example, which results in $t_{START-MAX}$ = 44 ms. In addition, a noise-decoupling ceramic capacitor of **C_{VCC-DC} = 0.1 µF** with low ESR is added in parallel to C_{VCC}.

Also ensure that the maximum power limit of the BSS126i is not violated.

After testing the values for capacitance and start-up, resistors can be further optimized.

Resistive start-up

In cases where the standby losses do not matter or a narrow AC-line voltage is certain, this is a very cost effective solution to charge the V_{CC} capacitor.

Following is a design example of how to calculate all the relevant values for this circuit. Assuming that the input voltage is 230 V with 10 percent tolerance, the minimum and maximum input voltages would be 207 V and 253 V.

The minimum size of the V_{CC} capacitor is calculated as above and results in a 22 µF capacitor.

From the above calculation, it can be seen that 89 kΩ is required to achieve a short start-up time.

Based on Ohm's law, there are the following results:

$$\left(V_{ACpk} - V_{VccON}\right) \times I = \frac{\left(V_{ACpk} - V_{VccON}\right)^2}{R_{startup}} = P_{losses} \quad (77)$$

$$P_{losses} = \frac{\left(253\ V \times \sqrt{2} - 13\ V\right)^2}{89\ k\Omega} = 1.4\ W$$

The losses within the circuit are at the maximum when the AC-line voltage is greatest.

Because these losses are always present, during both commissioning and operation, it must be considered whether this performance is acceptable for the system.

By increasing the resistor to 200 kΩ, the losses can be calculated as 630 mW, which looks more appealing. To decide whether this is acceptable, the charge time must be calculated:

$$V_{Vccon} \times \frac{C_{Vcc}}{I} = \frac{V_{Vccon} \times C_{Vcc}}{\left(\frac{V_{ACpk} - V_{VccON}}{R_{startup}}\right)} = t_{charge} \quad (78)$$

$$t_{charge} = \frac{13\ V \times 22\ uF}{\frac{207\ V \times \sqrt{2} - 13\ V}{200\ k\Omega}} = 208\ ms$$

For the charging time the lowest input voltage has to be used, as in this case the charging current is also the smallest.

For this example, with an input voltage of 230 V +/-10 percent, a 200 kΩ charging resistor can be used, which would always create 630 mW of losses, but has an acceptable charging time of 208 ms (for time-to-light the start-up time for the first and second stage has to be added).

4 THD optimization

The input AC current becomes most distorted in the area where the AC voltage is near zero (zero-crossing).

To reduce distortion of the AC current in this area, the ICL88xx extends the PFC MOSFET on-time during this period. The PFC MOSFET on-time is allowed to increase up to two times the maximum on-time according to the instantaneous value of the input voltage amplitude during zero-crossing.

The detection of AC input voltage zero-crossings is realized through the PFC auxiliary winding.

The concept of THD correction is shown in **Figure 19**.

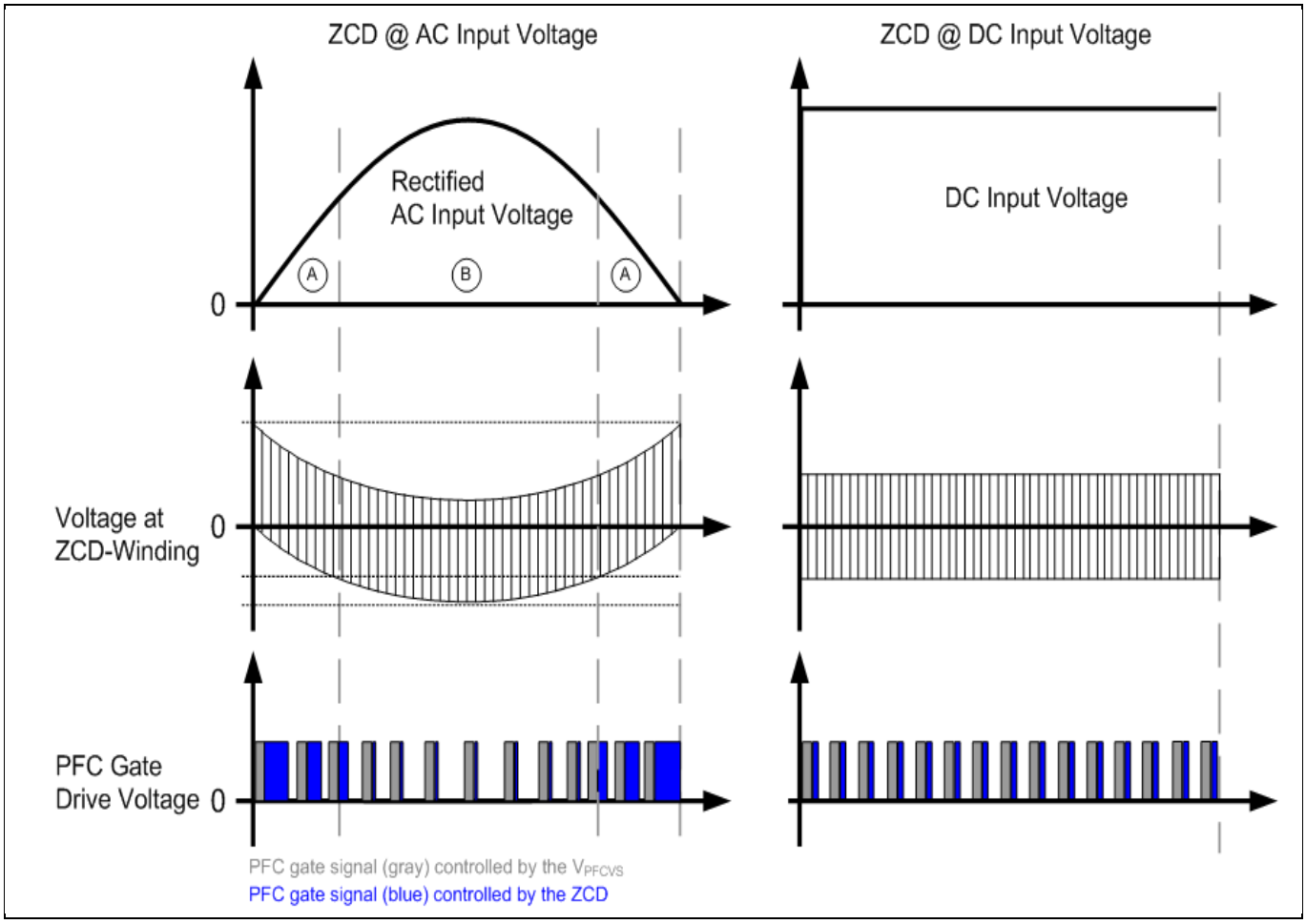

Figure 19 PFC THD correction

Extending the on-time during ZCD is accomplished by an external resistor connected to the TD pin. During low input voltage levels, the on-time of the MOSFET is increased to minimize gaps in the line current during zero crossing of the line voltage and to improve the THD of the input current. This THD correction is set with the TD resistor.

The voltage on the TD pin (2.15 V or a 68 kΩ resistor from TD to ground) is measured at start-up and is internally multiplied with the measured I_{ZCD} current. The result is handed over to the pulse-generation block inside the IC to create the optimized waveform.

In rare cases (small transformer inductance and small capacitor output capacitance which results in a high oscillation frequency), a lower-value resistor down to 27 kΩ might result in a better THD performance.

TD resistor with proposed start-up circuit

The primary function of the TD pin on the ICL88xx is to optimize THD over the AC-line and output load. The TD pin can be used as a signal that input voltage is applied to the circuit, and start-up should initiate. This signal is sensed and used to apply the V_{CC} start-up circuit. Below is a brief description of the circuit, its operation and calculation of components.

If the TD pin is used to control the start-up circuit during operation and in burst mode, special care must be taken when designing the circuitry around the TD pin.

The basis for this calculation is the TD resistor shown above. In addition, the voltage at the TD pin must be measured with the ideal resistor.

The measured TD voltage in this example is 2.10 V with a 68 kΩ resistor. The BJT has a base emitter voltage of 0.7 V, which leads to the calculation of the new TD resistor R34:

$$R_{TDupper} = \frac{V_{TDmeasured} - V_{BE}}{\frac{V_{TDmeasured}}{R_{TD}}} = \frac{2.1\,V - 0.7\,V}{\frac{2.1\,V}{68\,k\Omega}} = 47\,k\Omega \quad (79)$$

Because the BJT is used only as a switch, as much current as possible should be sent through its base. For this purpose, set this resistor to be highly ohmic, for example 47 kΩ or higher.

The voltage of the Zener diode is selected to be higher than the start-up voltage and higher than the normal operation voltage provided by the aux winding. It should be lower than the maximum voltage of the IC, which is 25 V.

In this way, it securely turns off the start-up circuit and does not waste power during normal operation.

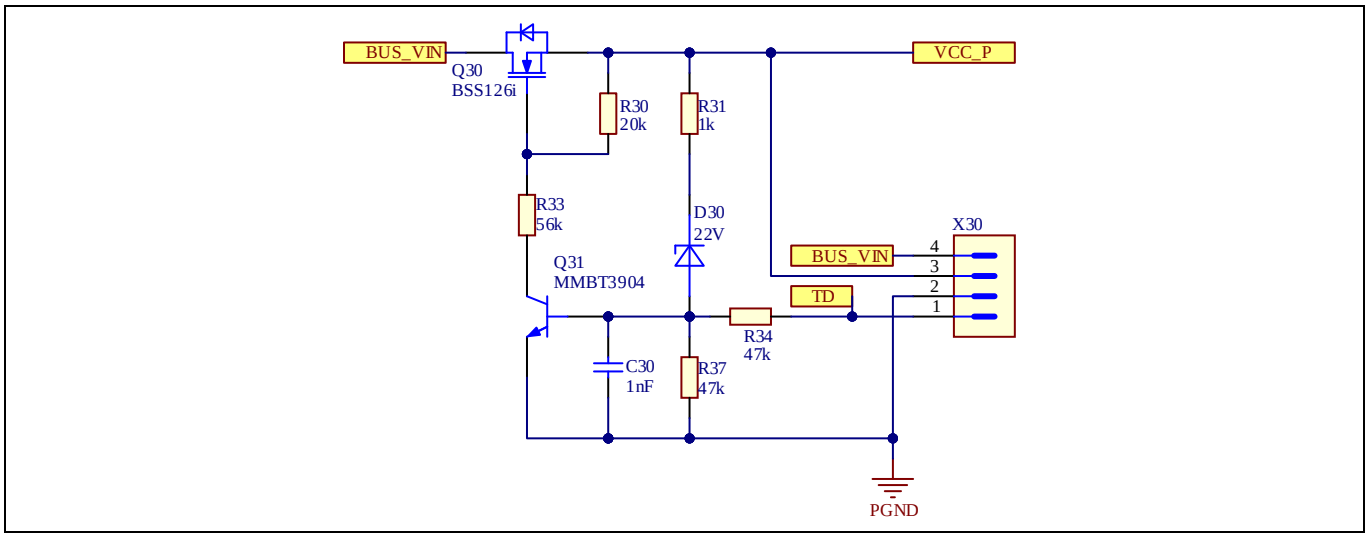

Figure 20 Start-up circuit without HV resistors connecting BUS_VIN with the input capacitor after the bridge

4.1 Output OVP-related design

Under a single-fault condition, where the feedback pin of the ICL88xx is open, the main output voltage would quickly rise above $V_{OUT-SET}$. The output OVP would be triggered when the ZCD pin estimated output voltage V_{OUT} is higher than the output OVP threshold.

During this fault condition, the ICL88xx relies on the current flowing through the ZCD pin during the demagnetization stage. This current information is sensed and internally multiplied with a factor of n_{ZCDOVP} = 0.484. An internal current source injects this current out of the CS pin during the demagnetization time. If the voltage through the additional series CS resistance reaches the V_{OCP1} = 0.61 V, a restart of the system is initiated.

The resulting waveforms associated with the OVP detection can be seen in **Figure 21**.

The top three waveforms display the voltage on the auxiliary winding, the gate drive voltage, and the voltage across the shunt resistor. The next two waveforms display the internal ZCD current signal and the resulting voltage at the CS pin. The sampling window for the OVP is shown in the next graph, and the resulting triggering when crossing the 0.61 V level.

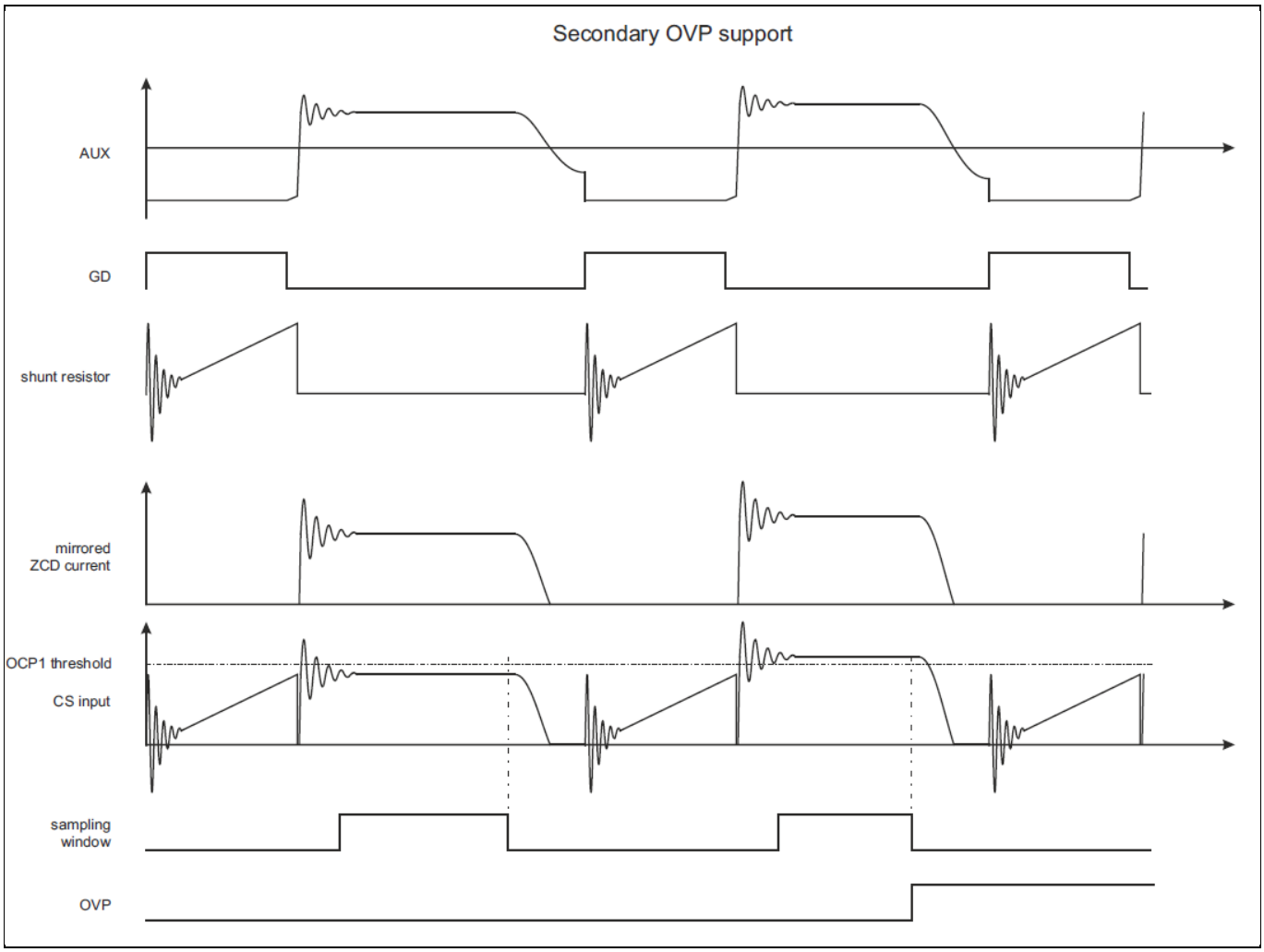

Figure 21 Waveform of the CS pin with mirrored secondary-side voltage on the CS pin during demagnetization

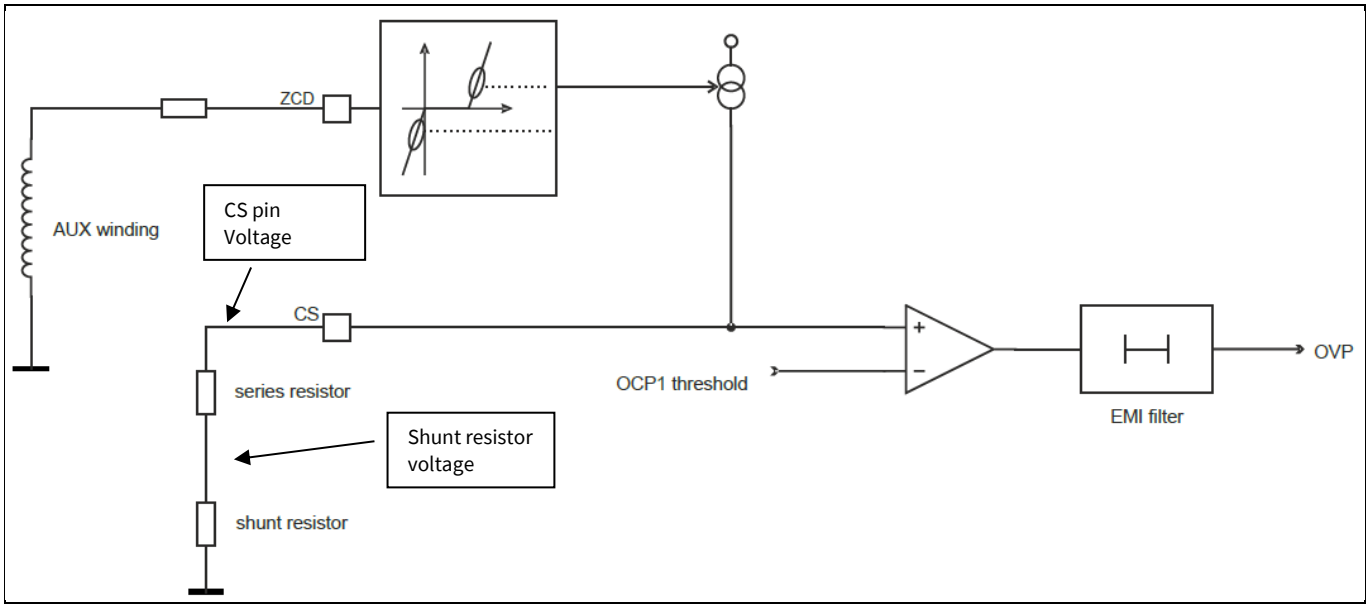

Figure 22 Internal function blocks and external circuit for the secondary-side OVP

To calculate the overvoltage sense resistor ($R_{CS\text{-}OVCP}$), the output OVP threshold is first determined. This design sets the OVP voltage at:

V_{outOVP} = 60 V

The current during the off-time of the MOSFET is calculated as follows with an added tolerance of 5 percent and $n_{aux} = N_{sec}/N_A$:

$$I_{ZCD-OVP} = \frac{\frac{1}{n_{aux}} \times V_{outovp} \times 1.05}{R_{ZCD}} \quad (80)$$

$$I_{ZCD-OVP} = \frac{\frac{1}{3{,}33} \times 60\,V \times 1.05}{33\,k\Omega} = 572\,\mu A$$

Next, the current out of the CS pin is calculated:

$$I_{CS-OVP} = I_{ZCD,OVP} \times n_{ZCD,OVP} = 572\,\mu A \times 0.484 = 277\,\mu A \quad (81)$$

Now the required series resistor is calculated as:

$$R_{CS-OVP} = \frac{V_{OCP1}}{I_{CS,OVP}} = \frac{0.61\ V}{277\ \mu A} = 2.2\ k\Omega \quad (82)$$

This resistor should be optimized as one of the last components. Since the output voltage, the ZCD resistor and the winding ratio are required for the definition of the value, the OVP can be easily triggered by accident.

It is recommended to keep the value low until all the other parameters are set. Only then will the adjustment of the secondary-side OVP generate a satisfying result.

Even when not intending to use the second OVP feature, it is advised to connect this resistor. The size of the resistor should be a view 100 Ohms smaller than the calculated resistor. This helps to limit the occurring voltage spikes on this pin.

5 Secondary-side regulation feedback circuit design

The feedback pin (VS) filter capacitor C_{VS}, optocoupler and the SSR FB circuit are configured as shown in **Figure 23**.

The VS pin does not need any external pull-up, as ICL88xx has a fixed voltage reference V_{REF} of 1.6 V, which is internally connected over a 500 Ω resistor to its VS pin.

To function properly in the SSR topology, a resistor R_{VS} has to be placed from the VS to GND. During start-up the IC checks the current flowing out of this pin. For SSR flyback, the resistor must draw about 102 µA, resulting in R_{VS} of about 12 kΩ with some buffer for the optocoupler dark current.

The ICL88xx is controlling its on-time and frequency based on the current out of this pin. The limit for maximum power is the minimum ADC current $I_{VSADCmin}$. Because there is already current flowing through the R_{VS} resistor we need to subtract the value from the datasheet value of 166 µA, resulting in 64 µA running through the optocoupler at full load. The highest current through the optocoupler defines the smallest operating point. Here the R_{VS} current must be subtracted from the maximum ADC current $I_{VSADCmax}$, which results in 618 µA.

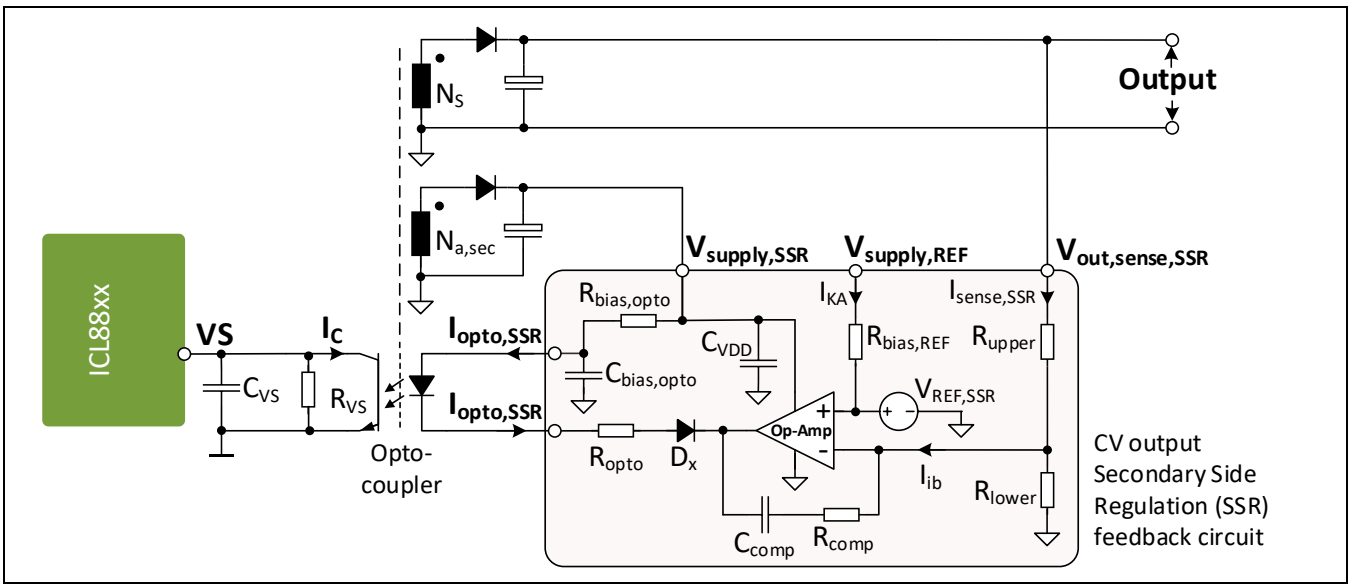

Figure 23 VS pin, C_{VS}, optocoupler and CV output SSR FB circuit connections

Power for circuitry on the secondary side is provided by supply $V_{SUPPLY-SSR}$. This includes SSR circuit op-amp operational voltage V_{DD} and optocoupler LED current $I_{OPTO-SSR}$ via resistor $R_{BIAS-OPTO}$.

For $V_{SUPPLY-SSR}$ noise decoupling a ceramic capacitor of **C_{VDD} = 100 nF** with low ESR is placed near the op-amp V_{DD} pin.

As shown in **Figure 23**, the SSR op-amp non-inverting input should be connected to the SSR reference voltage $V_{REF-SSR}$, while the inverting input should be connected to a resistor/divider formed by R_{UPPER} and R_{LOWER} for output voltage sensing. In this design example, the selected op-amp part number is TSM103W, which has dual op-amps, and the non-inverting input is internally set at 2.5 V.

$V_{SUPPLY-SSR}$ can be used as the SSR voltage reference supply $V_{SUPPLY-REF}$, to provide a minimum biasing current of I_{KA-MIN} via voltage reference biasing resistor $R_{BIAS-REF}$, for generating the $V_{REF-SSR}$.

This design example applies a voltage from a second auxiliary circuit with a lower output voltage. This reduces standby losses.

- $N_{AUX1} = 3$
- $N_{AUX2} = 2$

The voltage reference biasing resistance $R_{BIAS-REF-MAX}$ is defined and calculated as:

$$R_{BIAS-REF-MAX} = \frac{g}{I_{KA-MIN}} \times \left[(V_{OUT} + V_D) \times \left(N_{A,sec}/N_s\right) - V_{D-AUX} - V_{REF-SSR}\right] \quad (83)$$

Where g is the ratio recommended to be between 0.75 and 0.85, and V_{D-AUX} is the auxiliary output diode forward voltage.

Taking g = 0.8, V_{D-AUX} = 0.5 V and I_{KA-MIN} = 1 mA based on the selected op-amp datasheet:

$$R_{bias,REF,max} = \frac{0.8}{1 \cdot 10^{-3} A} \times [(52\,V + 0.7) \times (2/10) - 0.5\,V - 2.5] = 6.032\,k\Omega \quad (84)$$

Based on the above, $\boldsymbol{R_{BIAS-REF}}$ **= 6.2 kΩ** is selected in this design example.

To achieve accurate output voltage regulation, the op-amp input biasing current I_{IB} has to be much smaller than the output sensing upper resistor/divider current $I_{SENSE-SSR}$.

Compared to using the conventional shunt regulator TL431, which has a maximum reference input current of 4 µA, the selected op-amp has a maximum input bias current of I_{IB-MAX} = 0.2 µA. This results in much lower regulation offset error $ERR_{OFFSET-IB}$ with the same level of $I_{SENSE-SSR}$.

Considering that $ERR_{OFFSET-IB}$ is desired to be not more than 0.1 percent in this design example, the maximum output sensing upper divider resistance $R_{UPPER-MAX}$ can be defined and calculated as:

$$R_{UPPER-MAX} = \frac{ERR_{OFFSET-IB} \times (V_{OUT} - V_{REF})}{I_{IB-MAX}} = \frac{0.1\% \times (54\,V - 2.5\,V)}{0.2 \cdot 10^{-6} A} = 257.5\,k\Omega \quad (85)$$

Because the burst frequency is fixed based on the f_{BURST} = 200 Hz for low audible noise. To achieve stable main output voltage at no load, the R_{UPPER} selection should also ensure the output sensing resistor/divider power consumption is at least the power transfer of a single pulse. Therefore, the $R_{UPPER-MAX}$ value can also be defined and calculated as:

$$R_{UPPER-MAX} = \frac{L_p \times V_{OUT} \times (V_{OUT} - V_{REF})}{(V\_AC)^2 \times (t_{ON-MIN-BM})^2 \times f_{burst} \times \eta_{BM}} \quad (86)$$

Where t_{ON-MIN} is the burst mode minimum on-time parameter and η_{BM} is the estimated power efficiency in burst mode.

Take f_{BURST} = 200 Hz, t_{ON-MIN} = 715 ns and assume η_{BM} = 65 percent:

$$R_{UPPER-MAX} = \frac{544 \times 10^{-6}\,H \times 52\,V \times (52\,V - 2.5\,V)}{300^2\,V \times (0.715 \times 10^{-6}s)^2 \times 200\,Hz \times 0.65} = 234\,k\Omega \quad (87)$$

Using the calculated $R_{UPPER-MAX}$ calculated from equations (85) and (86), the output sensing upper resistance R_{UPPER} should be selected near to $R_{UPPER-MAX}$ = 240 kΩ to achieve low standby power.

$\boldsymbol{R_{UPPER} = 240\ k\Omega}$ is selected in this design example.

The output sensing lower divider resistance R_{LOWER} can then be defined and calculated as:

$$R_{lower} = \frac{R_{UPPER} \times V_{REF}}{V_{OUT} - V_{REF}} = \frac{240 \times 10^3\ \Omega \times 2.5\ V}{52\ V - 2.5\ V} = \boldsymbol{12.2\ k\Omega} \quad (88)$$

$\boldsymbol{R_{LOWER} \approx 12.2\ k\Omega}$

The FB pin capacitor C_{FB} is optional and is used to filter the converter switching noise from disturbing the regulation set-point. The averaging nature of the VS pin already helps to eliminate most of the noise.

The frequency of the noise can be up to a few MHz and the ADC sampling frequency $f_{SAMPLING-ADC}$ is around 3.9 kHz. The RC filter frequency f_{RC-FB} formed by C_{FB} and $R_{FB-PULLUP}$ is recommended to be in the range of 200 kHz to 400 kHz.

C_{FB} value is defined and calculated as:

$$C_{FB} = \frac{1}{2 \times \pi \times R_{FB-PULLUP} \times f_{RC,FB}} \quad (89)$$

Taking $f_{RC,FB}$ = 300 kHz:

$$C_{FB} = \frac{1}{2 \times \pi \times 500\ \Omega \times 300 \times 10^3\ Hz} = 1\ \text{nF} \quad (90)$$

C_{FB} = 470 pF is selected in this design example. It is recommended to limit the capacitance on this pin to 1 nF in order to not compromise the excellent burst mode regulation, due to a too-long charging time of that capacitor after wake-up.

The minimum power transfer of the system is reached when the filtered VS current level I_{VS} is the same as or more than $I_{VS,max}$. Therefore it is recommended to configure the maximum FB current $I_{FB,max}$ the same as the lowest possible VS voltage level of 1.2 V.

Based on the minimum current transfer ratio CTR_{min} from the selected optocoupler datasheet, the total resistance of $R_{bias,opto}$ and R_{opto} can be defined as:

$$R_{bias,opto} + R_{opto} \leq h \times CTR_{min} \times \left[\frac{(V_{out} + V_d) \times N_{a,sec}/N_s - V_{d,aux} - V_{f,opto} - V_{dx}}{(I_{VSADCmax} - I_{VSADCmin})}\right] \quad (91)$$

h is the ratio recommended to be between 0.7 and 0.8 for compensating the secondary auxiliary winding rectified output voltage drop under no load at the main output, $V_{f,opto}$ is the optocoupler LED forward voltage, and R_{opto} and V_{dx} are respectively the optocoupler series resistance and the forward voltage of D_x, as shown in **Figure 23**.

The ICL88xx monitors current sourced from the VS pin to regulate the system. The regulation range needs to be set within the minimum and maximum operating currents available from the IC ($I_{VSADCmax}$ and $I_{VSADCmin}$).

$I_{VSADCmax}$ and $I_{VSADCmin}$ values are obtained from the ICL88xx datasheet. Taking CTR_{min} = 100 percent, h = 0.7, $V_{f,opto}$ = 1.1 V and V_{dx} = 0.5 V for the calculation:

$$R_{bias,opto} + R_{opto} \leq 0.7 \times 100\% \times \left[\frac{(52 + 0.7) \times 2/10 - 0.5 - 1.1 - 0.5}{(610\ uA - 210\ uA)}\right] \quad (92)$$

$$R_{bias,opto} + R_{opto} \leq 14.77\ k\Omega$$

Based on the above, $R_{bias,opto} + R_{opto}$ = 10.7 kΩ is selected in this design example. Here the minimum operational current of the optocoupler needs to be considered too. $R_{bias,opto}$ is recommended to be around 10 times lower than R_{opto}, so $R_{bias,opto,max}$, which denotes the maximum $R_{bias,opto}$ value, can then be defined and calculated as:

$$R_{bias,opto,max} = \frac{R_{bias,opto} + R_{opto}}{10} = 1\ k\Omega \quad (93)$$

The recommended maximum RC filter frequency $f_{RC,bias,opto,max}$ formed by $R_{bias,opto}$ and $C_{bias,opto}$ is 40 Hz. Since $R_{bias,opto}$ with high resistance is generally cheaper than $C_{bias,opto}$ with high capacitance, $C_{bias,opto}$ nominal value is recommended not to exceed 4.7 µF. As a result, in this design example, **$C_{bias,opto}$ = 3.3 µF** is selected, while the minimum optocoupler biasing resistor value $R_{bias,opto,min}$ can be defined and calculated as:

$$R_{bias,opto,min} = \frac{1}{2 \times \pi \times C_{FB} \times f_{filter}} = \frac{1}{2 \times \pi \times 3.3 \times 10^{-6} \times 40} = 1.2\ k\Omega \quad (94)$$

Based on the $R_{bias,opto,max}$ and $R_{bias,opto,min}$ calculation results, and also $R_{bias,opto}$ + $\boldsymbol{R}_{opto}$ selection above, $\boldsymbol{R_{bias,opto}}$ = 1 kΩ and $\boldsymbol{R_{opto}}$ = 9.1 kΩ are selected in this design example. As here the current through the opto-diode is very small, a proper optocoupler has to be selected.

Feedback loop design

A type II feedback compensation network is used in this design example. It consists of a resistor R_{comp} in series with C_{comp}, as shown in **Figure 23**. It is common practice to place the frequency of the pole at origin $f_{pole,origin}$ 1 Hz to 3 Hz, while the initial frequency of the zero f_{zero} is suggested to be around 60 Hz. As a result, the initial value of C_{comp} and R_{comp} for system powering-up can be defined and calculated as:

$$C_{comp} = \frac{1}{2 \times \pi \times R_{upper} \times f_{pole,origin}} \quad (95)$$

$$R_{comp} = \frac{1}{2 \times \pi \times C_{comp} \times f_{zero}} \quad (96)$$

Taking $f_{pole,origin}$ = 1.3 Hz and f_{zero} = 60 Hz:

$$C_{comp} = \frac{1}{2 \times \pi \times 252 \times 10^3 \times 1.3} = 485\ \text{nF} \quad (97)$$

$$\boldsymbol{Initial\ C_{comp} = 470\ nF}$$

$$R_{comp} = \frac{1}{2 \times \pi \times 470 \times 10^{-9} \times 60} \quad (98)$$

$$\boldsymbol{Initial\ R_{comp} = 5.6\ k\Omega}$$

Attention: *After initial testing of the calculated feedback loop, it is advisable to measure the system's loop compensation with DC input.*

6 PCB layout guide

a) Minimize the circumference of the following high-current/high-frequency loop with traces, which are short and wide (or with jumper wires which are short and thick).

- Power switch loop formed by DC-link filter capacitor $C_{DC,filter}$ (input capacitor after the bridge), primary main winding , flyback MOSFET and CS resistor R_{CS}.(red loop)
- Main output rectifier loop formed by secondary main winding, main output diode and main output capacitor.(purple loop)
- Auxiliary output rectifier loop formed by auxiliary winding, auxiliary output diode and auxiliary output capacitor.(orange loop)
- Switching loop formed by IC gate drive, CS resistor R_{CS}, power GND to IC GND.(green loop)

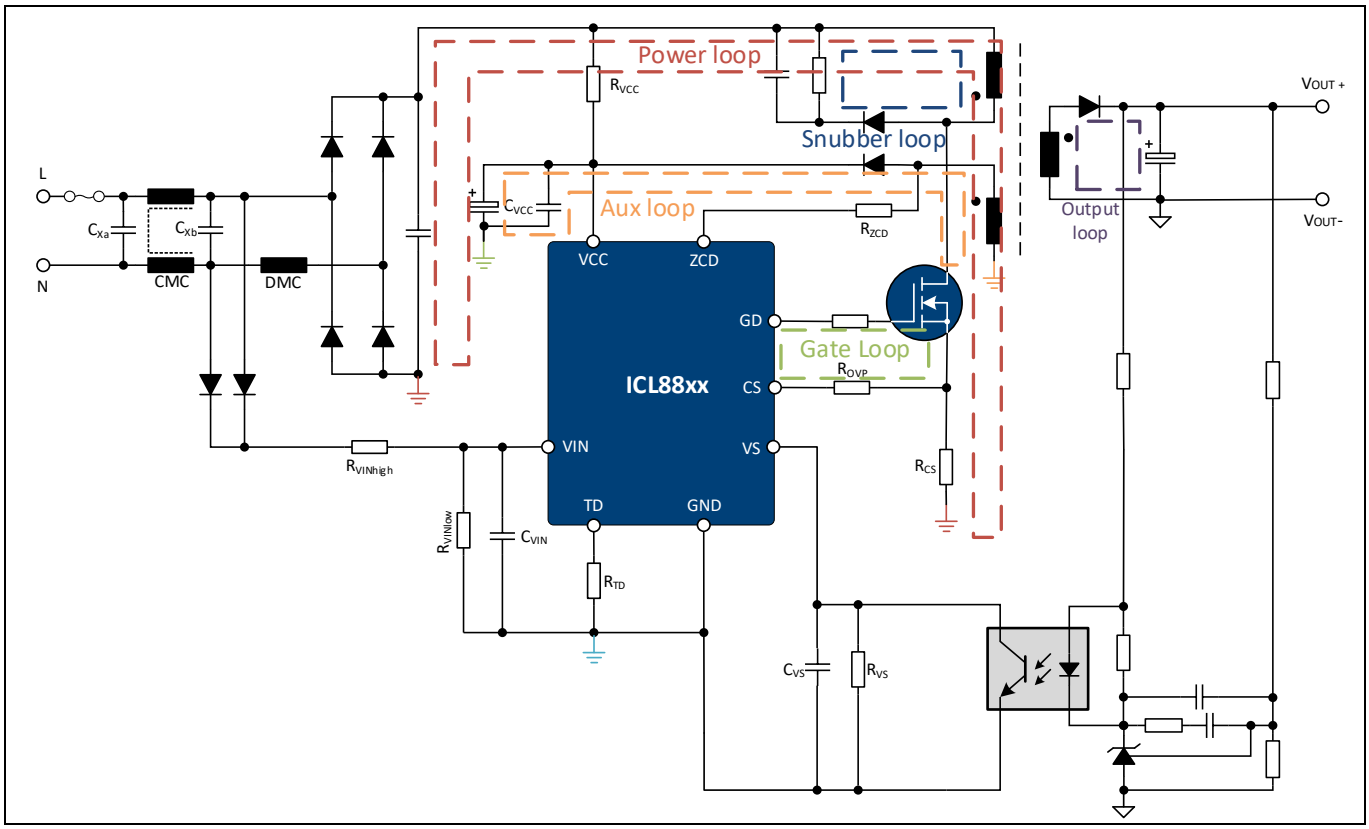

Figure 24 Layout guide for the different current loops

b) Place each filter capacitor, V_{CC} noise decoupling capacitor $C_{VCCdecouple}$ and FB pin filter capacitor C_{FB} near to its designated pin and the GND pin of the controller.

c) Apply the following guide for star grounding.

- Connect ground traces of R_{TD}, C_{FB} and C_{VIN} to march the signal or measurement GND.
- The GND close to the primary auxiliary winding should be shortly connected to a C_{VCC} capacitor to isolate the coupled noise.
- Connect the R_{CS} GND pin near to the ground pin of $C_{DC,filter}$. This results in the power GND.

- Connect the power GND, V_{CC} GND and the signal GND at a single point. This point should be a ceramic capacitor close the V_{CC} and GND pins of the IC.
- If this is not possible due to layout constraints, only the signal GND can be connected directly to the IC GND before connecting the V_{CC} capacitor.

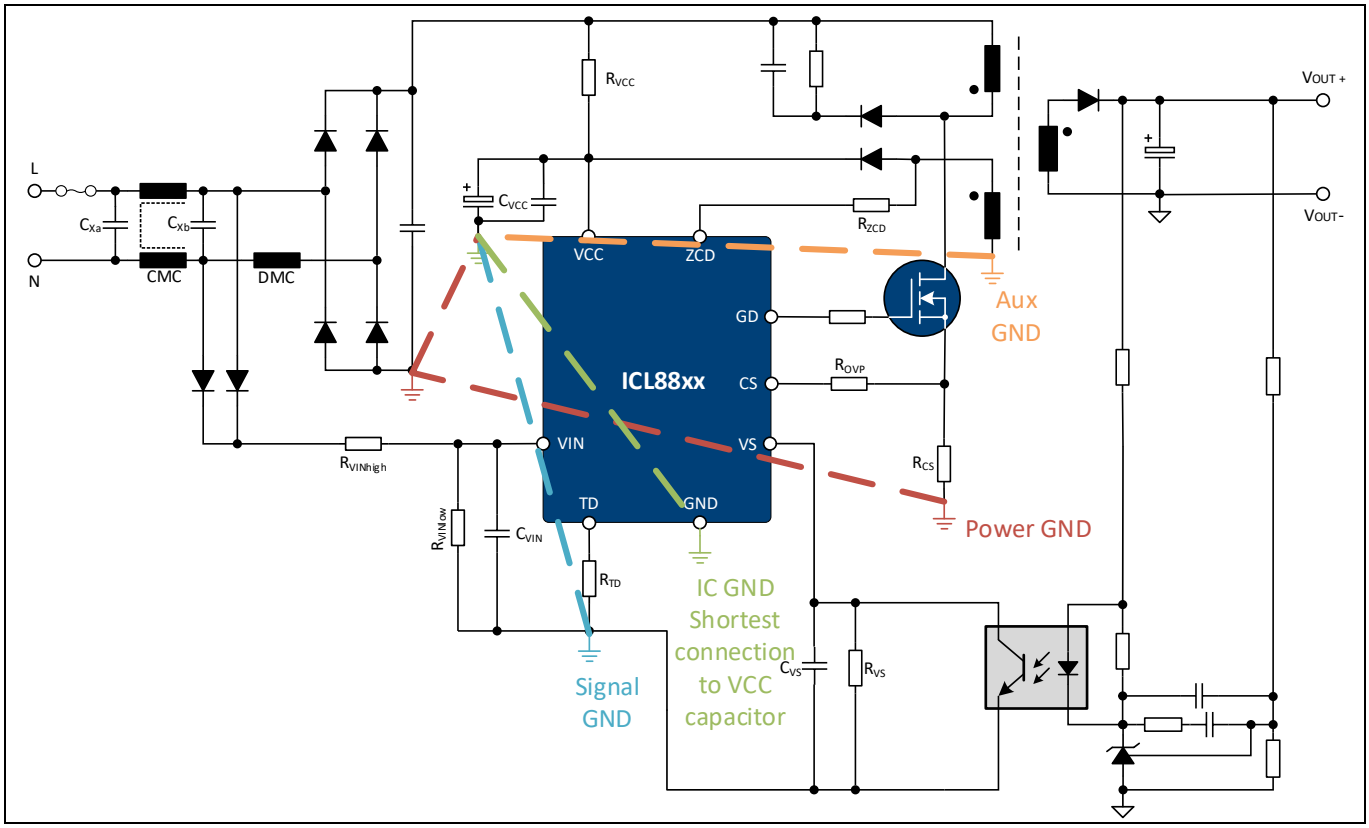

Figure 25 Layout guideline for star ground connection

d) Ensure the high dv/dt traces from the MOSFET drain and GD pin are as far as possible from the VS pin and its connected trace.

e) Shield signal traces with ground traces or ground plane, which can help to reduce noise pick-up.

f) Always ensure appropriate safety clearances between the HV and LV nets.

7 Tips and tricks

Here are some tips and tricks for optimization of the design:

- Make the R_{OVP} resistor initially smaller than calculated. This might help you to debug the board. Finalize this resistor as the last component.
- The ZCD resistor value controls the maximum on-time, but it can also be used to shift the valley jump from the first valley into the second.
- The thresholds for BI/BO and the output OVP are fixed and adjusted for wide-range designs. For narrow voltage range designs, it is necessary to decide which one of the input voltage protections is necessary: BI/BO or OVP and design the V_{IN} circuit around that threshold. Remember that as the lower end is protected by the maximum on-time setting, the OVP could be used without the risk of high currents at low input voltages. This might not be as accurate as the BI/BO but good enough to protect the system from high currents. With this compromise an OVP and UVP with a narrow-range design can be achieved.
- If the THD performance is not satisfactory and the ZCD adjustment does not help, it might be an option to change the R_{TD}. The value is measured after start-up, shortly before the MOSFET starts switching, and is stored inside the device until the next start-up.
- The R_{TD} influences the THD performance and also the valley switching of the IC. Here a compromise has to be found.
- For the ICL8800 and the ICL8810 where an AC-DC detection is not necessary, the VIN pin can also be connected to the DC-link capacitor after the bridge rectifier. In this way two diodes can be saved. For this circuit, the calculation from above is not valid and needs to be adjusted from average to peak measurement. This change is not covered in this document.
- For higher powers and MOSFETs with a high gate charge it can be useful to use an external gate driver circuit. This measure can increase the switching speed and therefore reduce losses, and it can reduce the noise in the system.

8 Debugging guide

This section describes some solutions to common errors:

- If the board is not starting up, the best way to find the reason is to probe V_{CC}, CS (at the pin) and V_{IN}. If these voltages don't cross any protection threshold as described in chapter **10**, it is worth checking the voltage of the regulation circuit on the secondary side.
- If all pin voltages are OK, the IC starts up and begins switching, but now power is delivered to the output, the issue can be along the way from the output at the VS pin. Please check for bad solder points and shorts. Furthermore, check that the diodes and the transformer are working.
- If the system starts up but regularly goes into protection mode with 200 ms restart time, a common reason is a wrongly dimensioned secondary-side OVP. In this case try to lower the R_{OVP} to see if that was the reason.
- If the system doesn't deliver enough power and the output voltage drops before reaching the desired power, a too-high R_{ZCD} might be the problem. Try a lower value. Please keep in mind that this pin is timing relevant, and any capacitive loading (potentiometer) can cause distortion. Furthermore, a too-small R_{CS} could cause similar behavior. Check if the OCP limit is reached in operation.
- If the THD is bad and the input current is distorted, there can be multiple reasons, such as a too-fast feedback loop, capacitive loading of the R_{ZCD}, unsuitable R_{TD}, or a too-small R_{CS}.
- If the IC doesn't start up at 12.5 V but at much higher voltages at low AC input voltage, the cause is the averaging of the VIN pin. If this is a problem in your system try to increase the V_{IN} voltage by changing the resistor divider.
- The fast-reacting second OVP and the slow feedback loop may cause an unwanted behavior, where the system is stuck in repetitive restarts. Here the output voltage rises very fast to the OVP level (half-charged output capacitor, fast AC restart, etc.), and triggers the protection while the feedback loop has no time to react. This can occur due to multiple reasons such as a too-small output capacitor or when the output voltage set-point is too close to the OVP level. Solutions might be to increase the output capacitor, increase the threshold for the OVP, lower the set-point or change the behavior of the load, to name a few.

9 ICL8800 operation flow chart

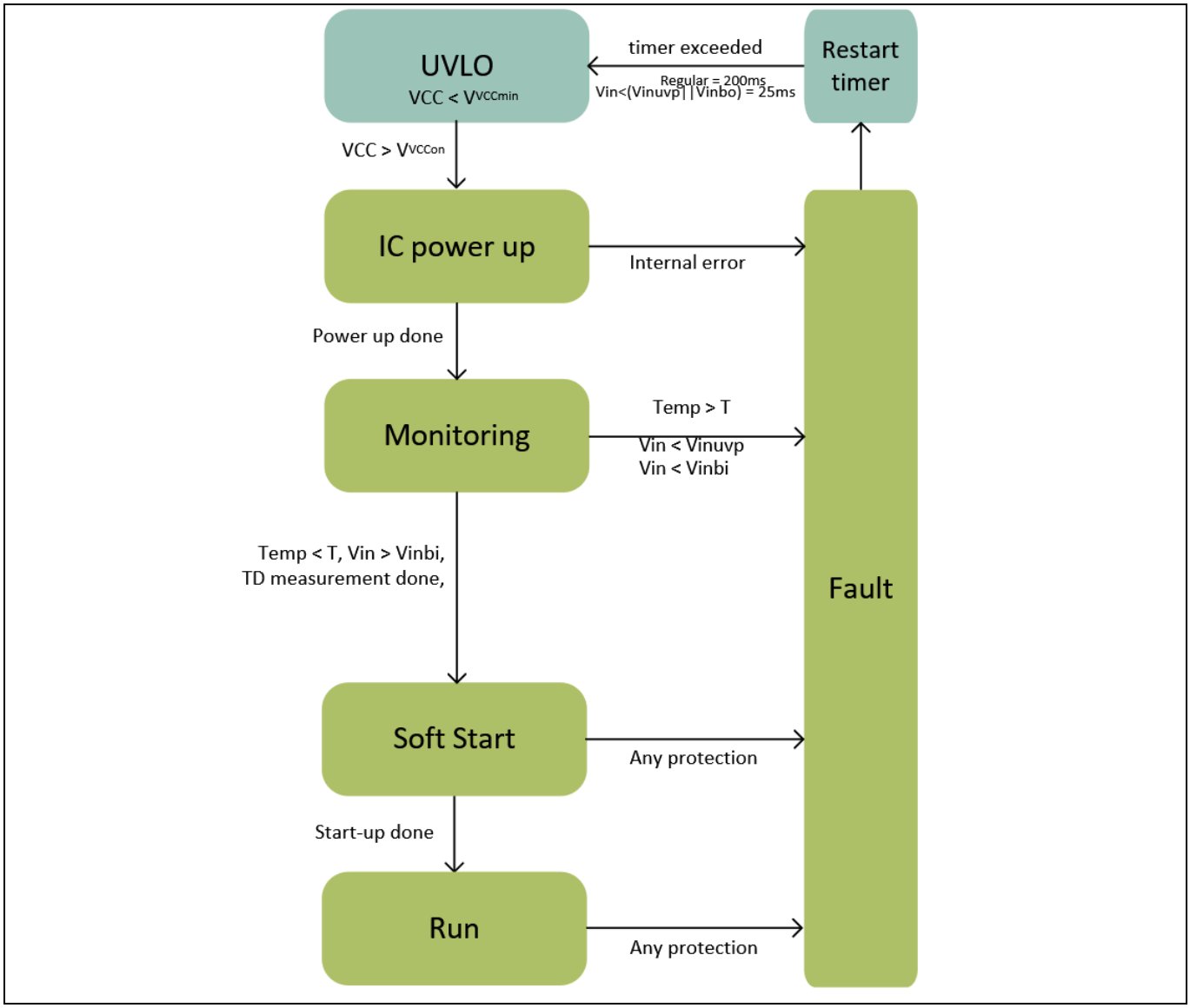

Figure 26 ICL88xx operation flow chart

10 Protection features

All ICL8800 protection features are summarized in the following fault matrix.

Table 4 Fault reactions

Fault	Detection	Typical blanking time	State				Reaction
			Monitor	Soft-start	Run	OV	
Insufficient supply	V_{VCC} less than V_{VCCon}	1 µs	X	–	–	–	Wait in reset
Insufficient supply	V_{VCC} less than V_{VCCmin}	1 µs	X	X	X	X	Reset
V_{IN} short protection	V_{VIN} less than $V_{VINshort}$	1 µs	X	X	X	X	Fast auto restart after $t_{restart,fast}$
V_{IN} UVP	V_{VIN} less than V_{BI}	2 ms	X	X	X	X	Auto restart after $t_{restart}$
V_{IN} OVP	V_{VIN} greater than V_{VINOV}	2 ms	X	X	X	X	Auto restart after $t_{restart}$
Overtemperature	T greater than $T_{critical}$	18 µs	X	X	X	X	Auto restart after $t_{restart}$
Open-loop	V_{VS} greater than $V_{VSOVOFFFB}$	1 µs	X	-	-	-	Auto restart after $t_{restart}$
Secondary output OVP	I_{ZCD} greater than ...	100 µs (100 clks)	–	X	X	X	Auto restart after $t_{restart}$
Overcurrent protection (OCP2)	V_{CS} greater than V_{OCP2}	150 ns	–	X	X	X	Auto restart after $t_{restart}$
V_{CC} OV	V_{CC} greater than V_{VCCOVP}	1 µs	–	X	X	X	Auto restart after $t_{restart}$
Overcurrent protection (OCP1)	V_{CS} greater than V_{OCP1}	250 ns	–	X	X	X	Turn off gate driver for the ongoing switching cycle

10.1 Schematic

The schematic of the ICL88xx 43 W, SSR reference design for LED lighting applications is given in **Figure 27** to **Figure 30**.

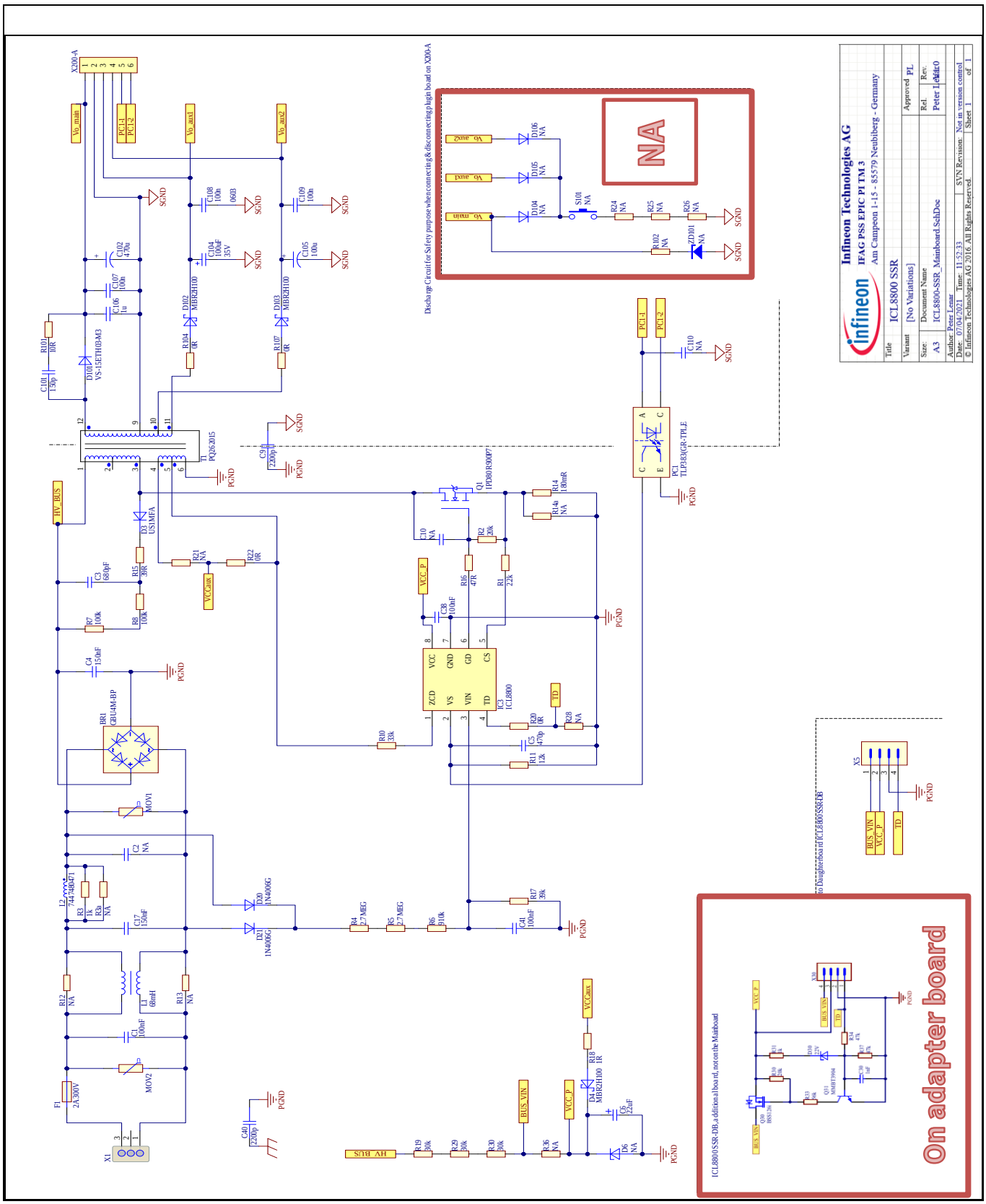

Figure 27 ICL88xx 43 W wide input voltage range SSR flyback reference design schematic

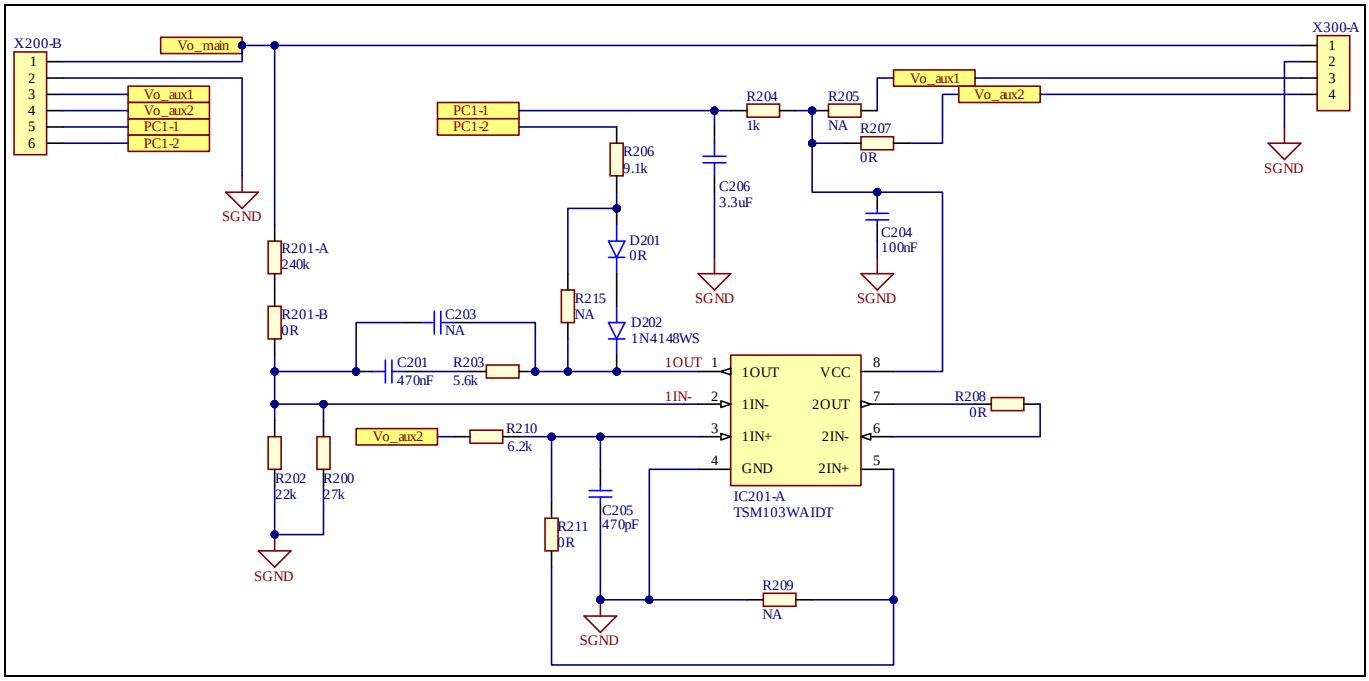

Figure 28 Flyback SSR regulation circuit with operational amplifier

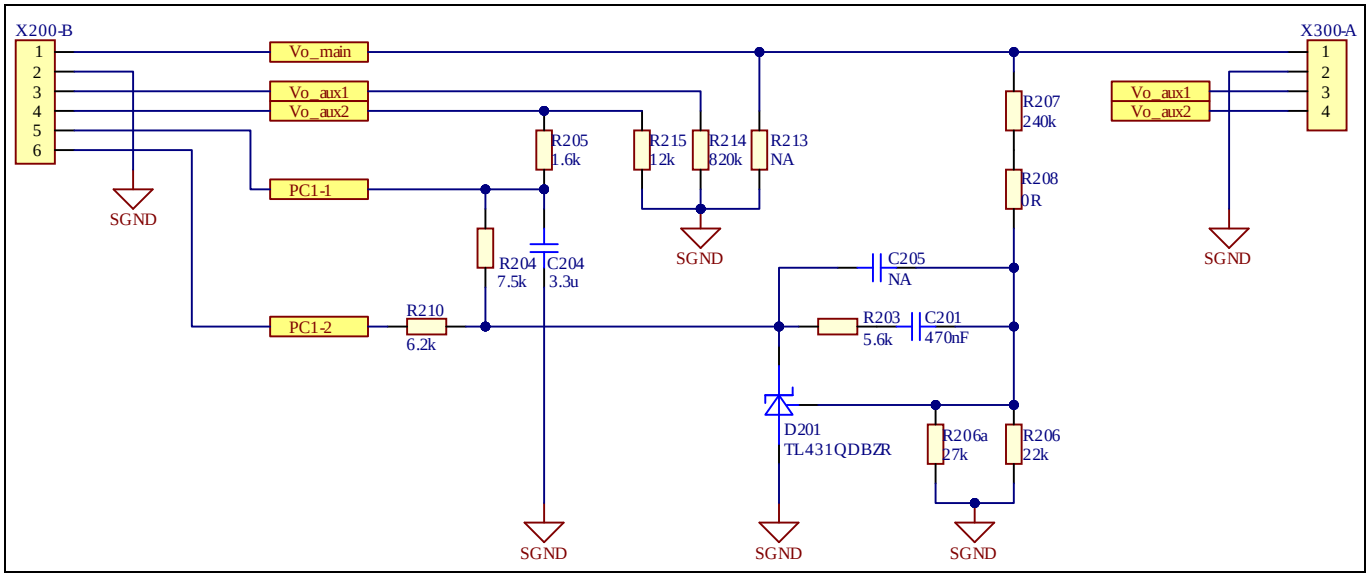

Figure 29 Flyback SSR regulation circuit based on TL431 reference

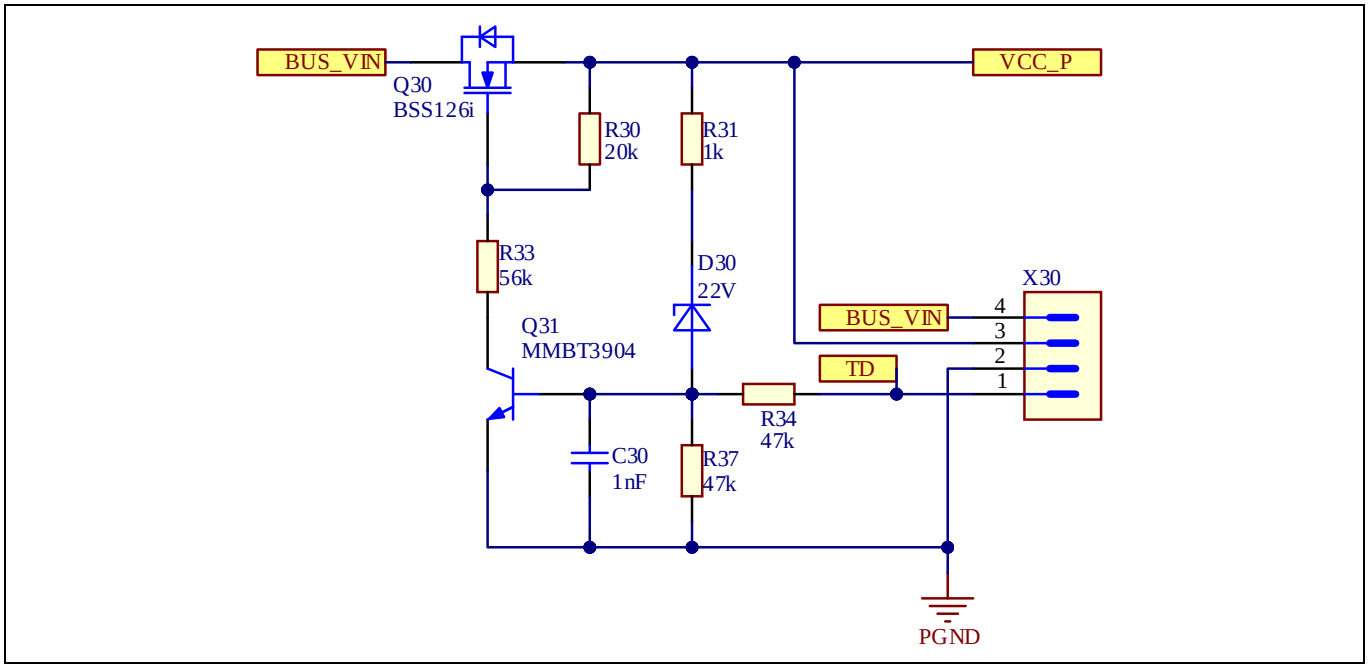

Figure 30 Optional start-up circuit for low standby current and fast start-up

11 References

[1] **ICL88xx datasheet**

[2] **REF-ICL88xx-U40W engineering report**

12 Revision history

Version	Date	Changes
V 1.0	01-07-2021	First release

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