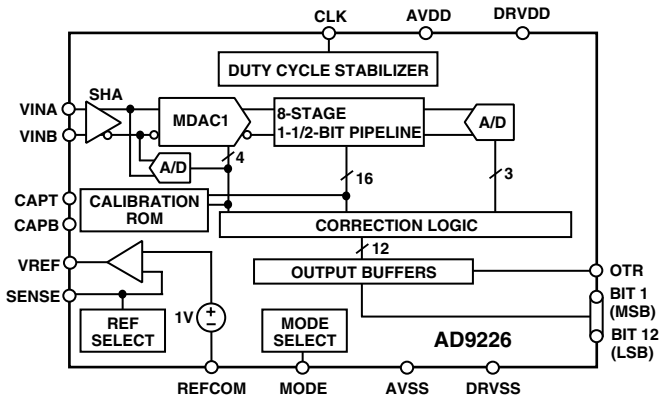
Complete 12-Bit, 65 MSPS ADC Converter

AD9226

FEATURES

Signal-to-Noise Ratio: 69 dB @ f_{IN} = 31 MHz
Spurious-Free Dynamic Range: 85 dB @ f_{IN} = 31 MHz
Intermodulation Distortion of –75 dBFS @ f_{IN} = 140 MHz
ENOB = 11.1 @ f_{IN} = 10 MHz
Low-Power Dissipation: 475 mW
No Missing Codes Guaranteed
Differential Nonlinearity Error: ±0.6 LSB
Integral Nonlinearity Error: ±0.6 LSB
Clock Duty Cycle Stabilizer
Patented On-Chip Sample-and-Hold with Full Power Bandwidth of 750 MHz
Straight Binary or Two's Complement Output Data
28-Lead SSOP, 48-Lead LQFP
Single 5 V Analog Supply, 3 V/5 V Driver Supply
Pin-Compatible to AD9220, AD9221, AD9223, AD9224, AD9225

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9226 is a monolithic, single-supply, 12-bit, 65 MSPS analog-to-digital converter with an on-chip, high-performance sample-and-hold amplifier and voltage reference. The AD9226 uses a multistage differential pipelined architecture with a patented input stage and output error correction logic to provide 12-bit accuracy at 65 MSPS data rates. There are no missing codes over the full operating temperature range (guaranteed).

The input of the AD9226 allows for easy interfacing to both imaging and communications systems. With a truly differential input structure, the user can select a variety of input ranges and offsets including single-ended applications.

The sample-and-hold amplifier (SHA) is well suited for IF undersampling schemes such as in single-channel communication applications with input frequencies up to and well beyond Nyquist frequencies.

The AD9226 has an on-board programmable reference. For system design flexibility, an external reference can also be chosen.

A single clock input is used to control all internal conversion cycles. An out-of-range signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

The AD9226 has two important mode functions. One will set the data format to binary or two's complement. The second will make the ADC immune to clock duty cycle variations.

PRODUCT HIGHLIGHTS

IF Sampling—The patented SHA input can be configured for either single-ended or differential inputs. It will maintain outstanding AC performance up to input frequencies of 300 MHz.

Low Power—The AD9226 at 475 mW consumes a fraction of the power presently available in existing, high-speed monolithic solutions.

Out of Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9226's input range.

Single Supply—The AD9226 uses a single 5 V power supply simplifying system power supply design. It also features a separate digital output driver supply line to accommodate 3 V and 5 V logic families.

Pin Compatibility—The AD9226 is similar to the AD9220, AD9221, AD9223, AD9224, and AD9225 ADCs.

Clock Duty Cycle Stabilizer—Makes conversion immune to varying clock pulsewidths.

REV. B

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AD9226–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = 5 V, DRVDD = 3 V, f_{SAMPLE} = 65 MSPS, VREF = 2.0 V, Differential inputs, T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION			12			Bits
ACCURACY						
Integral Nonlinearity (INL)	Full	V		±0.6		LSB
	25°C	I			±1.6	LSB
Differential Nonlinearity (DNL)	Full	V		±0.6		LSB
	25°C	I			±1.0	LSB
No Missing Codes Guaranteed	Full	I	12			Bits
Zero Error	Full	V		±0.3		% FSR
	25°C	I			±1.4	% FSR
Gain Error	25°C	I			±2.0	% FSR
	Full	V		±0.6		% FSR
TEMPERATURE DRIFT						
Zero Error	Full	V		±2		ppm/°C
Gain Error[1]	Full	V		±26		ppm/°C
Gain Error[2]	Full	V		±0.4		ppm/°C
POWER SUPPLY REJECTION						
AVDD (5 V ± 0.25 V)	Full	V		±0.05		% FSR
	25°C	I			±0.4	% FSR
INPUT REFERRED NOISE						
VREF = 1.0 V	Full	V		0.5		LSB rms
VREF = 2.0 V	Full	V		0.25		LSB rms
ANALOG INPUT						
Input Span (VREF = 1 V)	Full	V		1		V p-p
(VREF = 2 V)	Full	V		2		V p-p
Input (VINA or VINB) Range	Full	IV	0		AVDD	V
Input Capacitance	Full	V		7		pF
INTERNAL VOLTAGE REFERENCE						
Output Voltage (1 V Mode)	Full	V		1.0		V
Output Voltage Tolerance (1 V Mode)	25°C	I			±15	mV
Output Voltage (2.0 V Mode)	Full	V		2.0		V
Output Voltage Tolerance (2.0 V Mode)	25°C	I			±29	mV
Output Current (Available for External Loads)	Full	V		1.0		mA
Load Regulation[3]	Full	V		0.7		mV
	25°C	I			1.5	mV
REFERENCE INPUT RESISTANCE	Full	V		5		kΩ
POWER SUPPLIES						
Supply Voltages						
AVDD	Full	V	4.75	5	5.25	V (±5% AVDD Operating)
DRVDD	Full	V	2.85		5.25	V (±5% DRVDD Operating)
Supply Current						
IAVDD[4]	Full	V		86		mA (2 V External VREF)
	25°C	I			90.5	mA (2 V External VREF)
IDRVDD[5]	Full	V		14.6		mA (2 V External VREF)
	25°C	I			16.5	mA (2 V External VREF)
POWER CONSUMPTION[4, 5]	Full	V		475		
	25°C	I			500	mW (2 V External VREF)

NOTES
[1]Includes internal voltage reference error.
[2]Excludes internal voltage reference error.
[3]Load regulation with 1 mA load current (in addition to that required by the AD9226).
[4]AVDD = 5 V
[5]DRVDD = 3 V

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = 5 V, DRVDD = 3 V, f_{SAMPLE} = 65 MSPS, VREF = 2.0 V, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameters	Temp	Test Level	Min	Typ	Max	Unit
LOGIC INPUTS (Clock, DFS[1], Duty Cycle[1], and Output Enable[1])						
High-Level Input Voltage	Full	IV	2.4			V
Low-Level Input Voltage	Full	IV			0.8	V
High-Level Input Current (V_{IN} = AVDD)	Full	IV	–10		+10	µA
Low-Level Input Current (V_{IN} = 0 V)	Full	IV	–10		+10	µA
Input Capacitance	Full	V		5		pF
Output Enable[1]	Full	IV	$\frac{DRVDD}{2} - 0.5$		$\frac{DRVDD}{2} + 0.5$	V
LOGIC OUTPUTS (With DRVDD = 5 V)						
High-Level Output Voltage (I_{OH} = 50 µA)	Full	IV	4.5			V
High-Level Output Voltage (I_{OH} = 0.5 mA)	Full	IV	2.4			V
Low-Level Output Voltage (I_{OL} = 1.6 mA)	Full	IV			0.4	V
Low-Level Output Voltage (I_{OL} = 50 µA)	Full	IV			0.1	V
Output Capacitance				5		pF
LOGIC OUTPUTS (With DRVDD = 3 V)						
High-Level Output Voltage (I_{OH} = 50 µA)	Full	IV	2.95			V
High-Level Output Voltage (I_{OH} = 0.5 mA)	Full	IV	2.80			V
Low-Level Output Voltage (I_{OL} = 1.6 mA)	Full	IV			0.4	V
Low-Level Output Voltage (I_{OL} = 50 µA)	Full	IV			0.05	V

NOTES
[1]LQFP package.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AVDD = 5 V, DRVDD = 3 V, C_L = 20 pF)

Parameters	Temp	Test Level	Min	Typ	Max	Unit
Max Conversion Rate	Full	VI	65			MHz
Clock Period[1]	Full	V	15.38			ns
CLOCK Pulsewidth High[2]	Full	V	3			ns
CLOCK Pulsewidth Low[2]	Full	V	3			ns
Output Delay	Full	V	3.5		7	ns
Pipeline Delay (Latency)	Full	V		7		Clock Cycles
Output Enable Delay[3]	Full	V		15		ns

NOTES
[1]The clock period may be extended to 10 µs without degradation in specified performance @ 25°C.
[2]When MODE pin is tied to AVDD or grounded, the AD9226 SSOP is not affected by clock duty cycle.
[3]LQFP package.

Specifications subject to change without notice.

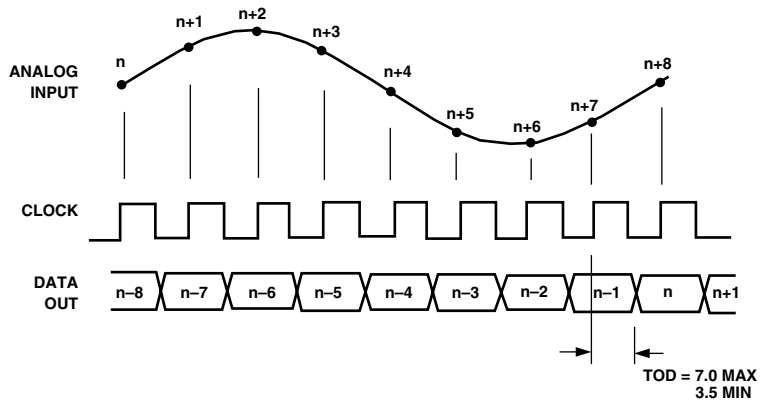


Figure 1. Timing Diagram

AD9226–SPECIFICATIONS

AC SPECIFICATIONS (AVDD = 5 V, DRVDD = 3 V, f_{SAMPLE} = 65 MSPS, VREF = 2.0 V, T_{MIN} to T_{MAX}, Differential Input unless otherwise noted.)

Parameter	Temp	Test Level	Min	Typ	Max	Unit
SIGNAL-TO-NOISE RATIO						
f_{IN} = 2.5 MHz	Full	V		68.9		dBc
	25°C	I	68			dBc
f_{IN} = 15 MHz	Full	V		68.4		dBc
	25°C	I	67.4			dBc
f_{IN} = 31 MHz	Full	V		68		dBc
f_{IN} = 60 MHz	Full	V		68		dBc
f_{IN} = 200 MHz[1]	Full	V		65		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION						
f_{IN} = 2.5 MHz	Full	V		68.8		dBc
	25°C	I	67.9			dBc
f_{IN} = 15 MHz	Full	V		68.3		dBc
	25°C	I	67.3			dBc
f_{IN} = 31 MHz	Full	V		67		dBc
f_{IN} = 60 MHz	Full	V		67		dBc
f_{IN} = 200 MHz[1]	Full	V		60		dBc
TOTAL HARMONIC DISTORTION						
f_{IN} = 2.5 MHz	Full	V		–84		dBc
	25°C	I			–77.0	dBc
f_{IN} = 15 MHz	Full	V		–82.3		dBc
	25°C	I			–76.0	dBc
f_{IN} = 31 MHz	Full	V		–68		dBc
f_{IN} = 60 MHz	Full	V		–68		dBc
f_{IN} = 200 MHz[1]	Full	V		–61		dBc
SECOND AND THIRD HARMONIC DISTORTION						
f_{IN} = 2.5 MHz	Full	V		–86.5		dBc
	25°C	I			–78	dBc
f_{IN} = 15 MHz	Full	V		–86.7		dBc
	25°C	I			–76	dBc
f_{IN} = 31 MHz	Full	V		–83		dBc
f_{IN} = 60 MHz	Full	V		–82		dBc
f_{IN} = 200 MHz[1]	Full	V		–75		dBc
SPURIOUS FREE DYNAMIC RANGE						
f_{IN} = 2.5 MHz	Full	V		86.4		dBc
	25°C	I	78			dBc
f_{IN} = 15 MHz	Full	V		85.5		dBc
	25°C	I	76			dBc
f_{IN} = 31 MHz	Full	V		82		dBc
f_{IN} = 60 MHz	Full	V		81		dBc
f_{IN} = 200 MHz[1]	Full	V		60		dBc
ANALOG INPUT BANDWIDTH	25°C	V		750		MHz

NOTES

[1]1.0 V Reference and Input Span

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures. AC testing done on sample basis.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. All devices are 100% production tested at 25°C; sample tested at temperature extremes.

THERMAL RESISTANCE

θ_{JC} SSOP . . . . . 23°C/W
θ_{JA} SSOP . . . . . 63.3°C/W
θ_{JC} LQFP . . . . . 17°C/W
θ_{JA} LQFP . . . . . 76.2°C/W

ABSOLUTE MAXIMUM RATINGS[1]

Pin Name	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+6.5	V
DRVDD	DRVSS	–0.3	+6.5	V
AVSS	DRVSS	–0.3	+0.3	V
AVDD	DRVDD	–6.5	+6.5	V
REFCOM	AVSS	–0.3	+0.3	V
CLK, MODE	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
OEB[2]	DRVSS	–0.3	DRVDD + 0.3	V
CM LEVEL[2]	AVSS	–0.3	AVDD + 0.3	V
VR[2]	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

[2]LQFP package.

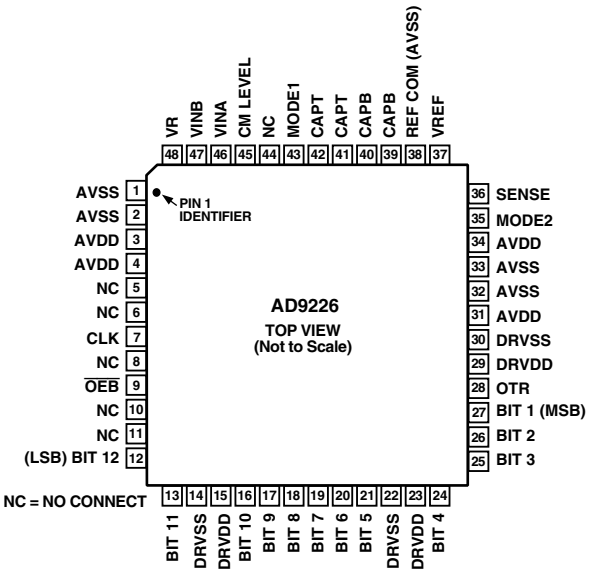
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9226ARS	–40°C to +85°C	28-Lead Shrink Small Outline (SSOP)	RS-28
AD9226AST	–40°C to +85°C	48-Lead Thin Plastic Quad Flatpack (LQFP)	ST-48
AD9226-EB		Evaluation Board (SSOP)	
AD9226-LQFP-EB		Evaluation Board (LQFP)	

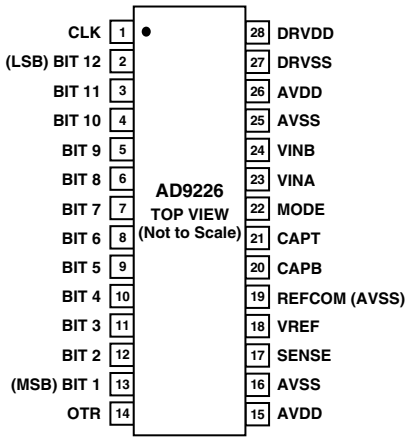
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9226 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONNECTION
48-Lead LQFP



PIN CONNECTION
28-Lead SSOP



48-PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Description
1, 2, 32, 33	AVSS	Analog Ground
3, 4, 31, 34	AVDD	5 V Analog Supply
5, 6, 8, 10, 11, 44	NC	No Connect
7	CLK	Clock Input Pin
9	$\overline{\text{OEB}}$	Output Enable (Active Low)
12	BIT 12	Least Significant Data Bit (LSB)
13	BIT 11	Data Output Bit
14, 22, 30	DRVSS	Digital Output Driver Ground
15, 23, 29	DRVDD	3 V to 5 V Digital Output Driver Supply
16–21, 24–26	BITS 10–5, BITS 4–2	Data Output Bits
27	BIT 1	Most Significant Data Bit (MSB)
28	OTR	Out of Range
35	MODE2	Data Format Select
36	SENSE	Reference Select
37	VREF	Reference In/Out
38	REFCOM (AVSS)	Reference Common
39, 40	CAPB	Noise Reduction Pin
41, 42	CAPT	Noise Reduction Pin
43	MODE1	Clock Stabilizer
45	CM LEVEL	Midsupply Reference
46	VINA	Analog Input Pin (+)
47	VINB	Analog Input Pin (–)
48	VR	Noise Reduction Pin

28-PIN FUNCTION DESCRIPTIONS

Pin Number	Name	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BITS 11–2	Data Output Bits
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Input Span Select (Reference I/O)
19	REFCOM (AVSS)	Reference Common
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	MODE	Data Format Select/Clock Stabilizer
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DRVSS	Digital Output Driver Ground
28	DRVDD	3 V to 5 V Digital Output Driver Supply

DEFINITIONS OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and can be manifested as noise on the input to the ADC.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to obtain a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

ENCODE PULSEWIDTH DUTY CYCLE

Pulsewidth high is the minimum amount of time that the clock pulse should be left in the logic "1" state to achieve rated performance; pulsewidth low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specs define an acceptable clock duty cycle.

MINIMUM CONVERSION RATE

The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

MAXIMUM CONVERSION RATE

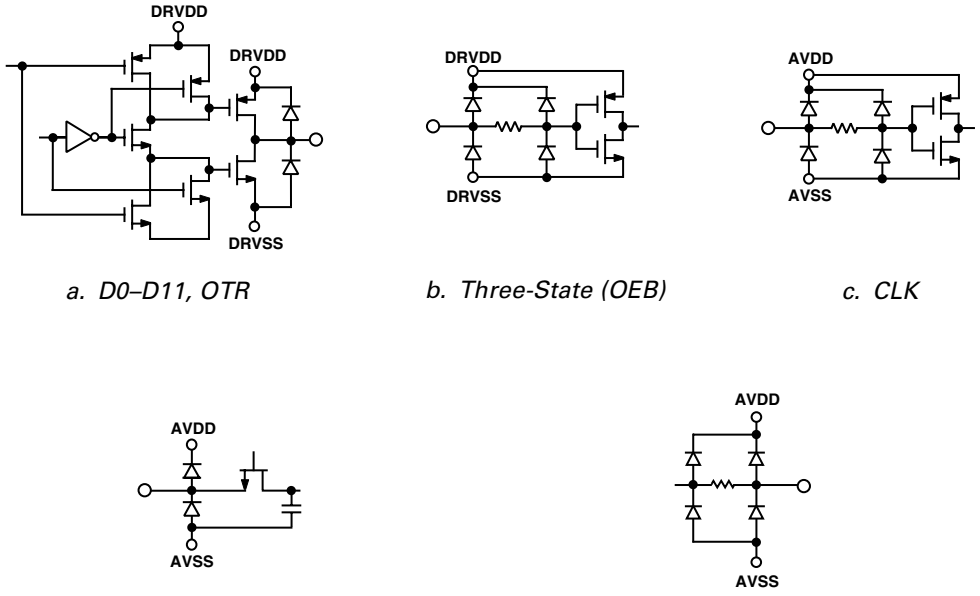
The encode rate at which parametric testing is performed.

OUTPUT PROPAGATION DELAY

The delay between the clock logic threshold and the time when all bits are within valid logic levels.

TWO TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).



a. D0–D11, OTR

b. Three-State (OEB)

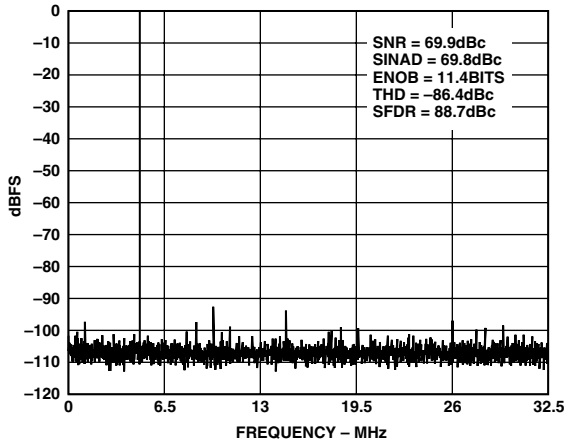
c. CLK

d. AIN

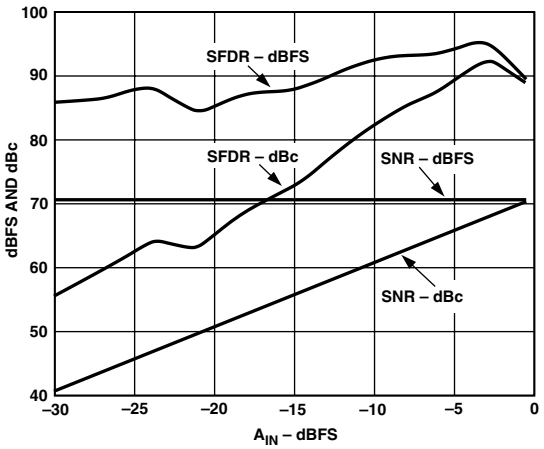
e. CAPT, CAPB, MODE, SENSE, VREF

Figure 2. Equivalent Circuits

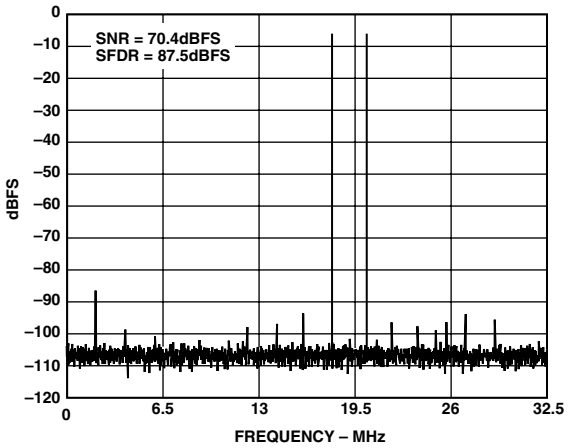
(AVDD = 5.0 V, DRVDD = 3.0 V, f_{SAMPLE} = 65 MSPS with CLK Stabilizer Enabled, T_A = 25°C, 2 V Differential Input Span, V_{CM} = 2.5 V, A_{IN} = –0.5 dBFS, V_{REF} = 2.0 V, unless otherwise noted.)



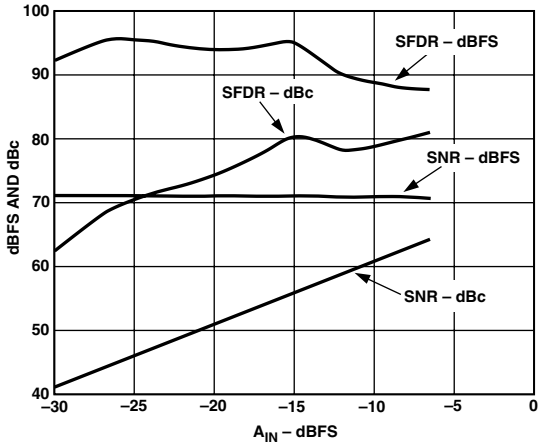
TPC 1. Single-Tone 8K FFT with f_{IN} = 5 MHz



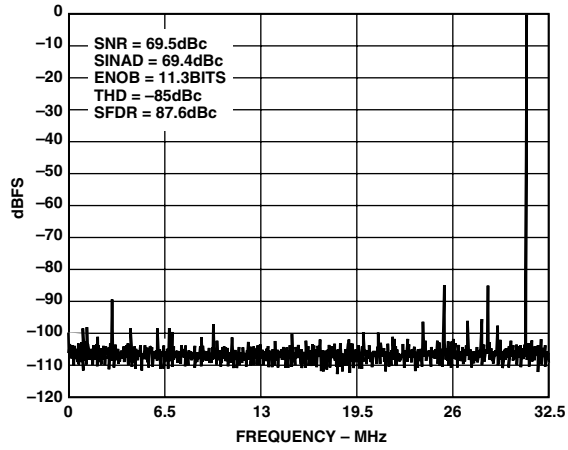
TPC 4. Single-Tone SNR/SFDR vs. A_{IN} with f_{IN} = 5 MHz



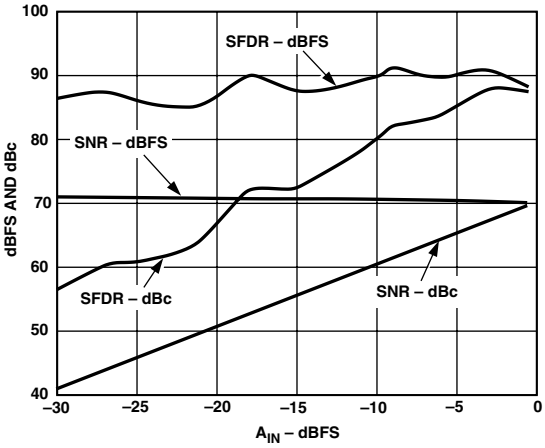
TPC 2. Dual-Tone 8K FFT with $f_{IN–1}$ = 18 MHz and $f_{IN–2}$ = 20 MHz ($A_{IN–1}$ = $A_{IN–2}$ = –6.5 dBFS)



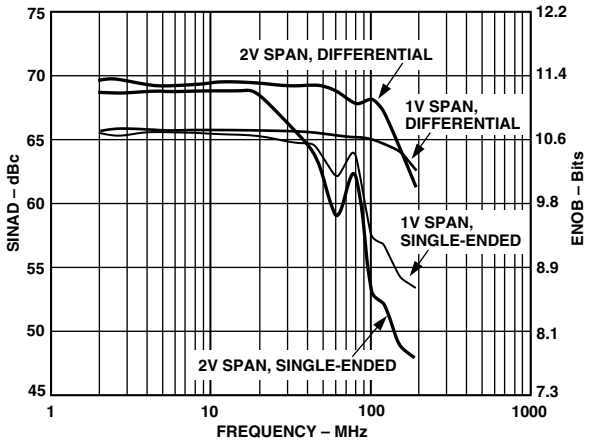
TPC 5. Dual-Tone SNR/SFDR vs. A_{IN} with $f_{IN–1}$ = 18 MHz and $f_{IN–2}$ = 20 MHz



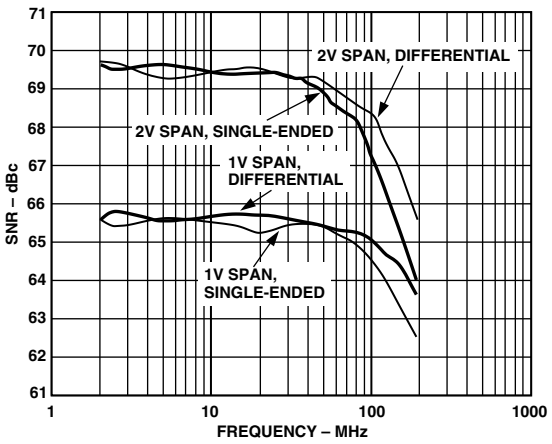
TPC 3. Single-Tone 8K FFT with f_{IN} = 31 MHz



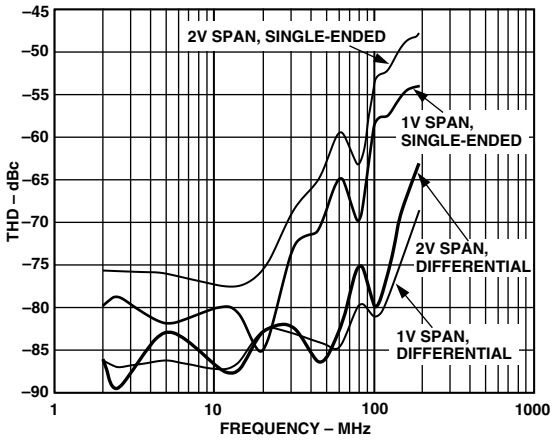
TPC 6. Single-Tone SNR/SFDR vs. A_{IN} with f_{IN} = 31 MHz



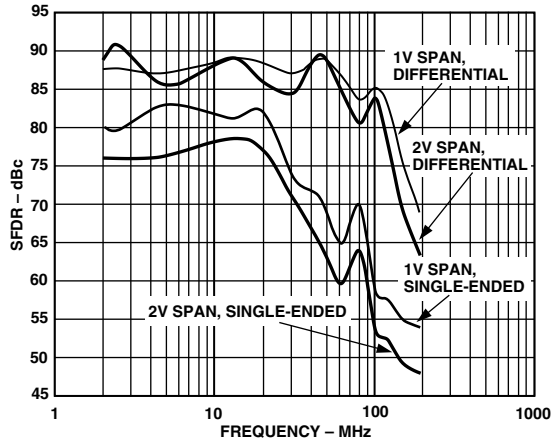
TPC 7. SINAD/ENOB vs. Frequency



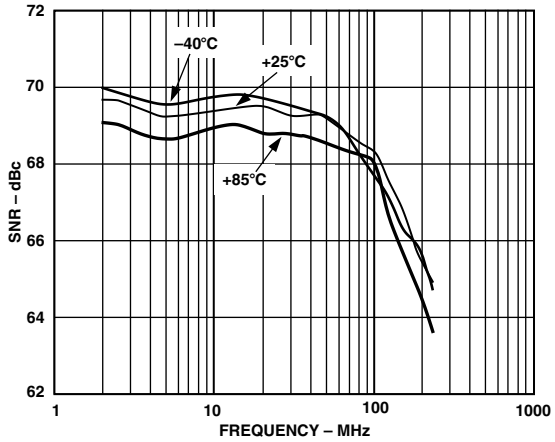
TPC 10. SNR vs. Frequency



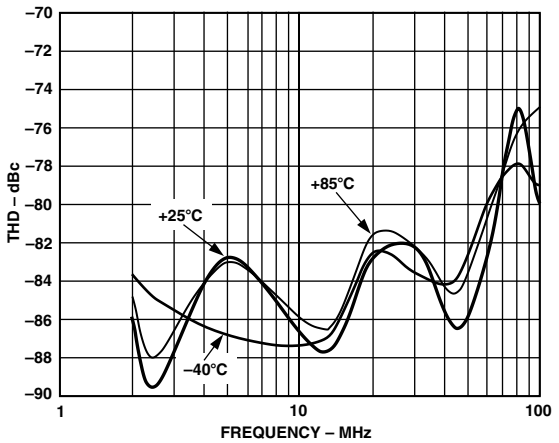
TPC 8. THD vs. Frequency



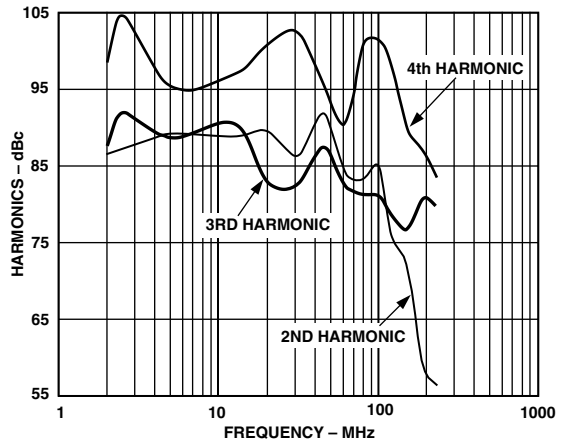
TPC 11. SFDR vs. Frequency



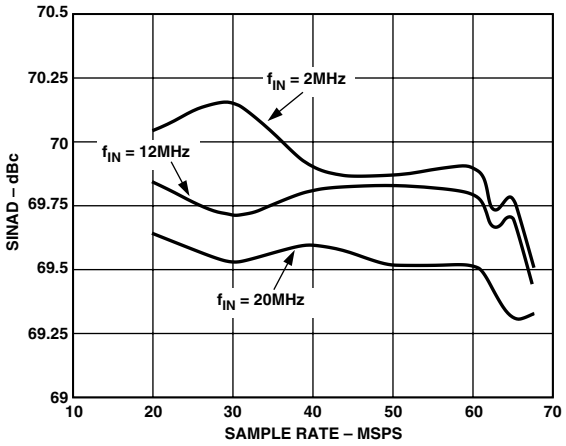
TPC 9. SNR vs. Temperature and Frequency



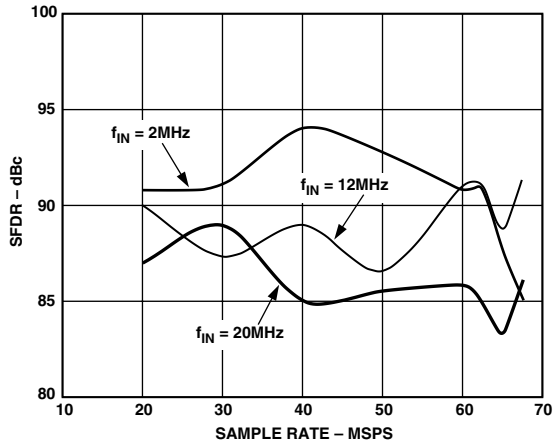
TPC 12. THD vs. Temperature and Frequency



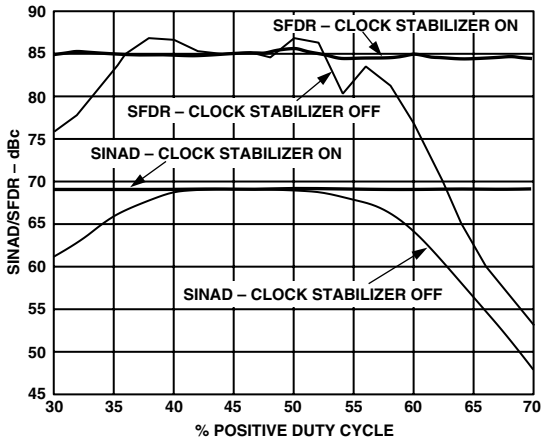
TPC 13. Harmonics vs. Frequency



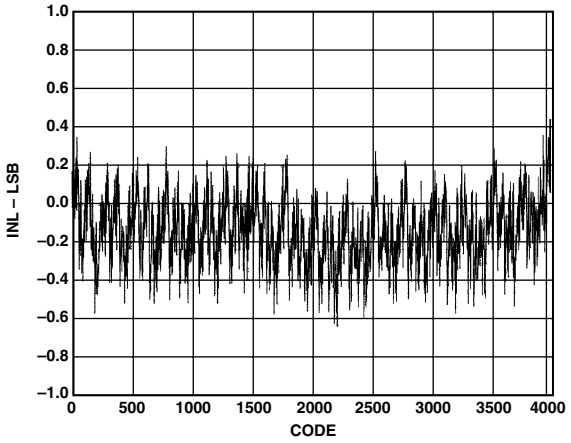
TPC 16. SINAD vs. Sample Rate



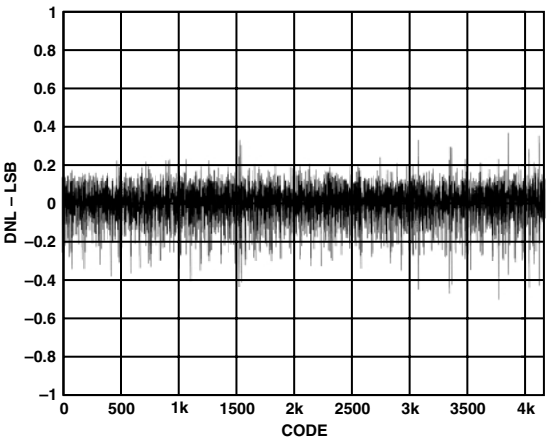
TPC 14. SFDR vs. Sample Rate



TPC 17. SINAD/SFDR vs. Duty Cycle @ f_{IN} = 20 MHz



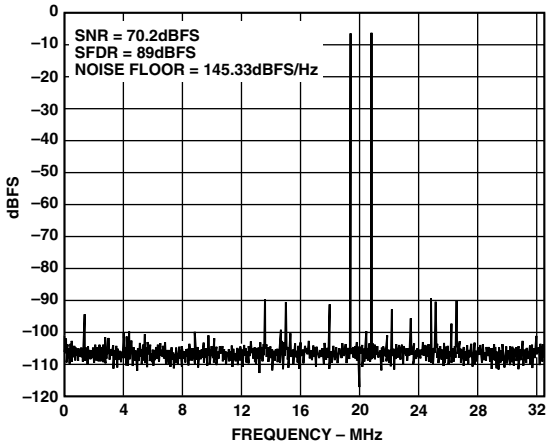
TPC 15. Typical INL



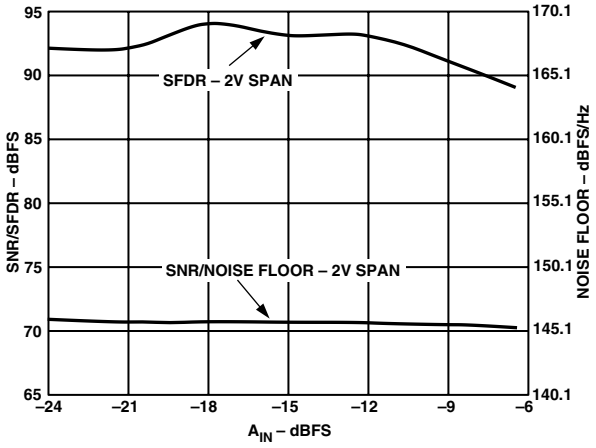
TPC 18. Typical DNL

AD9226–Typical IF Sampling Performance Characteristics

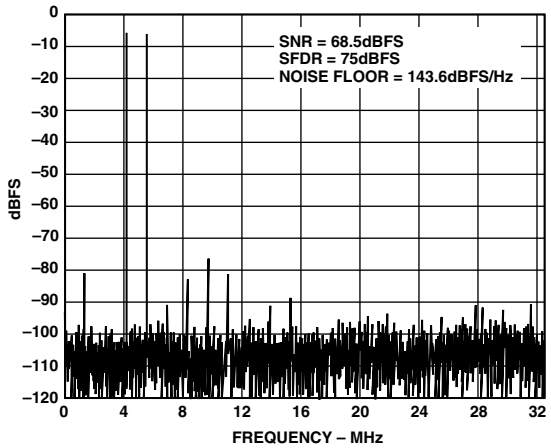
(AVDD = 5.0 V, DRVDD = 3.0 V, f_{SAMPLE} = 65 MSPS with CLK Stabilizer Enabled, T_A = 25°C, 2 V Differential Input Span, V_{CM} = 2.5 V, A_{IN} = –6.5 dBFS, V_{REF} = 2.0 V, unless otherwise noted.)



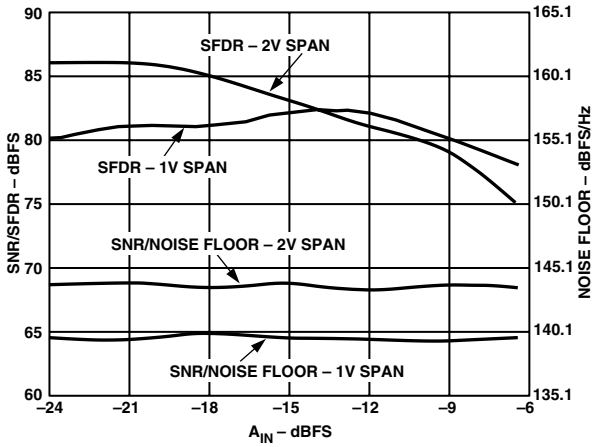
TPC 19. Dual-Tone 8K FFT with f_{IN-1} = 44.2 MHz and f_{IN-2} = 45.6 MHz



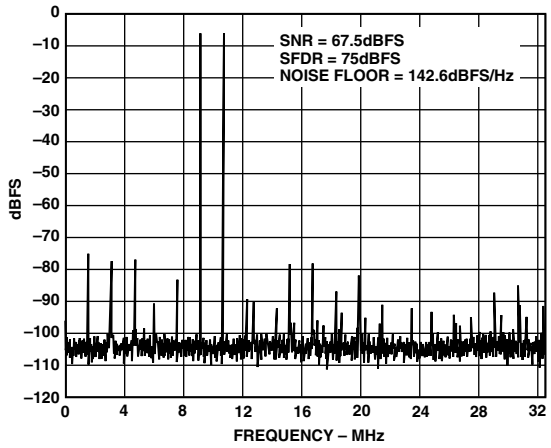
TPC 22. Dual-Tone SNR and SFDR with f_{IN-1} = 44.2 MHz and f_{IN-2} = 45.6 MHz



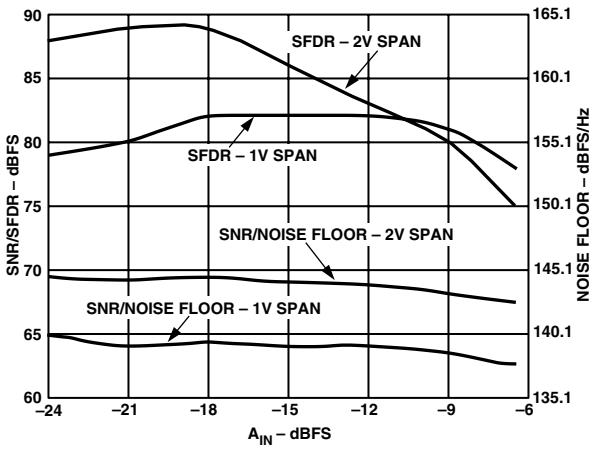
TPC 20. Dual-Tone 8K FFT with f_{IN-1} = 69.2 MHz and f_{IN-2} = 70.6 MHz



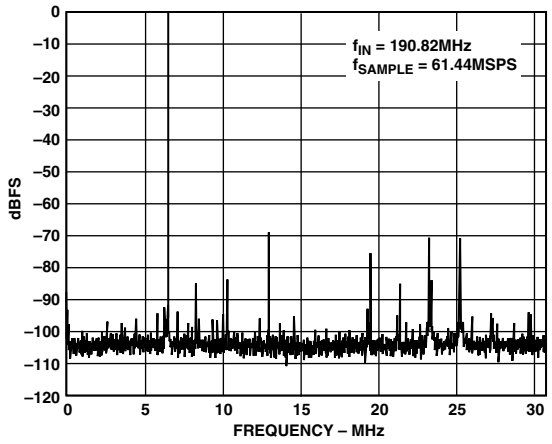
TPC 23. Dual-Tone SNR and SFDR with f_{IN-1} = 69.2 MHz and f_{IN-2} = 70.6 MHz



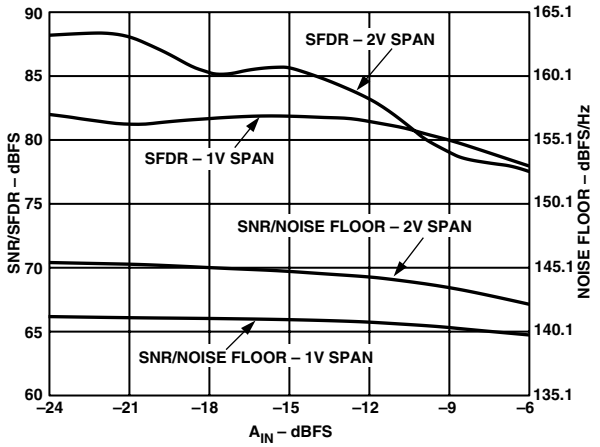
TPC 21. Dual-Tone 8K FFT with f_{IN-1} = 139.2 MHz and f_{IN-2} = 140.7 MHz



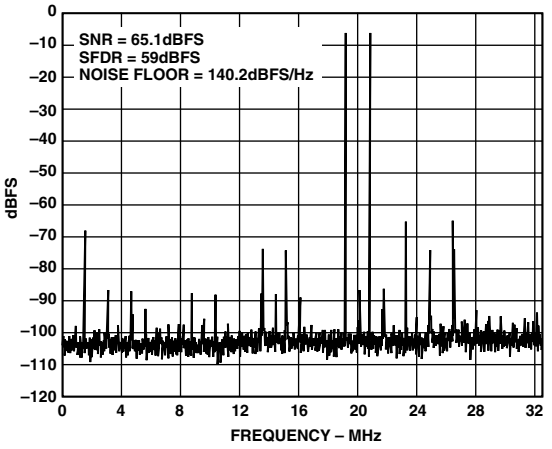
TPC 24. Dual-Tone SNR and SFDR with f_{IN-1} = 139.2 MHz and f_{IN-2} = 140.7 MHz



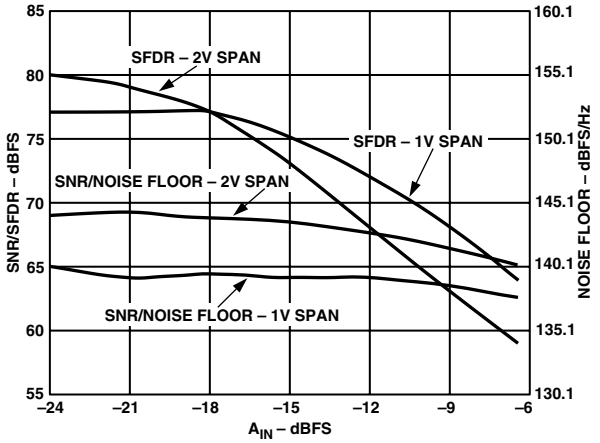
TPC 25. Single-Tone 8K FFT at IF = 190 MHz–WCDMA (f_{IN} = 190.82 MHz, f_{SAMPLE} = 61.44 MSPS)



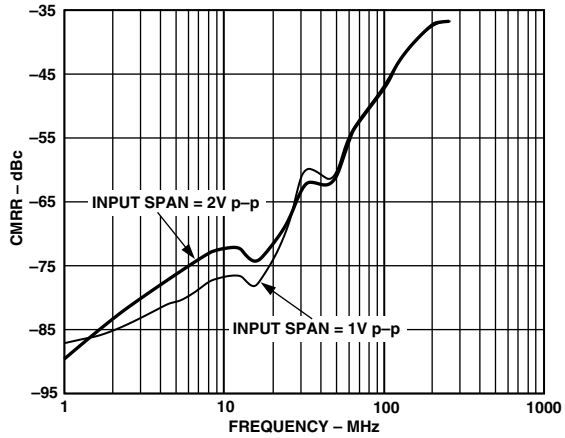
TPC 28. Single-Tone SNR and SFDR vs. A_{IN} at IF = 190 MHz –WCDMA (f_{IN-1} = 190.8 MHz, f_{SAMPLE} = 61.44 MSPS)



TPC 26. Dual-Tone 8K FFT with f_{IN-1} = 239.1 MHz and f_{IN-2} = 240.7 MHz



TPC 29. Dual-Tone SNR and SFDR with f_{IN-1} = 239.1 MHz and f_{IN-2} = 240.7 MHz



TPC 27. CMRR vs. Frequency (A_{IN} = –0 dBFS and CML = 2.5 V)

THEORY OF OPERATION

The AD9226 is a high-performance, single-supply 12-bit ADC. The analog input of the AD9226 is very flexible allowing for both single-ended or differential inputs of varying amplitudes that can be ac- or dc-coupled.

It utilizes a nine-stage pipeline architecture with a wideband, sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. A patented structure is used in the SHA to greatly improve high frequency SFDR/distortion. This also improves performance in IF undersampling applications. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

Factory calibration ensures high linearity and low distortion.

ANALOG INPUT OPERATION

Figure 3 shows the equivalent analog input of the AD9226 which consists of a 750 MHz differential SHA. The differential input structure of the SHA is highly flexible, allowing the device to be easily configured for either a differential or single-ended input. The analog inputs, VINA and VINB, are interchangeable with the exception that reversing the inputs to the VINA and VINB pins results in a data inversion (complementing the output word).

The optimum noise and dc linearity performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 2 V input span) and matched input impedance for VINA and VINB. Only a slight degradation in dc linearity performance exists between the 2 V and 1 V input spans.

High frequency inputs may find the 1 V span better suited to achieve superior SFDR performance. (See Typical Performance Characteristics.)

The ADC samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time it is in hold. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter on the rising edge may cause the input SHA to acquire the wrong value and should be minimized.

When the ADC is driven by an op amp and a capacitive load is switched onto the output of the op amp, the output will momentarily drop due to its effective output impedance. As the output recovers, ringing may occur. To remedy the situation, a series resistor can be inserted between the op amp and the SHA input as shown in Figure 4. A shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H, further reducing current transients seen at the op amp's output.

The optimum size of this resistor is dependent on several factors, including the ADC sampling rate, the selected op amp, and the particular application. In most applications, a 30 Ω to 100 Ω resistor is sufficient.

For noise-sensitive applications, the very high bandwidth of the AD9226 may be detrimental and the addition of a series resistor and/or shunt capacitor can help limit the wideband noise at the ADC's input by forming a low-pass filter. The source impedance driving VINA and VINB should be matched. Failure to provide matching will result in degradation of the AD9226's SNR, THD, and SFDR.

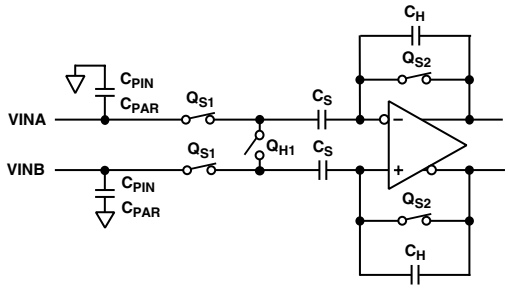


Figure 3. Equivalent Input Circuit

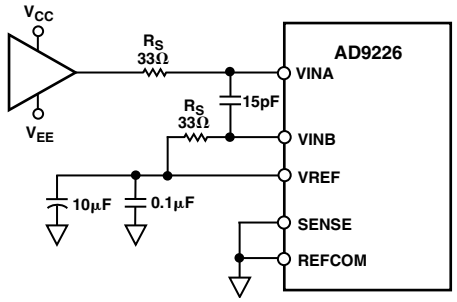


Figure 4. Series Resistor Isolates Switched-Capacitor SHA Input from Op Amp; Matching Resistors Improve SNR Performance

OVERVIEW OF INPUT AND REFERENCE CONNECTIONS

The overall input span of the AD9226 is equal to the potential at the VREF pin. The VREF potential may be obtained from the internal AD9226 reference or an external source (see Reference Operation section).

In differential applications, the center point of the span is obtained by the common-mode level of the signals. In single-ended applications, the center point is the dc potential applied to one input pin while the signal is applied to the opposite input pin. Figures 5a–5f show various system configurations.

DRIVING THE ANALOG INPUTS

The AD9226 has a very flexible input structure allowing it to interface with single-ended or differential input interface circuitry.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular applications performance requirements as well as power supply options.

DIFFERENTIAL DRIVER CIRCUITS

Differential operation requires that VINA and VINB be simultaneously driven with two equal signals that are 180° out of phase with each other.

Differential modes of operation (ac- or dc-coupled input) provide the best THD and SFDR performance over a wide frequency range. They should be considered for the most demanding spectral-based applications (e.g., direct IF conversion to digital).

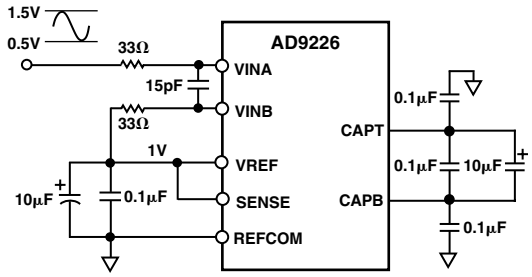


Figure 5a. 1 V Single-Ended Input, Common-Mode Voltage = 1 V

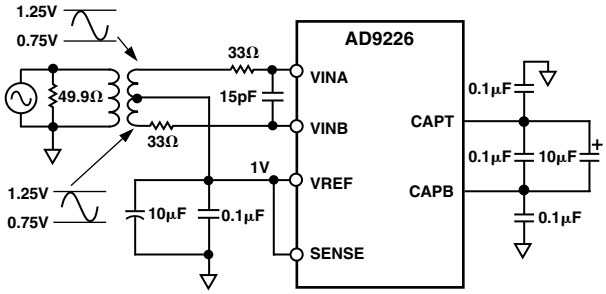


Figure 5b. 1 V Differential Input, Common-Mode Voltage = 1 V

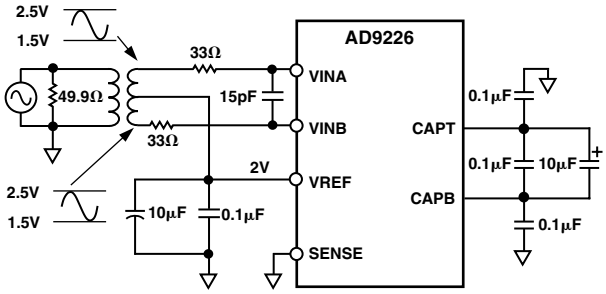


Figure 5c. 2 V Differential Input, Common-Mode Voltage = 2 V

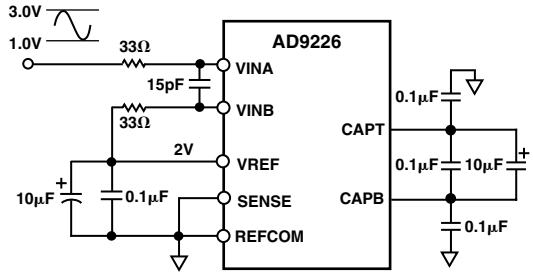


Figure 5d. 2 V Single-Ended Input, Common-Mode Voltage = 2 V

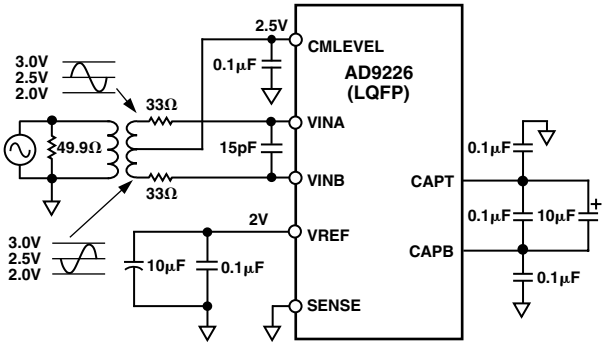


Figure 5e. 2 V Differential Input, Common-Mode Voltage = 2.5 V

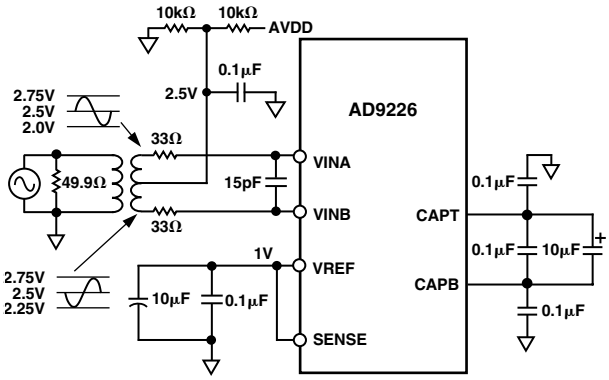


Figure 5f. 1 V Differential Input, Common-Mode Voltage = 2.5 V (Recommended for IF Undersampling)

The differential input characterization for this data sheet was performed using the configuration shown in Figure 7.

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. In systems that do not need to be dc-coupled, an RF transformer with a center tap is the best method to generate differential inputs for the AD9226. It provides all the benefits of operating the ADC in the differential mode without contributing additional noise or distortion. An RF transformer also has the added benefit of providing electrical isolation between the signal source and the ADC. An improvement in THD and SFDR performance can be realized by operating the AD9226 in the differential mode. The performance enhancement between the differential and single-ended mode is most noteworthy as the input frequency approaches and goes beyond the Nyquist frequency (i.e., $f_{IN} > F_S/2$).

The circuit shown in Figure 6a is an ideal method of applying a differential dc drive to the AD9226. It uses an AD8138 to derive a differential signal from a single-ended one. Figure 6b illustrates its performance.

Figure 7 presents the schematic of the suggested transformer circuit. The circuit uses a Minicircuits RF transformer, model T1-1T, which has an impedance ratio of four (turns ratio of 2). The schematic assumes that the signal source has a 50 Ω source impedance. The center tap of the transformer provides a convenient means of level-shifting the input signal to a desired common-mode voltage. In Figure 7 the transformer centertap is connected to a resistor divider at the midsupply voltage.

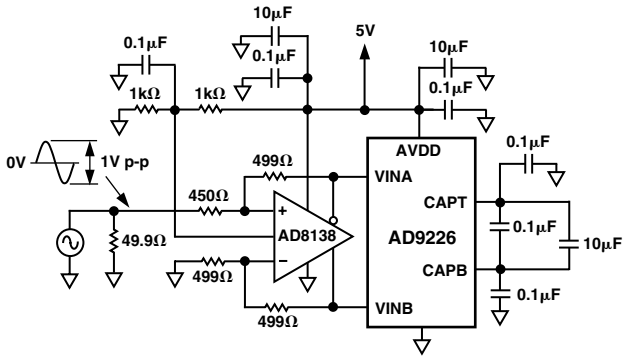


Figure 6a. Direct-Coupled Drive Circuit with AD8138 Differential Op Amp

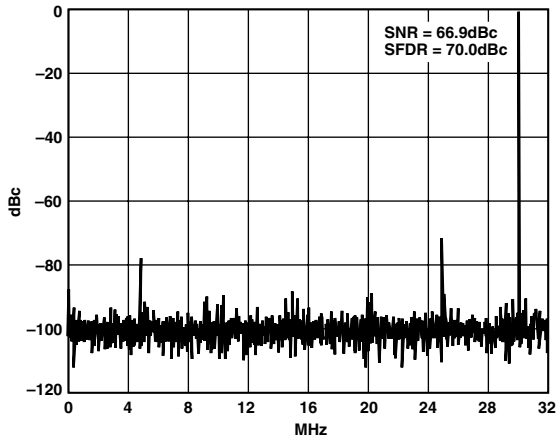


Figure 6b. FS = 65 MSPS, f_{IN} = 30 MHz, Input Span = 1 V p-p

The same midsupply potential may be obtained from the CMLEVEL pin of the AD9226 in the LQFP package.

Referring to Figure 7, a series resistor, R_S, is inserted between the AD9226 and the secondary of the transformer. The value of 33 ohm was selected to specifically optimize both the THD and SNR performance of the ADC. R_S and the internal capacitance help provide a low-pass filter to block high-frequency noise.

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. By selecting a transformer with a higher impedance ratio (e.g., Minicircuits T16-6T with a 1:16 impedance ratio), the signal level is effectively "stepped up" thus further reducing the driving requirements of signal source.

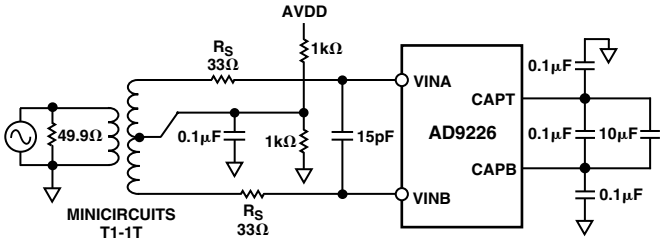


Figure 7. Transformer-Coupled Input

SINGLE-ENDED DRIVER CIRCUITS

The AD9226 can be configured for single-ended operation using dc- or ac-coupling. In either case, the input of the ADC must be driven from an operational amplifier that will not degrade the ADC's performance. Because the ADC operates from a single supply, it will be necessary to level-shift ground-based bipolar signals to comply with its input requirements. Both dc- and ac-coupling provide this necessary function, but each method results in different interface issues which may influence the system design and performance.

Single-ended operation requires that VINA be ac- or dc-coupled to the input signal source, while VINB of the AD9226 be biased to the appropriate voltage corresponding to the middle of the input span. The single-ended specifications for the AD9226 are characterized using Figure 9a circuitry with input spans of 1 V and 2 V. The common-mode level is 2.5 V.

If the analog inputs exceed the supply limits, internal parasitic diodes will turn on. This will result in transient currents within the device. Figure 8 shows a simple means of clamping an input. It uses a series resistor and two diodes. An optional capacitor is shown for ac-coupled applications. A larger series resistor can be used to limit the fault current through D1 and D2. This can cause a degradation in overall performance. A similar clamping circuit can also be used for each input if a differential input signal is being applied. A better method to ensure the input is not overdriven is to use amplifiers powered by a single 5 V supply such as the AD8138.

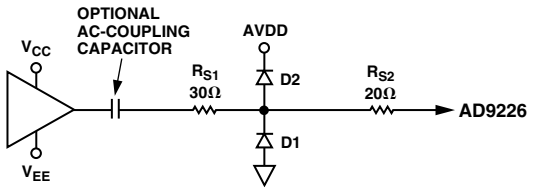


Figure 8. Simple Clamping Circuit

AC-COUPLING AND INTERFACE ISSUES

For applications where ac-coupling is appropriate, the op amp output can be easily level-shifted by means of a coupling capacitor. This has the advantage of allowing the op amp's common-mode level to be symmetrically biased to its midsupply level (i.e., (AVDD/2). Op amps that operate symmetrically with respect to their power supplies typically provide the best ac performance as well as greatest input/output span. Various high-speed performance amplifiers that are restricted to +5 V/–5 V operation and/or specified for 5 V single-supply operation can be easily configured for the 2 V or 1 V input span of the AD9226.

Simple AC Interface

Figure 9a shows a typical example of an ac-coupled, single-ended configuration of the SSOP package. The bias voltage shifts the bipolar, ground-referenced input signal to approximately AVDD/2. The capacitors, C1 and C2, are 0.1 µF ceramic and 10 µF tantalum capacitors in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. The combination of the capacitor and the resistor form a high-pass network with a high-pass –3 dB frequency determined by the equation,

$$f_{-3\,dB} = 1/(2 \times \pi \times R \times (C1 + C2))$$

The low-impedance VREF output can be used to provide dc bias levels to the fixed VINB pin and the signal on VINA. Figure 9b shows the VREF configured for 2.0 V, thus the input range of the ADC is 1.0 V to 3.0 V. Other input ranges could be selected by changing VREF.

When the inputs are biased from the reference (Figure 9b), there may be a slight degeneration of dynamic performance. A midsupply output level is available at the $\overline{CM}$ LEVEL pin of the LQFP package.

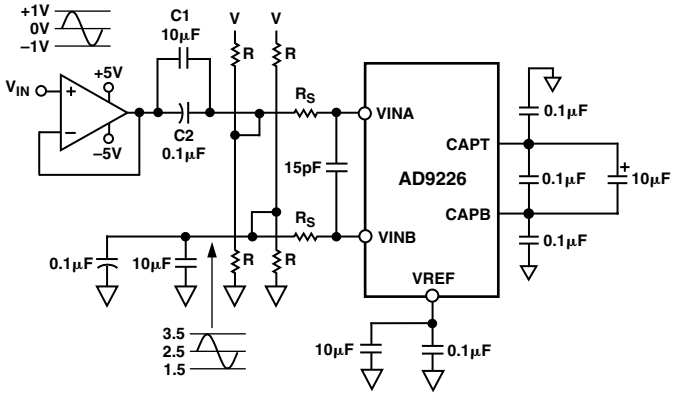


Figure 9a. AC-Coupled Input Configuration

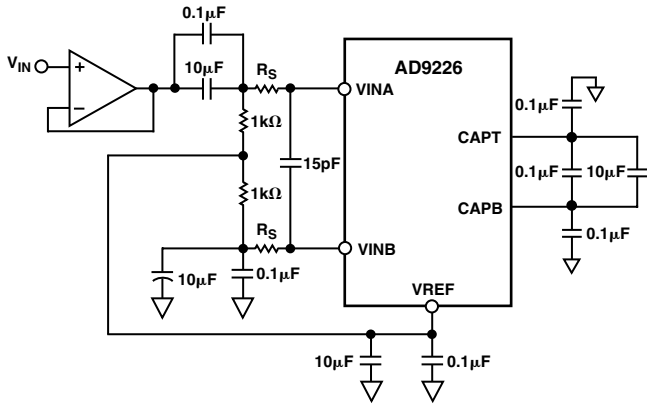


Figure 9b. Alternate AC-Coupled Input Configuration

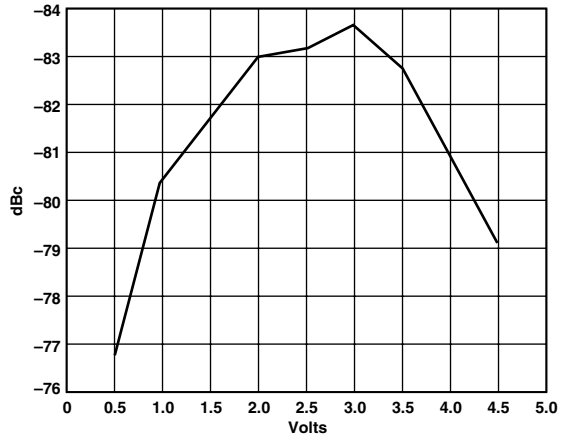


Figure 10. THD vs. Common-Mode Voltage (2 V Differential Input Span, f_{IN} = 10 MHz)

Figure 10 illustrates the relation between common-mode voltage and THD. Note that optimal performance occurs when the reference voltage is set to 2.0 V (input span = 2.0 V).

DC-COUPLING AND INTERFACE ISSUES

Many applications require the analog input signal to be dc-coupled to the AD9226. An operational amplifier can be configured to rescale and level-shift the input signal to make it compatible with the selected input range of the ADC.

The selected input range of the AD9226 should be considered with the headroom requirements of the particular op amp to prevent clipping of the signal. Many of the new high-performance op amps are specified for only ±5 V operation and have limited input/output swing capabilities. Also, since the output of a dual supply amplifier can swing below absolute minimum (–0.3 V), clamping its output should be considered in some applications (see Figure 8). When single-ended, dc-coupling is needed, the use of the AD8138 in a differential configuration (Figure 9a) is highly recommended.

Simple Op Amp Buffer

In the simplest case, the input signal to the AD9226 will already be biased at levels in accordance with the selected input range. It is necessary to provide an adequately low source impedance for the VINA and VINB analog pins of the ADC.

REFERENCE OPERATION

The AD9226 contains an on-board bandgap reference that provides a pin-strappable option to generate either a 1 V or 2 V output. With the addition of two external resistors, the user can generate reference voltages between 1 V and 2 V. See Figures 5a-5f for a summary of the pin-strapping options for the AD9226 reference configurations. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance described later in this section.

Figure 11a shows a simplified model of the internal voltage reference of the AD9226. A reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. The voltage on the VREF pin determines the full-scale input span of the ADC. This input span equals,

Full-Scale Input Span = VREF

The voltage appearing at the VREF pin, and the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains comparators that monitor the voltage at the SENSE pin. If the SENSE pin is tied to AVSS, the switch is connected to the internal resistor network thus providing a VREF of 2.0 V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch will connect to the SENSE pin. This connection will provide a VREF of 1.0 V. An external resistor network will provide an alternative VREF between 1.0 V and 2.0 V (see Figure 12). Another comparator controls internal circuitry that will disable the reference amplifier if the SENSE pin is tied to AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

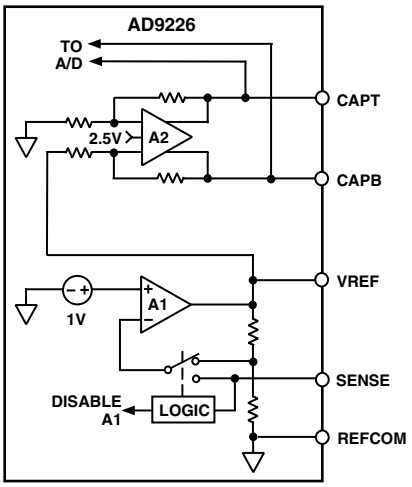


Figure 11a. Equivalent Reference Circuit

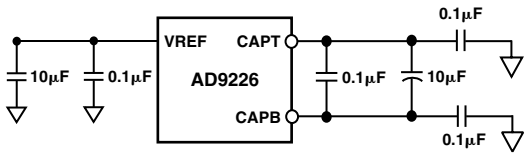


Figure 11b. CAPT and CAPB DC-Coupling

The actual reference voltages used by the internal circuitry of the AD9226 appear on the CAPT and CAPB pins. The voltages on these pins are symmetrical about the analog supply. For proper operation when using an internal or external reference, it is necessary to add a capacitor network to decouple these pins. Figure 11b shows the recommended decoupling network. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 10 ms and should be evaluated in any power-down mode of operation.

USING THE INTERNAL REFERENCE

The AD9226 can be easily configured for either a 1 V p-p input span or 2 V p-p input span by setting the internal reference. Other input spans can be realized with two external gain-setting resistors as shown in Figure 12 of this data sheet, or using an external reference.

Pin Programmable Reference

By shorting the VREF pin directly to the SENSE pin, the internal reference amplifier is placed in a unity-gain mode and the resultant VREF output is 1 V. By shorting the SENSE pin directly to the REFCOM pin, the internal reference amplifier is configured for a gain of 2.0 and the resultant VREF output is 2.0 V. The VREF pin should be bypassed to the REFCOM pin with a 10 μF tantalum capacitor in parallel with a low-inductance 0.1 μF ceramic capacitor as shown in Figure 11b.

Resistor Programmable Reference

Figure 12 shows an example of how to generate a reference voltage other than 1.0 V or 2.0 V with the addition of two external resistors. Use the equation,

$$VREF = 1\ V \times (1 + R1/R2)$$

to determine appropriate values for $R1$ and $R2$. These resistors should be in the 2 kΩ to 10 kΩ range. For the example shown, R1 equals 2.5 kΩ and R2 equals 5 kΩ. From the equation above, the resultant reference voltage on the VREF pin is 1.5 V. This sets the input span to be 1.5 V p-p. The midscale voltage can also be set to VREF by connecting VINB to VREF. Alternatively, the midscale voltage can be set to 2.5 V by connecting VINB to a low-impedance 2.5 V source as shown in Figure 12.

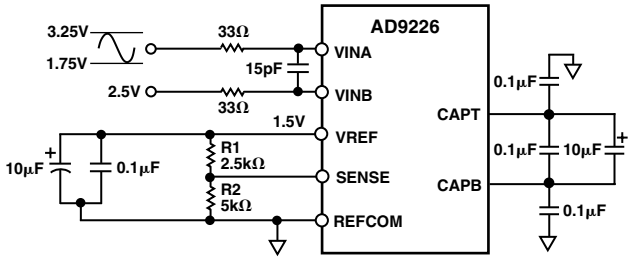


Figure 12. Resistor Programmable Reference (1.5 V p-p Input Span, Differential Input V_{CM} = 2.5 V)

USING AN EXTERNAL REFERENCE

The AD9226 contains an internal reference buffer, A2 (see Figure 11b), that simplifies the drive requirements of an external reference. The external reference must be able to drive about 5 kΩ (±20%) load. Note that the bandwidth of the reference buffer is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to rapidly change the reference voltage in this mode.

Figure 13 shows an example of an external reference driving both VINB and VREF. In this case, both the common-mode voltage and input span are directly dependent on the value of VREF. Both the input span and the center of the input span are equal to the external VREF. Thus the valid input range extends from (VREF + VREF/2) to (VREF – VREF/2). For example, if the REF191, a 2.048 V external reference, is selected, the input span extends to 2.048 V. In this case, 1 LSB of the AD9226 corresponds to 0.5 mV. It is essential that a minimum of a 10 μF capacitor, in parallel with a 0.1 μF low-inductance ceramic capacitor, decouple the reference output to ground.

To use an external reference, the SENSE pin must be connected to AVDD. This connection will disable the internal reference.

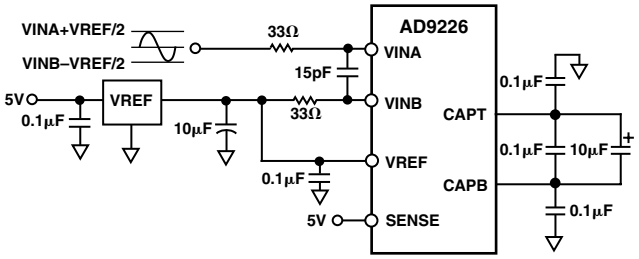


Figure 13. Using an External Reference

MODE CONTROLS

Clock Stabilizer

The clock stabilizer is a circuit that desensitizes the ADC from clock duty cycle variations. The AD9226 eases system clock constraints by incorporating a circuit that restores the internal duty cycle to 50%, independent of the input duty cycle. Low jitter on the rising edge (sampling edge) of the clock is preserved while the noncritical falling edge is generated on-chip.

It may be desirable to disable the clock stabilizer, and may be necessary when the clock frequency speed is varied or completely stopped. Once the clock frequency is changed, over 100 clock cycles may be required for the clock stabilizer to settle to a different speed. When the stabilizer is disabled, the internal switching will be directly affected by the clock state. If the external clock is high, the SHA will be in hold. If the clock pulse is low, the SHA will be in track. TPC 16 shows the benefits of using the clock stabilizer. See Tables I and III.

Data Format Select (DFS)

The AD9226 may be set for binary or two's complement data output formats. See Tables I and II.

SSOP Package

The SSOP mode control (Pin 22) has two functions. It enables/disables the clock stabilizer and determines the output data format. The exact functions of the mode pin are outlined in Table I.

Table I. Mode Select (SSOP)

Mode	DFS	Clock Duty Cycle Shaping
DNC	Binary	Clock Stabilizer Disabled
AVDD	Binary	Clock Stabilizer Enabled
GND	Two's Complement	Clock Stabilizer Enabled
10 kΩ Resistor	Two's Complement To GND	Clock Stabilizer Disabled

LQFP Package

Pin 35 of the LQFP package determines the output data format (DFS). If it is connected to AVSS, the output word will be straight binary. If it is connected to AVDD, the output data format will be two's complement. See Table II.

Pin 43 of the LQFP package controls the clock stabilizer function of the AD9226. If the pin is connected to AVSS, both clock edges will be used in the conversion architecture. When Pin 43 is connected to AVDD, the internal duty cycle will be determined by the clock stabilizer function within the ADC. See Table III.

Table II. DFS Pin Controls

DFS Function	Pin 35 Connection
Straight Binary	AVSS
Two's Complement	AVDD

Table III. Clock Stabilizer Pin

Clock Restore Function	Pin 43 Connection
Clock Stabilizer Enabled	AVDD
Clock Stabilizer Disabled	AVSS

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

Table IV details the relationship among the ADC input, OTR, and straight binary output.

Table IV. Output Data Format

Input (V)	Condition (V)	Binary Output Mode	Two's Complement Mode	OTR
VINA–VINB	< – VREF	0000 0000 0000	1000 0000 0000	1
VINA–VINB	= – VREF	0000 0000 0000	1000 0000 0000	0
VINA–VINB	= 0	1000 0000 0000	0000 0000 0000	0
VINA–VINB	= + VREF – 1 LSB	1111 1111 1111	0111 1111 1111	0
VINA–VINB	≥ + VREF	1111 1111 1111	0111 1111 1111	1

Out of Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the converter. OTR is a digital output that is updated along with the data output corresponding to the particular sampled analog input voltage. Hence, OTR has the same pipeline delay (latency) as the digital data. It is LOW when the analog input voltage is within the analog input range. It is HIGH when the analog input voltage exceeds the input range as shown in Figure 14. OTR will remain HIGH until the analog input returns within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table V is a truth table for the over/underrange circuit in Figure 15, which uses NAND gates. Systems requiring programmable gain conditioning of the AD9226 input signal can immediately detect an out-of-range condition, thus eliminating gain selection iterations. Also, OTR can be used for digital offset and gain calibration.

Table V. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

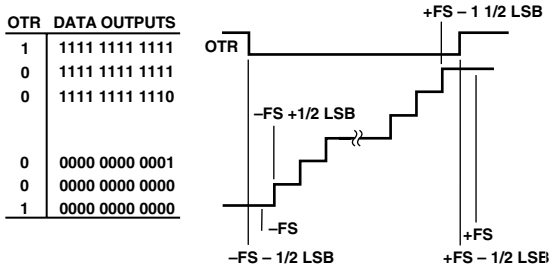


Figure 14. OTR Relation to Input Voltage and Output Data

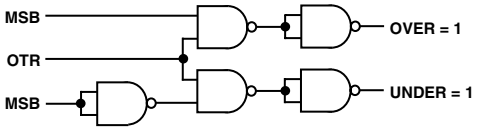


Figure 15. Overrange or Underrange Logic

Digital Output Driver Considerations
The AD9226 output drivers can be configured to interface with 5 V or 3.3 V logic families by setting DRVDD to 5 V or 3.3 V respectively. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan outs may require external buffers or latches.

OEB Function (Three-State)
The LQFP-packaged AD9226 has Three-State (OEB) ability. If the OEB pin is held low, the output data drivers are enabled. If the OEB pin is high, the output data drivers are placed in a high impedance state. It is not intended for rapid access to buss.

Clock Input Considerations
High-speed, high-resolution ADCs are sensitive to the quality of the clock input. The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic performance of the AD9226. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low-jitter crystal controlled oscillators make the best clock sources.

The quality of the clock input, particularly the rising edge, is critical in realizing the best possible jitter performance of the part. Faster rising edges often have less jitter.

Clock Input and Power Dissipation
Most of the power dissipated by the AD9226 is from the analog power supplies. However, lower clock speeds will reduce digital current. Figure 16 shows the relationship between power and clock rate.

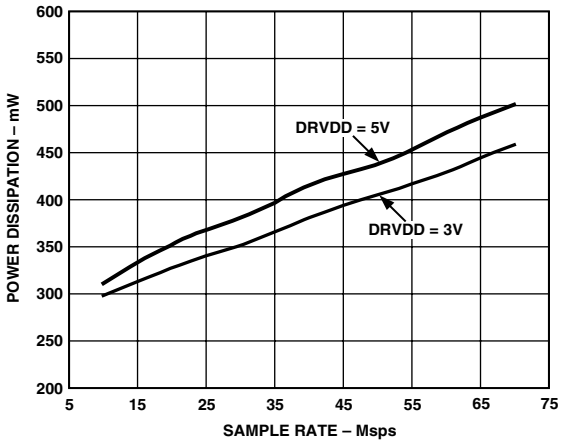


Figure 16. Power Consumption vs. Sample Rate

GROUNDING AND DECOUPLING
Analog and Digital Grounding
Proper grounding is essential in any high-speed, high-resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9226 features separate analog and driver ground pins, it should be treated as an analog component. The AVSS and DRVSS pins must be joined together directly under the AD9226. A solid ground plane under the ADC is acceptable if the power and ground return currents are carefully managed.

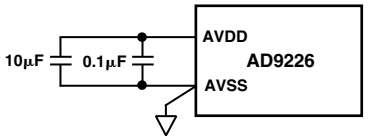


Figure 17. Analog Supply Decoupling

Analog and Digital Driver Supply Decoupling
The AD9226 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AVDD (analog power) should be decoupled to AVSS (analog ground). The AVDD and AVSS pins are adjacent to one another. Also, DRVDD (digital power) should be decoupled to DRVDD (digital ground). The decoupling capacitors (especially 0.1 µF) should be located as close to the pins as possible. Figure 17 shows the recommended decoupling for the pair of analog supplies; 0.1 µF ceramic chip and 10 µF tantalum capacitors should provide adequately low impedance over a wide frequency range.

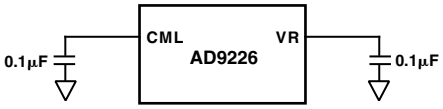


Figure 18. CML Decoupling (LQFP)

Bias Decoupling
The CML and VR are analog bias points used internally by the AD9226. These pins must be decoupled with at least a 0.1 µF capacitor as shown in Figure 18. The dc level of CML is approximately AVDD/2. This voltage should be buffered if it is to be used for any external biasing. CML and VR outputs are only available in the LQFP package.

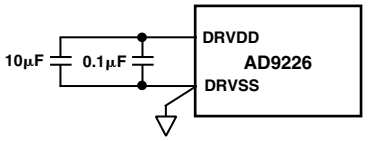


Figure 19. Digital Supply Decoupling

CML
The LQFP-packaged AD9226 has a midsupply reference point. This midsupply point is used within the internal architecture of the AD9226 and must be decoupled with a 0.1 µF capacitor. It will source or sink a load of up to 300 µA. If more current is required, it should be buffered with a high impedance amplifier.

VR

VR is an internal bias point on the LQFP package. It must be decoupled to ground with a 0.1 μF capacitor.

The digital activity on the AD9226 chip falls into two general categories: correction logic and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided.

For the digital decoupling shown in Figure 19, 0.1 μF ceramic chip and 10 μF tantalum capacitors are appropriate. Reasonable capacitive loads on the data pins are less than 20 pF per bit. Applications involving greater digital loads should consider increasing the digital decoupling proportionally and/or using external buffers/latches.

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the power supply connector to reduce low-frequency ripple to negligible levels.

EVALUATION BOARD AND TYPICAL BENCH CHARACTERIZATION TEST SETUP

The AD9226 evaluation board is configured to operate upon applying both power and the analog and clock input signals. It provides three possible analog input interfaces to characterize the AD9226's ac and dc performance. For ac characterization, it provides a transformer coupled input with the common-mode input voltage (CMV) set to AVDD/2. Note, the evaluation board is shipped with a transformer coupled interface and a 2 V input span. For differential dc coupled applications, the evaluation board has provisions to be driven by the AD8138 amplifier. If a single-ended input is desired, it may be driven through the S3 connector. The various input signal options are accessible by the jumper connections. Refer to the Evaluation Board schematic.

The clock input signal to the AD9226 evaluation board can be applied to one of two inputs, CLOCK and AUXCLK. The CLOCK input should be selected if the frequency of the input clock signal is at the target sample rate of the AD9226. The input clock signal is ac-coupled and level-shifted to the switching threshold of a 74VHC02 clock driver. The AUXCLK input should be selected in applications requiring the lowest jitter and SNR performance (i.e., IF Undersampling characterization). It allows the user to apply a clock input signal that is 4× the target sample rate of the AD9226. A low-jitter, differential divide-by-4 counter, the MC100EL33D, provides a 1× clock output that is subsequently returned back to the CLOCK input via JP7. For example, a 260 MHz signal (sinusoid) will be divided down to a 65 MHz signal for clocking the ADC. Note, R1 must be removed with the AUXCLK interface. Lower jitter is often achieved with this interface since many RF signal generators display improved phase noise at higher output frequencies and the slew rate of the sinusoidal output signal is 4× that of a 1× signal of equal amplitude.

Figure 20 shows the bench characterization setup used to evaluate the AD9226's ac performance for many of the data sheet characterization curves. Signal and Clock RF generators A and B are high-frequency, "very" low-phase noise frequency sources. These generators should be phase locked by sharing the same 10 MHz REF signal (located on the instruments back panel) to allow for nonwindowed, coherent FFTs. Also, the AUXCLK option on the AD9226 evaluation board should be used to achieve the best SNR performance. Since the distortion and broadband noise of an RF generator can often be a limiting factor in measuring the true performance of an ADC, a high Q passive bandpass filter should be inserted between the generator and AD9226 evaluation board.

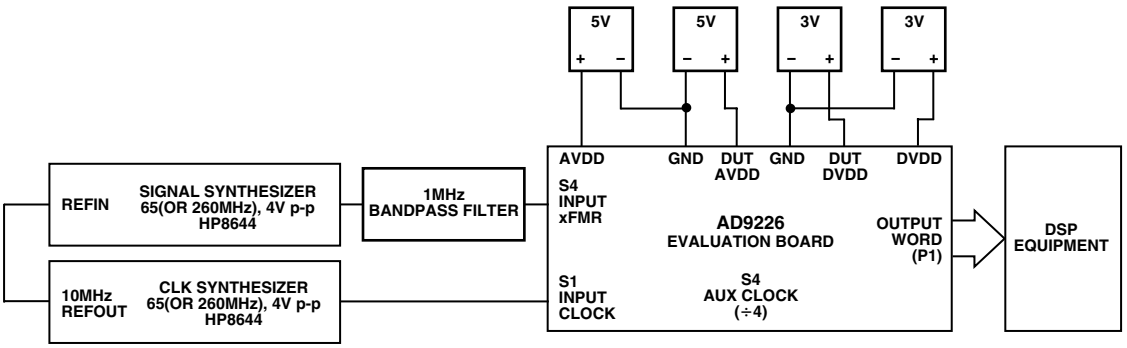


Figure 20. Evaluation Board Connections

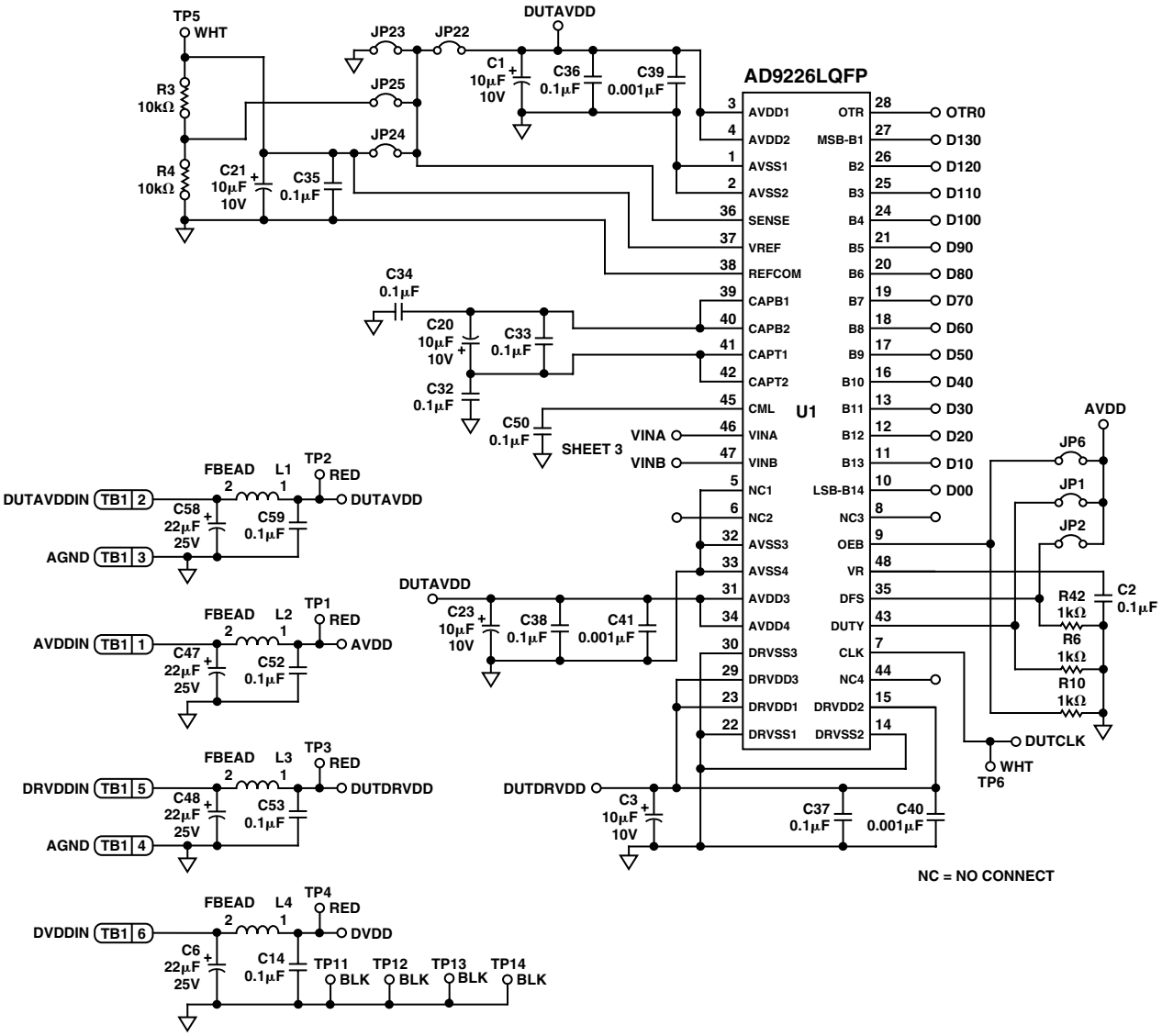


Figure 21. AD9226 Evaluation Board

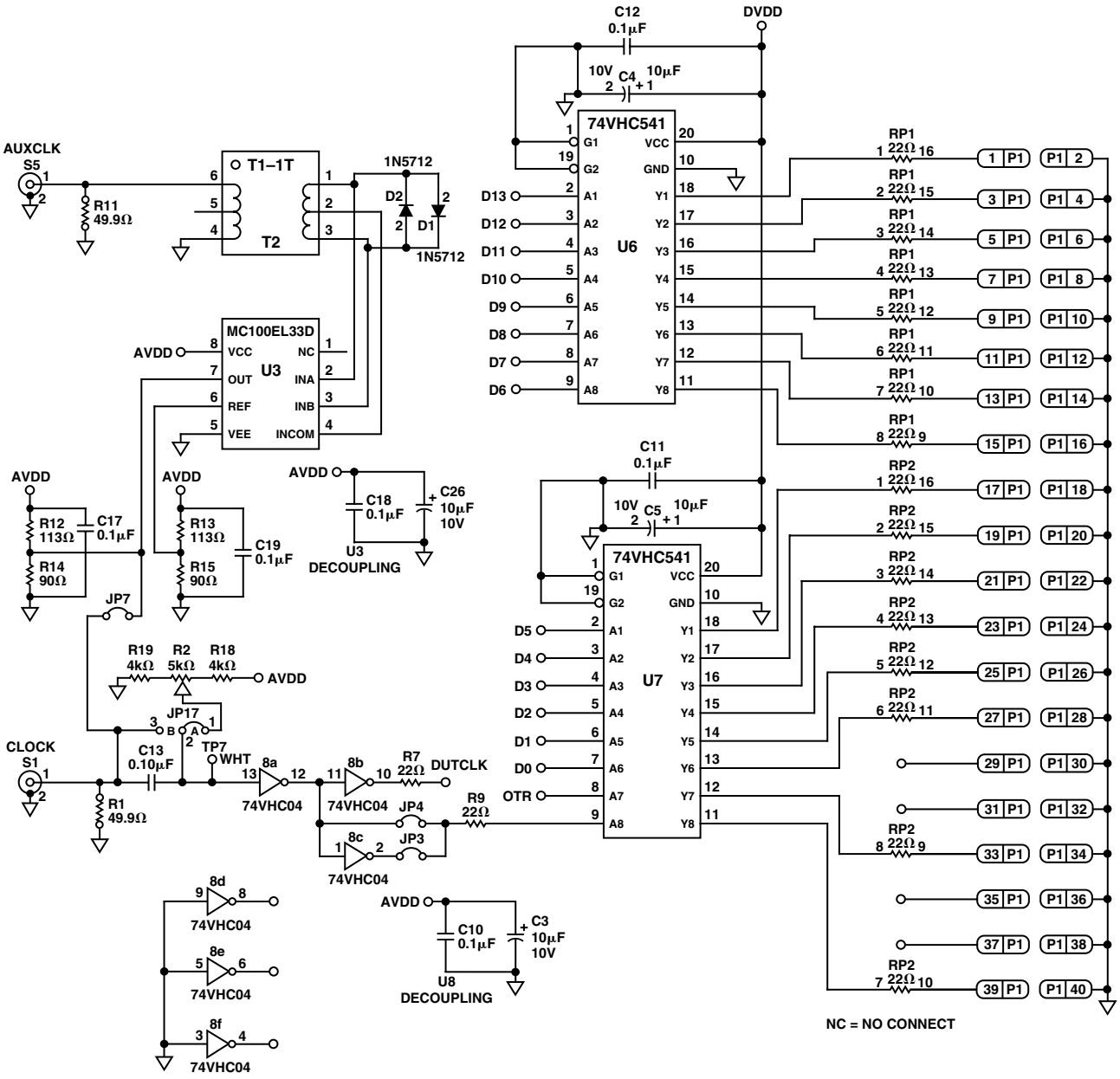


Figure 22. AD9226 Evaluation Board

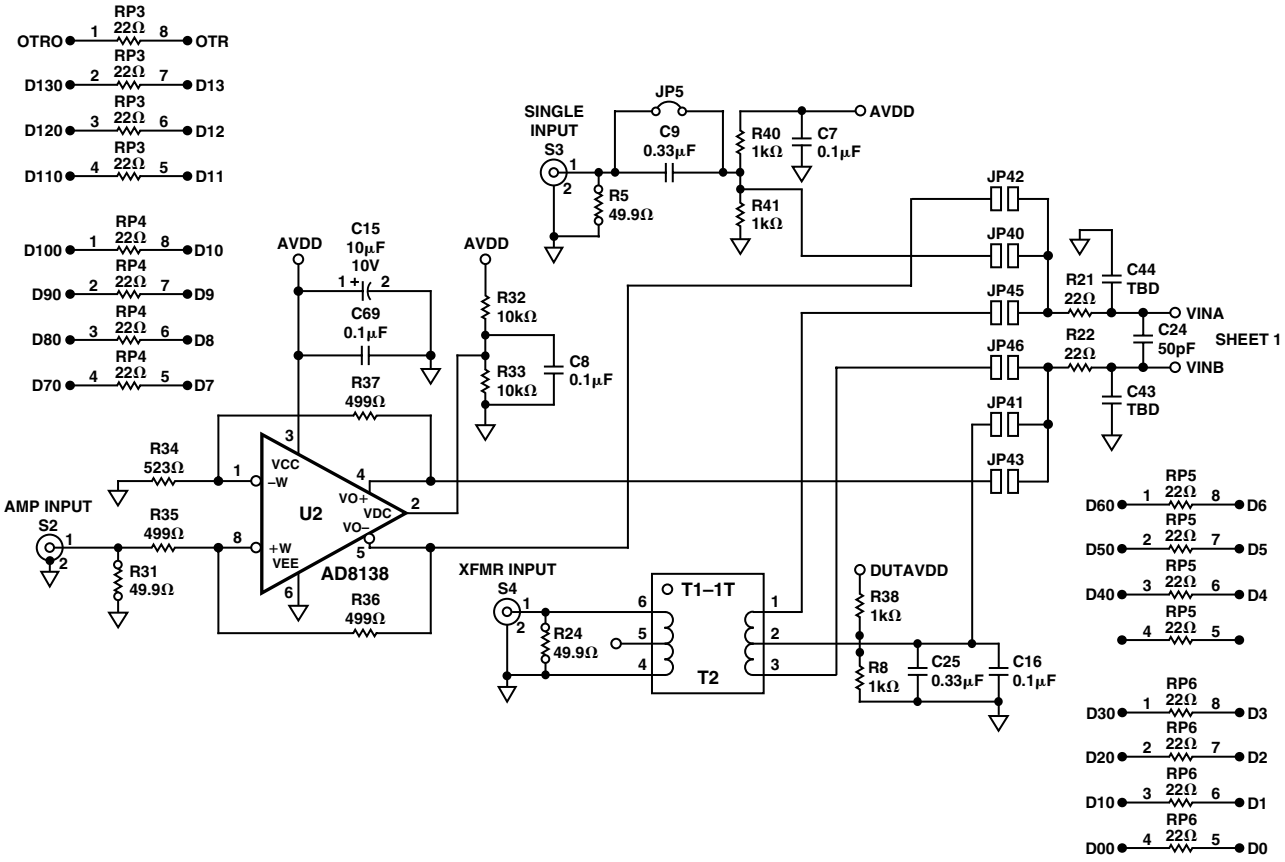


Figure 23. AD9226 Evaluation Board

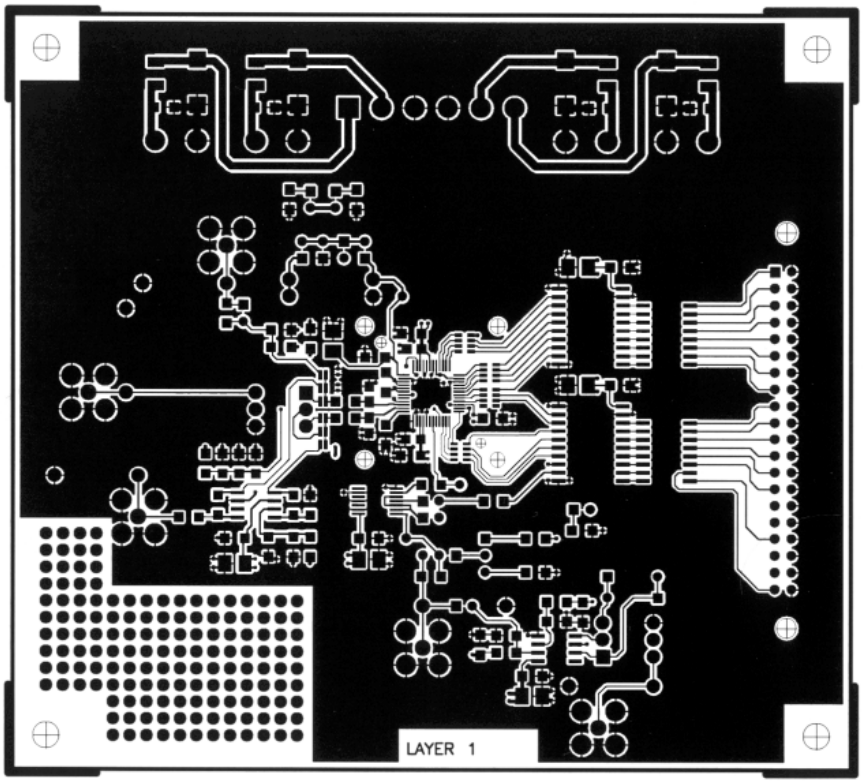


Figure 24. Evaluation Board Component Side Layout (Not to Scale)

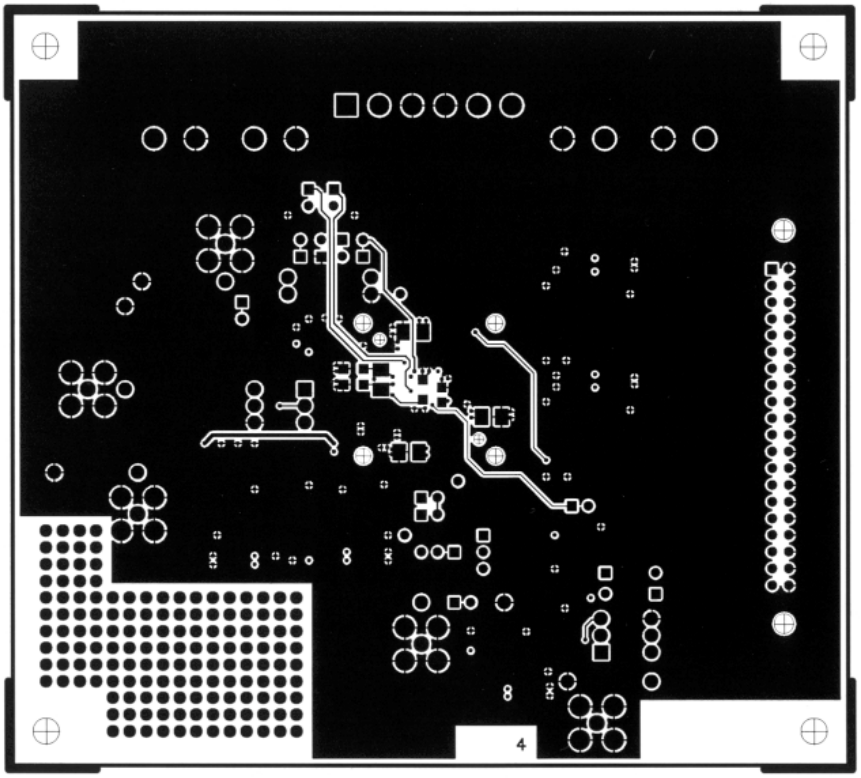


Figure 25. Evaluation Board Solder Side Layout (Not to Scale)

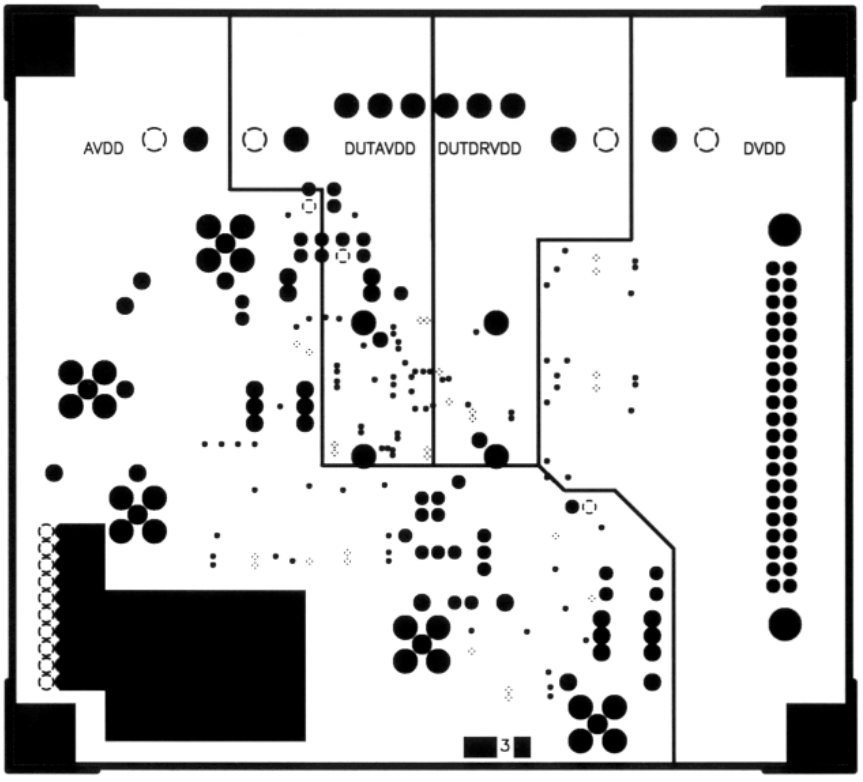


Figure 26. Evaluation Board Power Plane

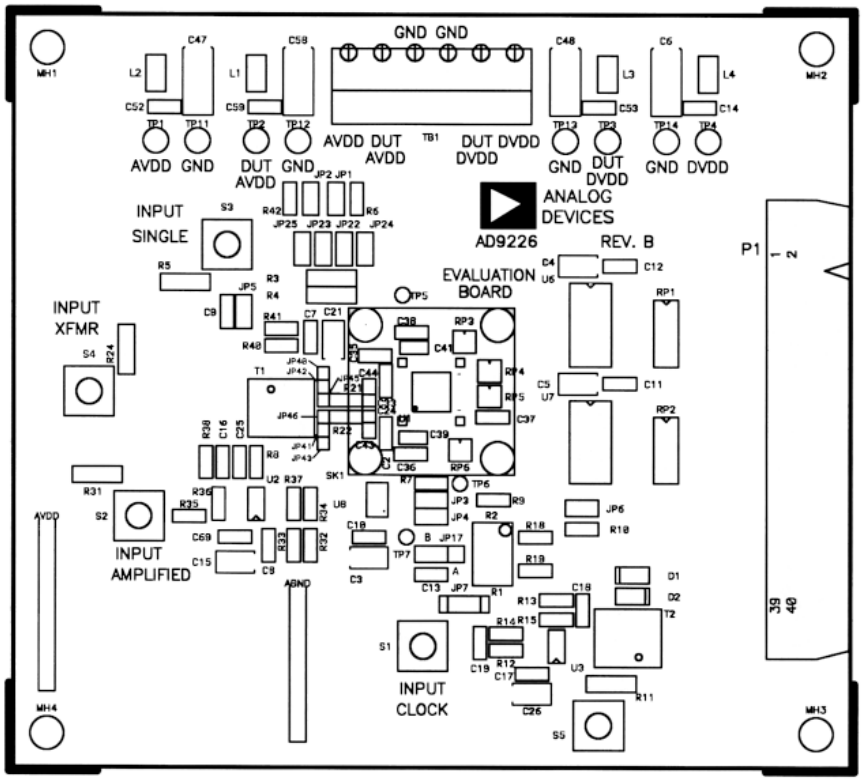


Figure 27. Evaluation Board Ground Plane

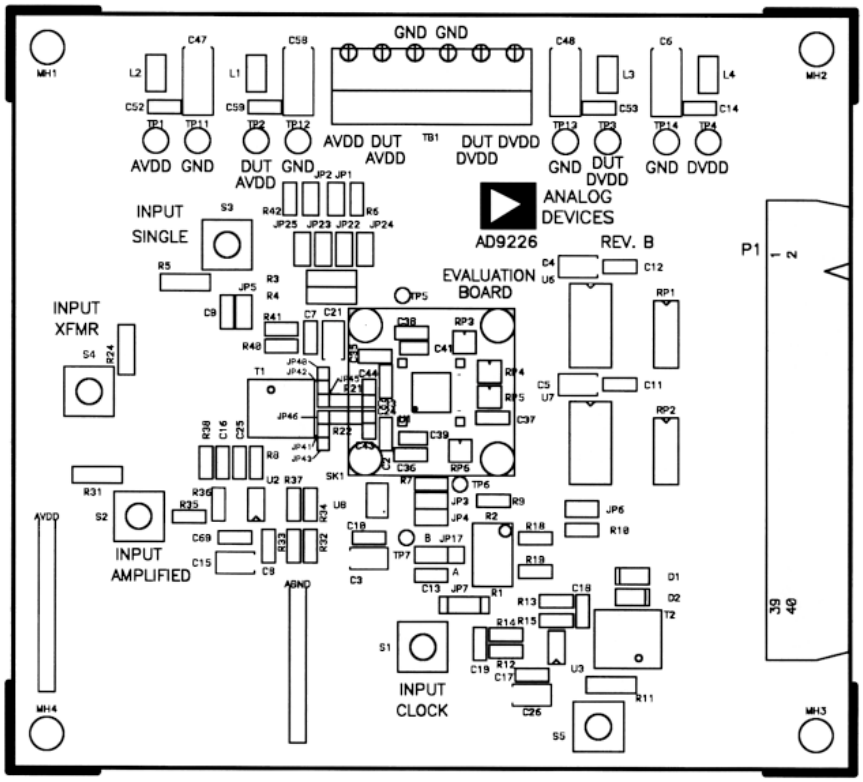


Figure 28. Evaluation Board Component Side (Not to Scale)

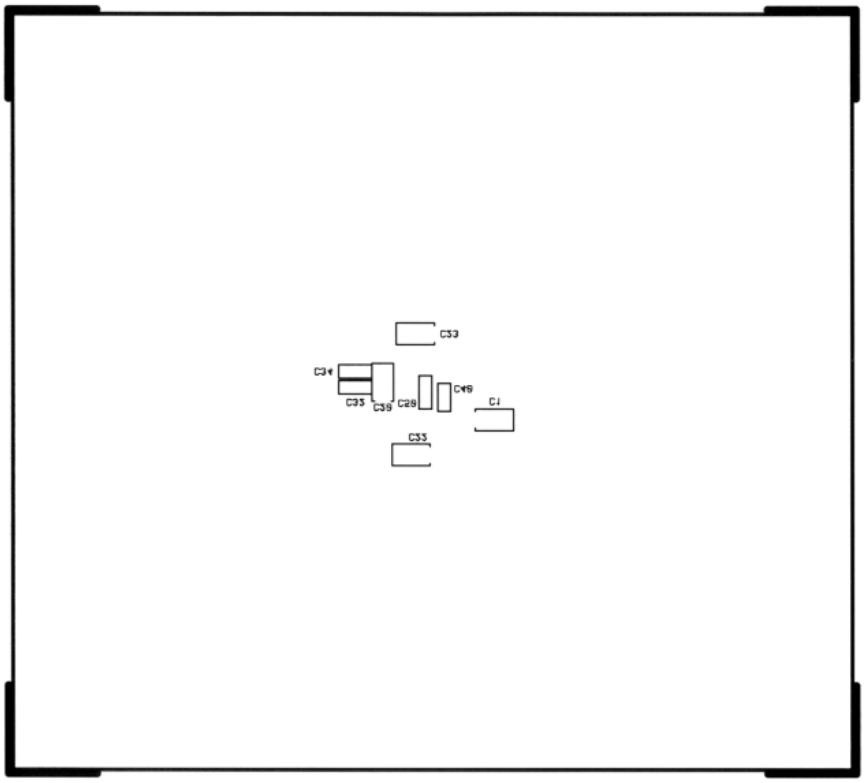
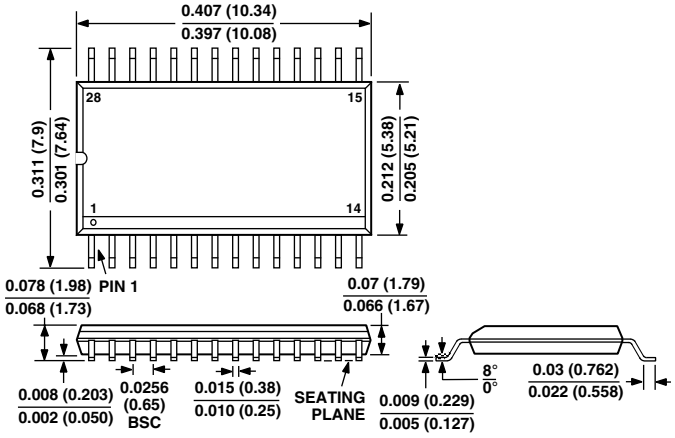


Figure 29. Evaluation Board Solder Side (Not to Scale)

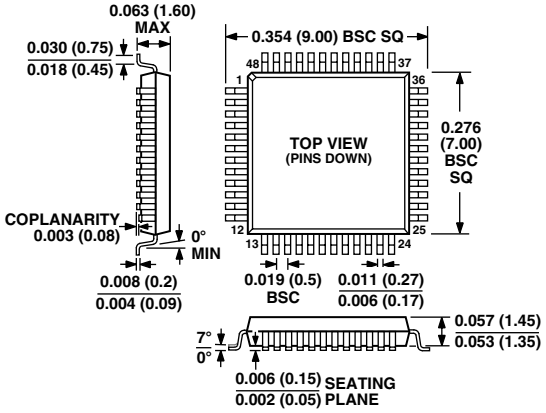
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead Shrink Small Outline (RS-28)



48-Lead Thin Plastic Quad Flatpack (ST-48)



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