'290, 'LS290 . . . DECADE COUNTERS
'293, 'LS293 . . . 4-BIT BINARY COUNTERS

- GND and $V_{CC}$ on Corner Pins (Pins 7 and 14 Respectively)

## description

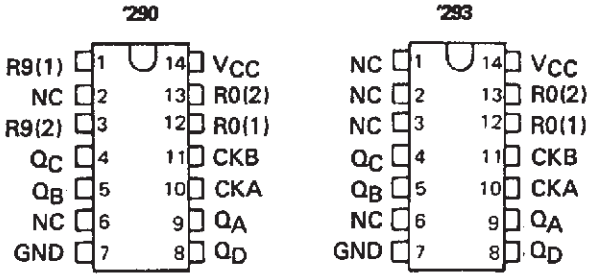
The SN54290/SN74290, SN54LS290/SN74LS290, SN54293/SN74293, and SN54LS293/SN74LS293 counters are electrically and functionally identical to the SN5490A/SN7490A, SN54LS90/SN74LS90, SN5493A/SN7493A, and SN54LS93/SN74LS93, respectively. Only the arrangement of the terminals has been changed for the '290, 'LS290, '293, and 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and 'LS290 and divide-by-eight for the '293 and 'LS293.

All of these counters have a gated zero reset and the '290 and 'LS290 also have gated set-to-nine inputs for use in BCD nine's complement applications.

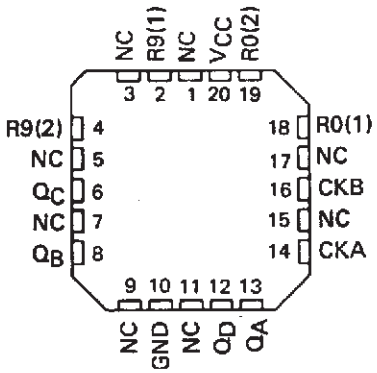
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the $Q_A$ output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 and 'LS290 counters by connecting the $Q_D$ output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output $Q_A$.

**SN54290, SN54LS290, SN54293, SN54LS293 . . . J OR W PACKAGE**
**SN74290, SN74293 . . . N PACKAGE**
**SN74LS290, SN74LS293 . . . D OR N PACKAGE**
**(TOP VIEW)**

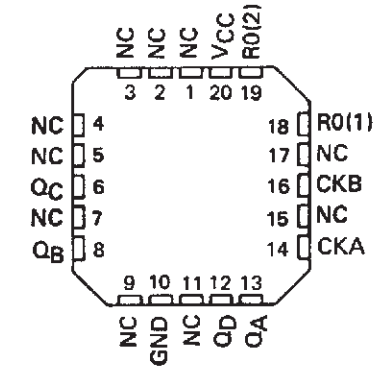



**SN54LS290, SN54LS293 . . . FK PACKAGE**
**(TOP VIEW)**

**'LS290**




**'LS293**




NC – No internal connection

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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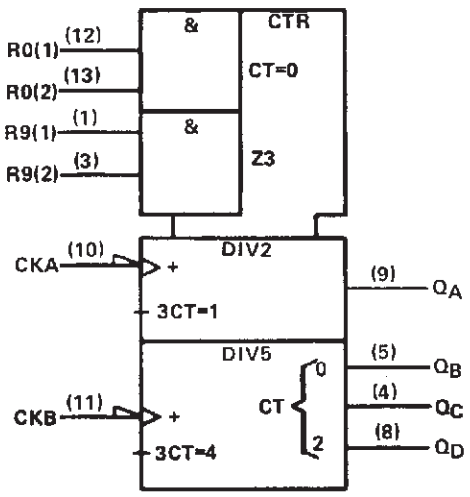
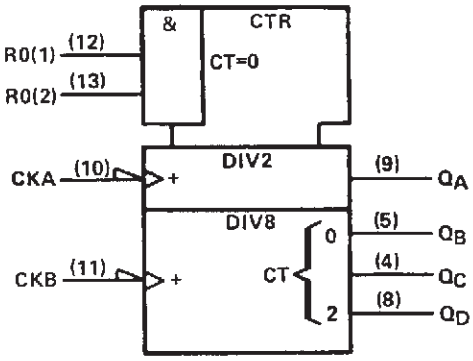
## logic symbols†

'290, 'LS290




'293, 'LS293




† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

**'290, 'LS290**
**BCD COUNT SEQUENCE**
**(See Note A)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |

**'290, 'LS290**
**BI-QUINARY (5-2)**
**(See Note B)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_A$ | $Q_D$ | $Q_C$ | $Q_B$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | H | L | L | L |
| 6 | H | L | L | H |
| 7 | H | L | H | L |
| 8 | H | L | H | H |
| 9 | H | H | L | L |

**'290, 'LS290**
**RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | | | OUTPUT | | | |
|---|---|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $R_{9(1)}$ | $R_{9(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | X | L | L | L | L |
| H | H | X | L | L | L | L | L |
| X | X | H | H | H | L | L | H |
| X | L | X | L | COUNT | | | |
| L | X | L | X | COUNT | | | |
| L | X | X | L | COUNT | | | |
| X | L | L | X | COUNT | | | |

**'293, 'LS293**
**RESET/COUNT FUNCTION TABLE**

| RESET INPUTS | | OUTPUT | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | COUNT | | | |
| X | L | COUNT | | | |

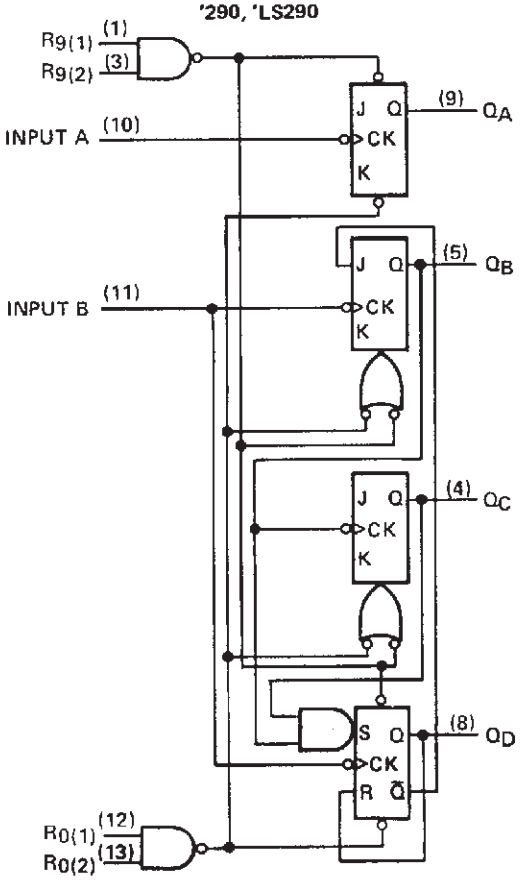
**'293, 'LS293**
**COUNT SEQUENCE**
**(See Note C)**

| COUNT | OUTPUT | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

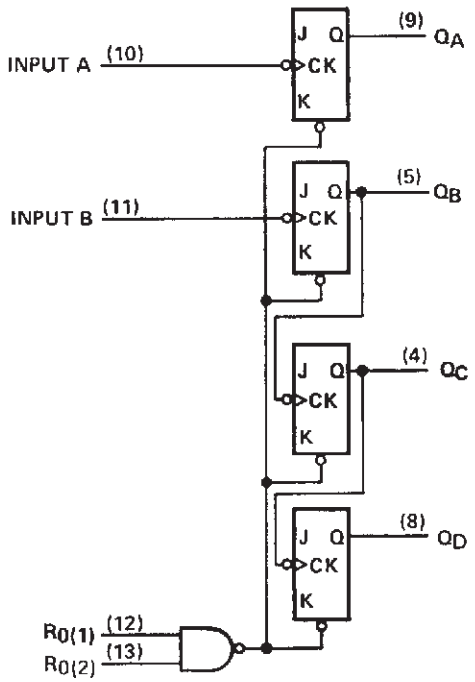
NOTES: A. Output $Q_A$ is connected to input B for BCD count.
B. Output $Q_D$ is connected to input A for bi-quinary count.
C. Output $Q_A$ is connected to input B.
D. H = high level, L = low level, X = irrelevant

## logic diagrams (positive logic)

**'290, 'LS290**

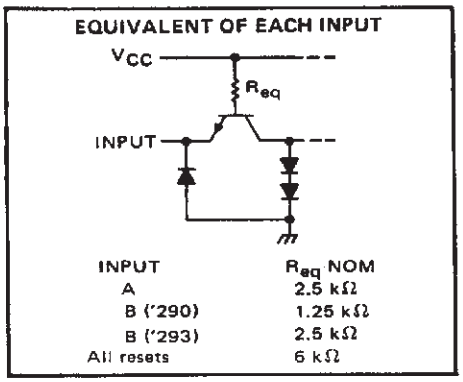


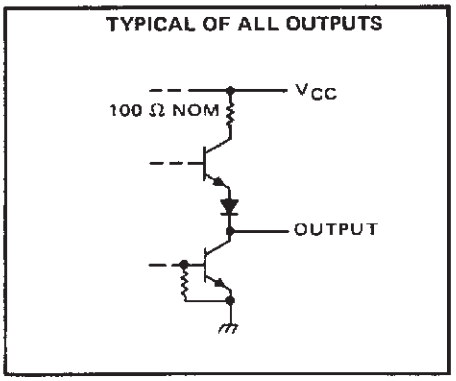

**'293, 'LS293**




Pin numbers shown are for D, J, N, and W packages.
The J and K inputs shown without connection are for reference only and are functionally at a high level.

## schematics of inputs and outputs




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two $R_0$ inputs, and for the '290 circuit, it also applies between the two R9 inputs.

## recommended operating conditions

| | | SN54' | | | SN74' | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | | 16 | | | 16 | mA |
| Count frequency, $f_{count}$ | A input | 0 | | 32 | 0 | | 32 | MHz |
| | B input | 0 | | 16 | 0 | | 16 | |
| Pulse width, $t_w$ | A input | 15 | | | 15 | | | ns |
| | B input | 30 | | | 30 | | | |
| | Reset inputs | 15 | | | 15 | | | |
| Reset inactive-state setup time, $t_{su}$ | | 25 | | | 25 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | '290 MIN | '290 TYP‡ | '290 MAX | '293 MIN | '293 TYP‡ | '293 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA¶ | | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | Any reset | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | | A input | | | | | 80 | | | 80 | |
| | | B input | | | | | 120 | | | 80 | |
| $I_{IL}$ | Low-level input current | Any reset | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| | | A input | | | | | −3.2 | | | −3.2 | |
| | | B input | | | | | −4.8 | | | −3.2 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | SN54' | −20 | | −57 | −20 | | −57 | mA |
| | | | | SN74' | −18 | | −57 | −18 | | −57 | |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, See Note 3 | | | 29 | 42 | | 26 | 39 | mA |

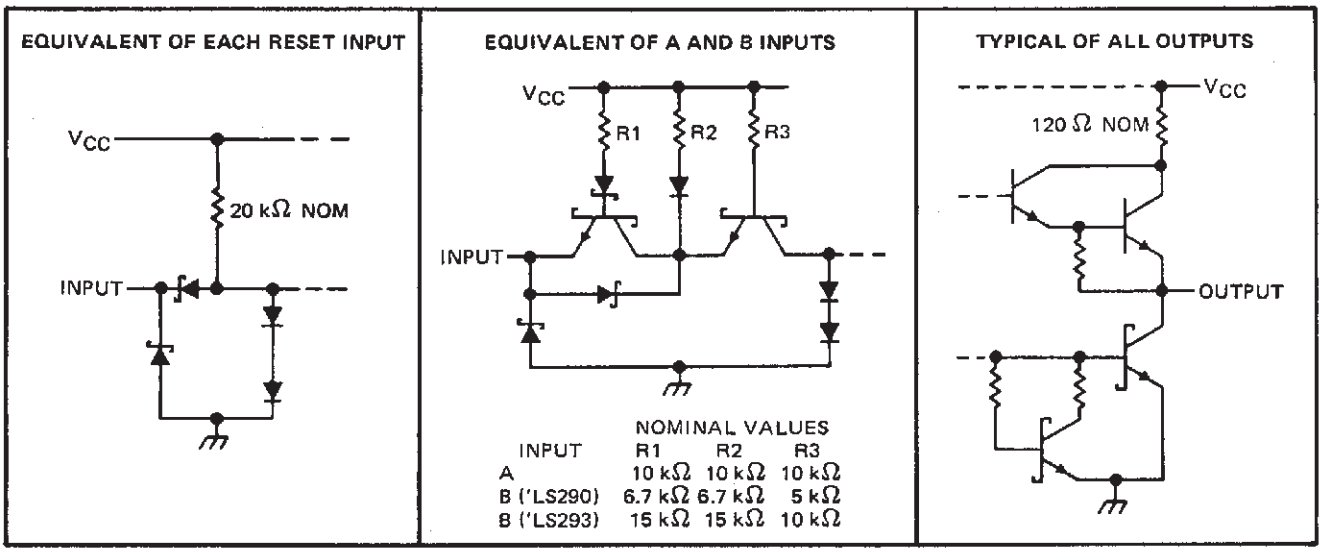
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
¶$Q_A$ outputs are tested at $I_{OL}$ = 16 mA plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER# | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | '290 MIN | '290 TYP | '290 MAX | '293 MIN | '293 TYP | '293 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 4 | 32 | 42 | | 32 | 42 | | MHz |
| | B | $Q_B$ | | 16 | | | 16 | | | |
| $t_{PLH}$ | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 12 | 18 | |
| $t_{PLH}$ | A | $Q_D$ | | | 32 | 48 | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 34 | 50 | | 46 | 70 | |
| $t_{PLH}$ | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | | 14 | 21 | |
| $t_{PLH}$ | B | $Q_C$ | | | 21 | 32 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 23 | 35 | |
| $t_{PLH}$ | B | $Q_D$ | | | 21 | 32 | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | ns |
| $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | ns |
| $t_{PHL}$ | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | |

#$f_{max}$ = maximum count frequency
$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

### schematics of inputs and outputs




### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 5) . . . . . 7 V
Input voltage: R inputs . . . . . 7 V
A and B inputs . . . . . 5.5 V
Operating free-air temperature range: SN54LS290, SN54LS293 . . . . . −55°C to 125°C
SN74LS290, SN74LS293 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 5: Voltage values are with respect to network ground terminal.

### recommended operating conditions

| | | SN54LS' | | | SN74LS' | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | | 4 | | | 8 | mA |
| Count frequency, $f_{count}$ | A input | 0 | | 32 | 0 | | 32 | MHz |
| | B input | 0 | | 16 | 0 | | 16 | |
| Pulse width, $t_w$ | A input | 15 | | | 15 | | | ns |
| | B input | 30 | | | 30 | | | |
| | Reset inputs | 30 | | | 30 | | | |
| Reset inactive-state setup time, $t_{su}$ | | 25 | | | 25 | | | ns |
| Operating free-air temperature, $T_A$ | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS† | | | SN54LS' MIN | SN54LS' TYP‡ | SN54LS' MAX | SN74LS' MIN | SN74LS' TYP‡ | SN74LS' MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max, | $V_{IH}$ = 2 V, $I_{OH}$ = −400 μA | | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = MIN, $V_{IL}$ = $V_{IL}$ max | $V_{IH}$ = 2 V, | $I_{OL}$ = 4 mA¶ | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | | | $I_{OL}$ = 8 mA¶ | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | Any reset | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| | | A input | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 0.2 | | | 0.2 | |
| | | B of 'LS290 | | | | | | 0.4 | | | 0.4 | |
| | | B of 'LS293 | | | | | | 0.2 | | | 0.2 | |
| $I_{IH}$ | High-level input current | Any reset | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| | | A input | | | | | | 40 | | | 40 | |
| | | B of 'LS290 | | | | | | 80 | | | 80 | |
| | | B of 'LS293 | | | | | | 40 | | | 40 | |
| $I_{IL}$ | Low-level input current | Any reset | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| | | A input | | | | | | −2.4 | | | −2.4 | |
| | | B of 'LS290 | | | | | | −3.2 | | | −3.2 | |
| | | B of 'LS293 | | | | | | −1.6 | | | −1.6 | |
| $I_{OS}$ | Short-circuit output current§ | | $V_{CC}$ = MAX | | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | | $V_{CC}$ = MAX, | See Note 3 | 'LS290 | | 9 | 15 | | 9 | 15 | mA |
| | | | | | 'LS293 | | 9 | 15 | | 9 | 15 | |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
¶$Q_A$ outputs are tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: $I_{CC}$ is measured with all outputs open, both $R_0$ inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

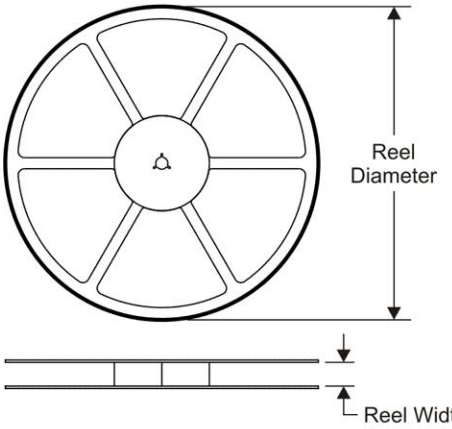
## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER# | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | 'LS290 MIN | 'LS290 TYP | 'LS290 MAX | 'LS293 MIN | 'LS293 TYP | 'LS293 MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| $f_{max}$ | A | $Q_A$ | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 4 | 32 | 42 | | 32 | 42 | | MHz |
| | B | $Q_B$ | | 16 | | | 16 | | | |
| $t_{PLH}$ | A | $Q_A$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 12 | 18 | | 12 | 18 | |
| $t_{PLH}$ | A | $Q_D$ | | | 32 | 48 | | 46 | 70 | ns |
| $t_{PHL}$ | | | | | 34 | 50 | | 46 | 70 | |
| $t_{PLH}$ | B | $Q_B$ | | | 10 | 16 | | 10 | 16 | ns |
| $t_{PHL}$ | | | | | 14 | 21 | | 14 | 21 | |
| $t_{PLH}$ | B | $Q_C$ | | | 21 | 32 | | 21 | 32 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 23 | 35 | |
| $t_{PLH}$ | B | $Q_D$ | | | 21 | 32 | | 34 | 51 | ns |
| $t_{PHL}$ | | | | | 23 | 35 | | 34 | 51 | |
| $t_{PHL}$ | Set-to-0 | Any | | | 26 | 40 | | 26 | 40 | ns |
| $t_{PLH}$ | Set-to-9 | $Q_A$, $Q_D$ | | | 20 | 30 | | | | ns |
| $t_{PHL}$ | | $Q_B$, $Q_C$ | | | 26 | 40 | | | | |

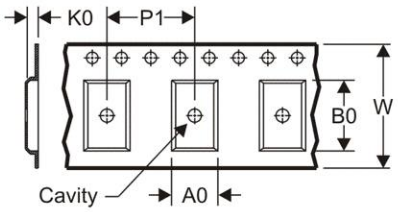
#$f_{max}$ = maximum count frequency
$t_{PLH}$ = propagation delay time, low-to-high-level output
$t_{PHL}$ = propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

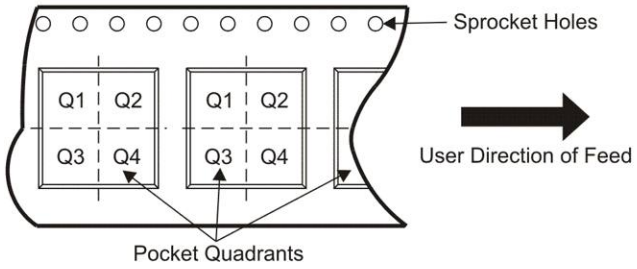



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

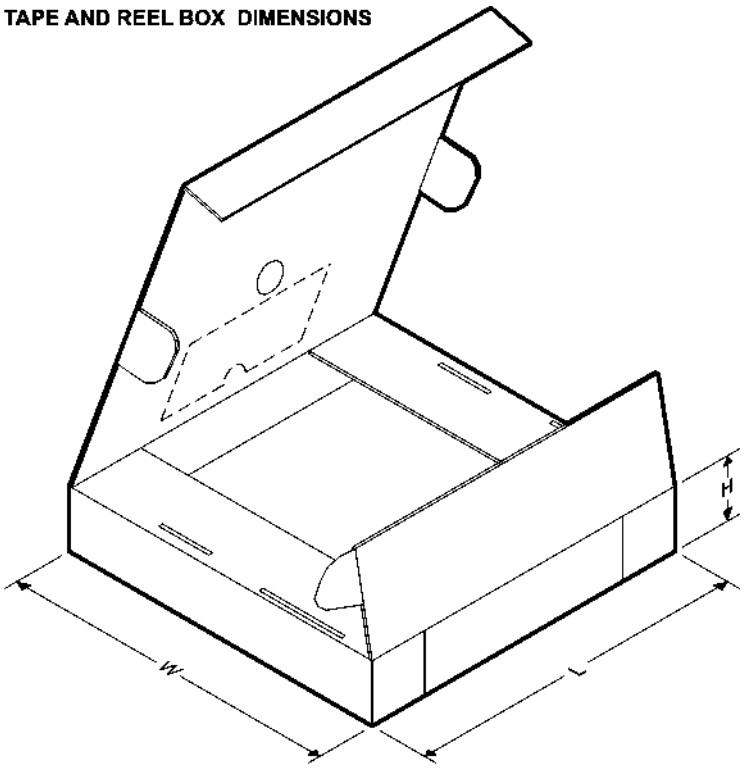
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LS293DR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LS293DR | SOIC | D | 14 | 2500 | 346.0 | 346.0 | 33.0 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN74LS293D | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS293 |
| SN74LS293D.A | Active | Production | SOIC (D) \| 14 | 50 \| TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | LS293 |
| SN74LS293N | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS293N |
| SN74LS293N.A | Active | Production | PDIP (N) \| 14 | 25 \| TUBE | Yes | NIPDAU | N/A for Pkg Type | 0 to 70 | SN74LS293N |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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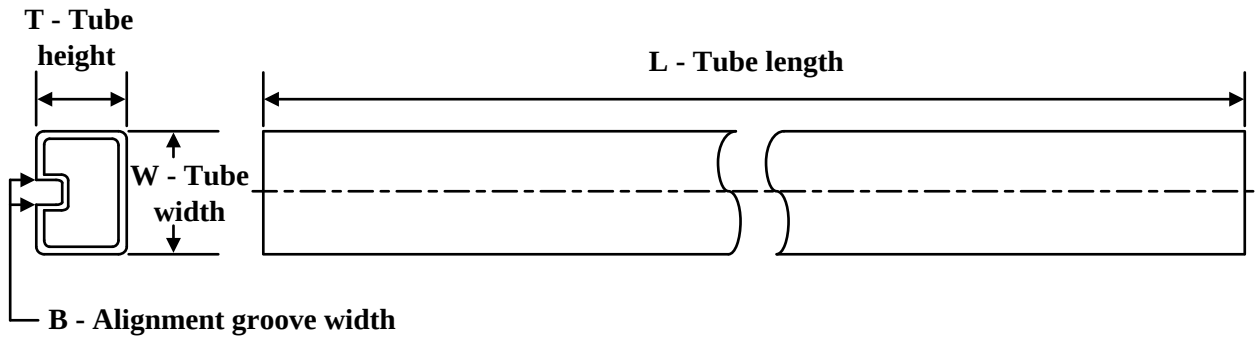
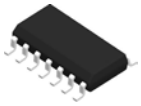
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74LS293D | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS293D.A | D | SOIC | 14 | 50 | 506.6 | 8 | 3940 | 4.32 |
| SN74LS293N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS293N | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS293N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN74LS293N.A | N | PDIP | 14 | 25 | 506 | 13.97 | 11230 | 4.32 |

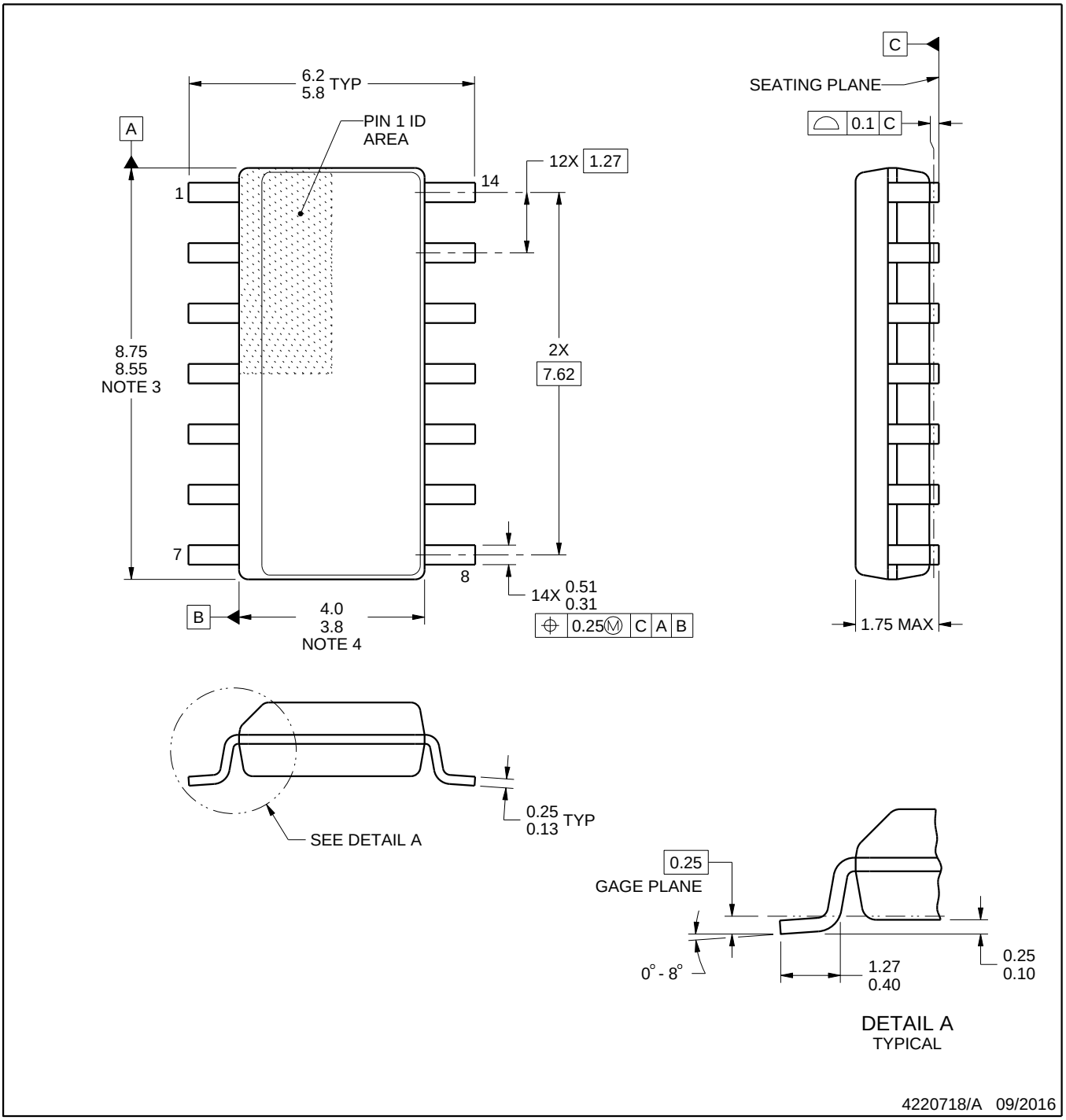


# PACKAGE OUTLINE

## D0014A

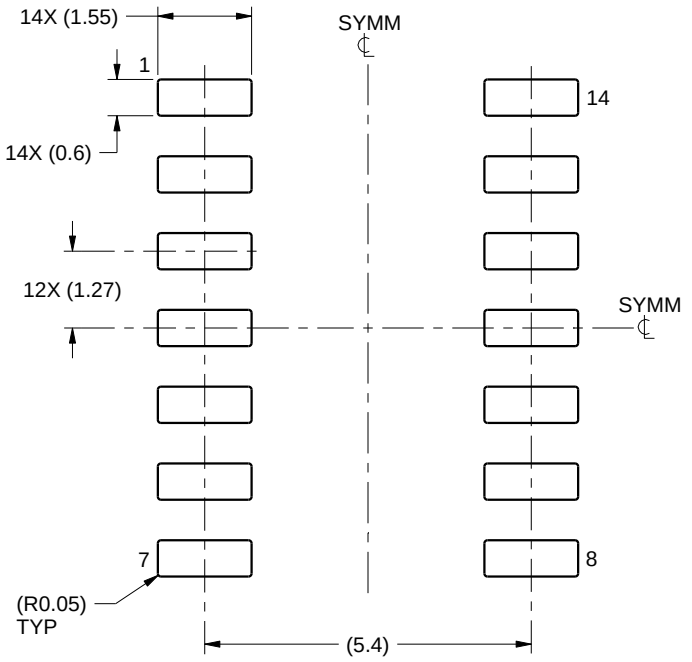
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

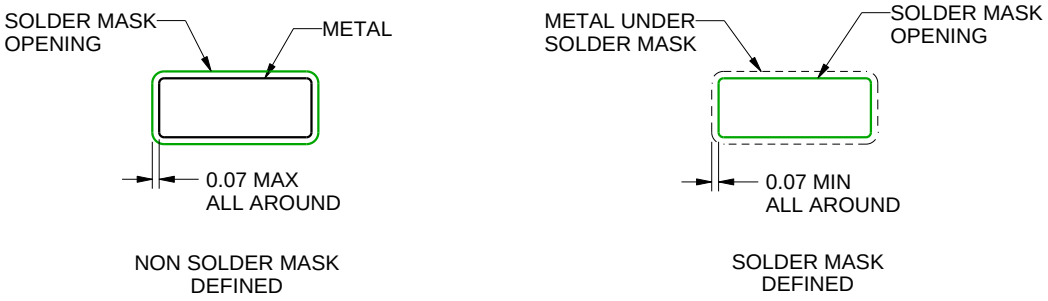



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.




LAND PATTERN EXAMPLE
SCALE:8X




SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

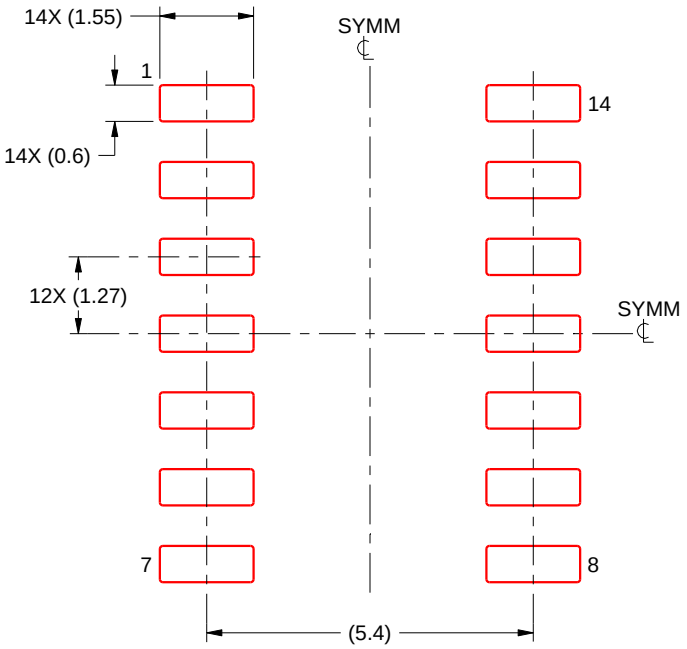
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0014A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

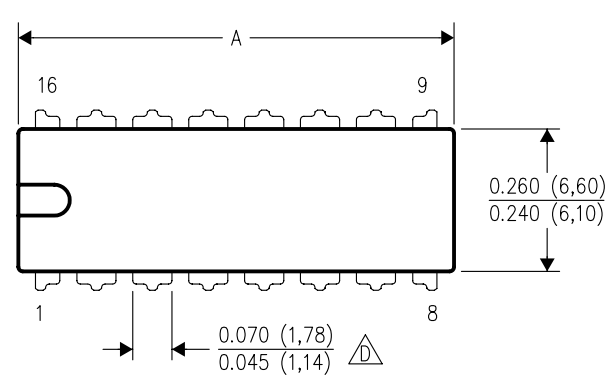
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

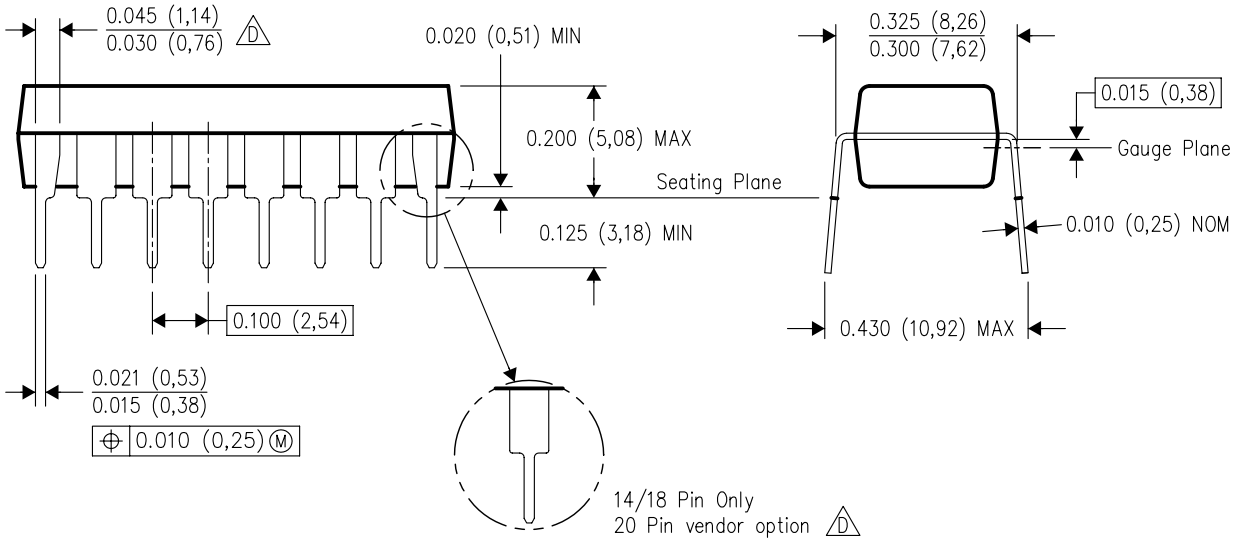
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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