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# FDMC6679AZ

## P-Channel PowerTrench<sup>®</sup> MOSFET

-30 V, -20 A, 10 mΩ

### Features

- Max  $r_{DS(on)}$  = 10 mΩ at  $V_{GS} = -10$  V,  $I_D = -11.5$  A
- Max  $r_{DS(on)}$  = 18 mΩ at  $V_{GS} = -4.5$  V,  $I_D = -8.5$  A
- HBM ESD protection level of 8 kV typical(note 3)
- Extended  $V_{GSS}$  range (-25 V) for battery applications
- High performance trench technology for extremely low  $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant

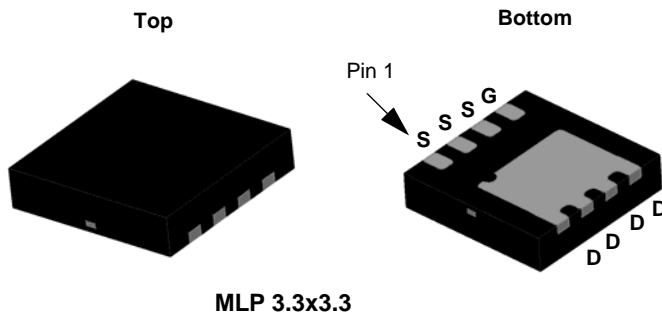


### General Description

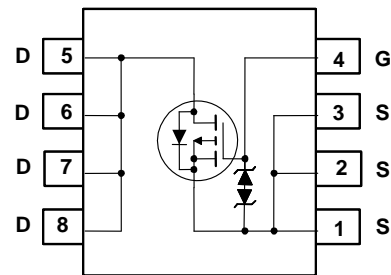
The FDMC6679AZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  and ESD protection.

### Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



MLP 3.3x3.3



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-30	V
$V_{GS}$	Gate to Source Voltage	±25	V
$I_D$	Drain Current -Continuous $T_C = 25$ °C	-20	A
	-Continuous $T_A = 25$ °C (Note 1a)	-11.5	
	-Pulsed	-32	
$P_D$	Power Dissipation $T_C = 25$ °C	41	W
	Power Dissipation $T_A = 25$ °C (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC6679AZ	FDMC6679AZ	MLP 3.3x3.3	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\text{ }\mu\text{A}, V_{GS} = 0\text{ V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		29		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V},$ $V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-7		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{ V}, I_D = -11.5\text{ A}$		8.6	10	m $\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -8.5\text{ A}$		12	18	
		$V_{GS} = -10\text{ V}, I_D = -11.5\text{ A}, T_J = 125\text{ }^\circ\text{C}$		12	15	
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -11.5\text{ A}$		46		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1\text{ MHz}$		2985	3970	pF
$C_{oss}$	Output Capacitance			570	755	pF
$C_{rss}$	Reverse Transfer Capacitance			500	750	pF

### Switching Characteristics

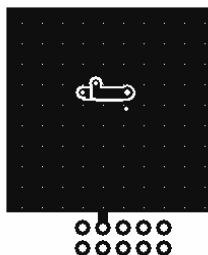
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{ V}, I_D = -11.5\text{ A},$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\text{ }\Omega$		12	21	ns	
$t_r$	Rise Time			14	25	ns	
$t_{d(off)}$	Turn-Off Delay Time			63	100	ns	
$t_f$	Fall Time			46	73	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } -10\text{ V}$		65	91	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } -5\text{ V}$		37	52	nC
$Q_{gs}$	Gate to Source Charge	$V_{DD} = -15\text{ V},$ $I_D = -11.5\text{ A}$		8.7		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			17		nC	

### Drain-Source Diode Characteristics

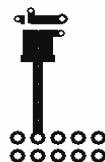
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -11.5\text{ A}$ (Note 2)		0.83	1.30	V
		$V_{GS} = 0\text{ V}, I_S = -1.6\text{ A}$ (Note 2)		0.71	1.20	
$t_{rr}$	Reverse Recovery Time	$I_F = -11.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		31	49	ns
$Q_{rr}$	Reverse Recovery Charge			16	28	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 53  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper

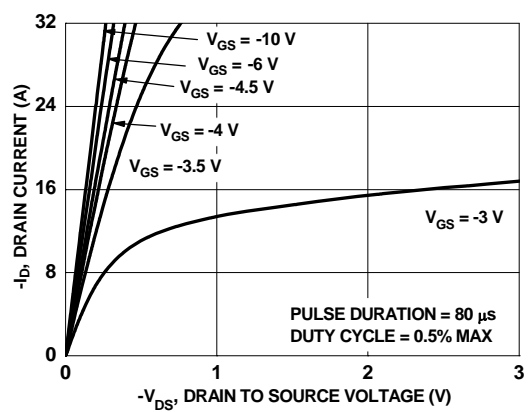


b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

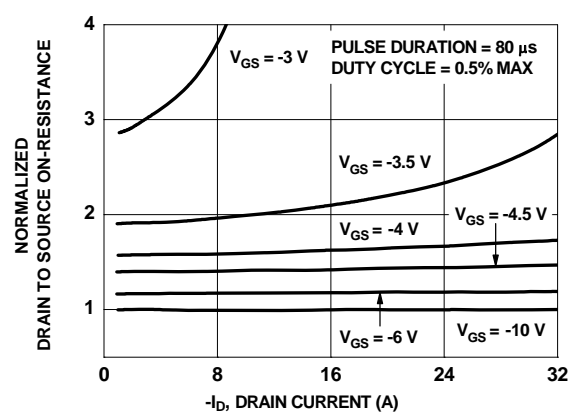
- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

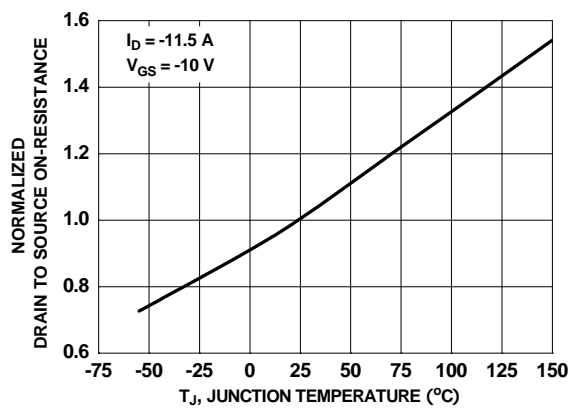
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



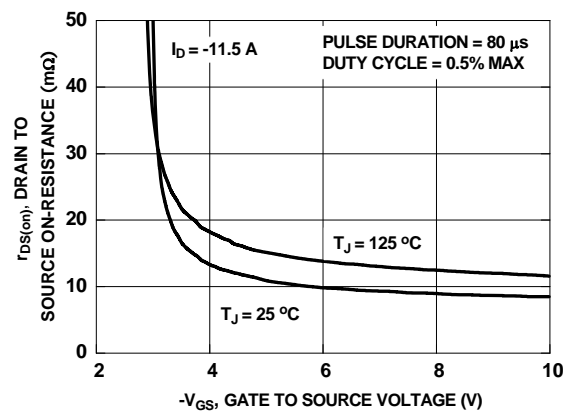
**Figure 1. On Region Characteristics**



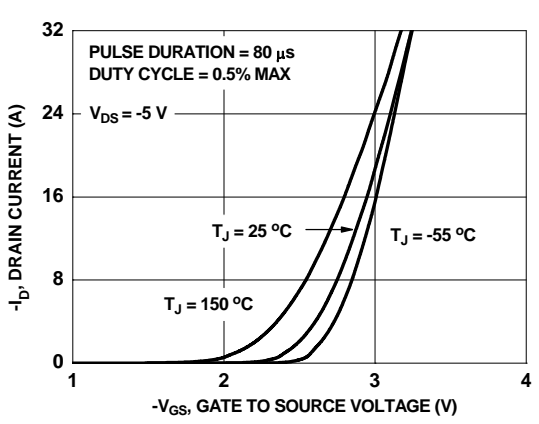
**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**



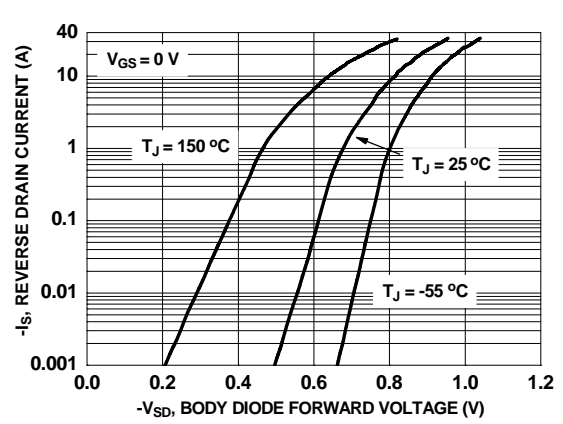
**Figure 3. Normalized On Resistance vs. Junction Temperature**



**Figure 4. On-Resistance vs. Gate to Source Voltage**

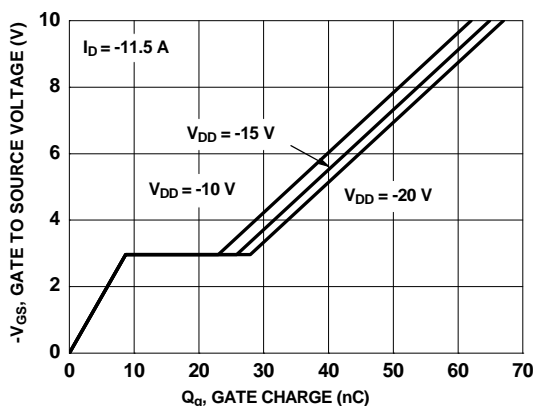


**Figure 5. Transfer Characteristics**

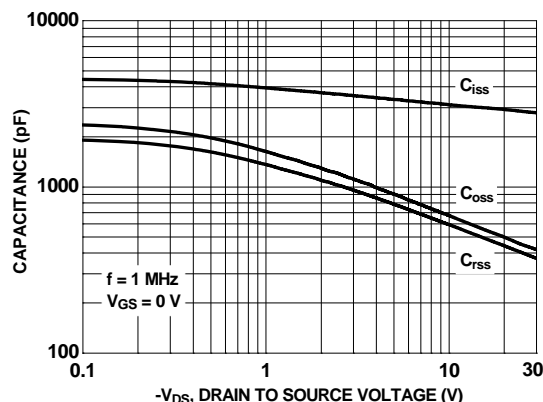


**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

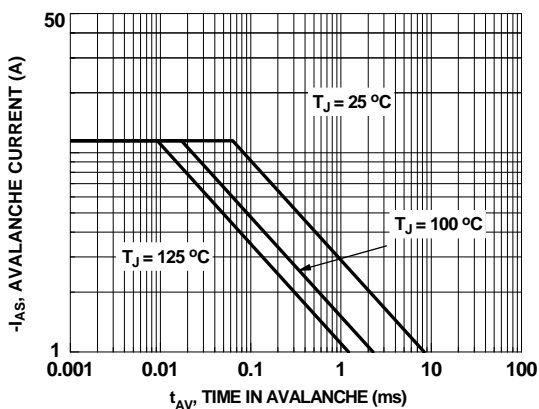
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



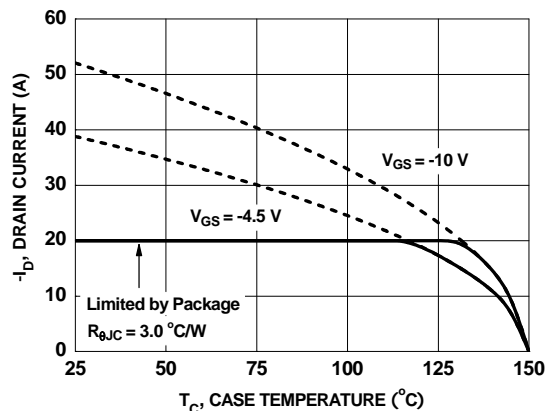
**Figure 7. Gate Charge Characteristics**



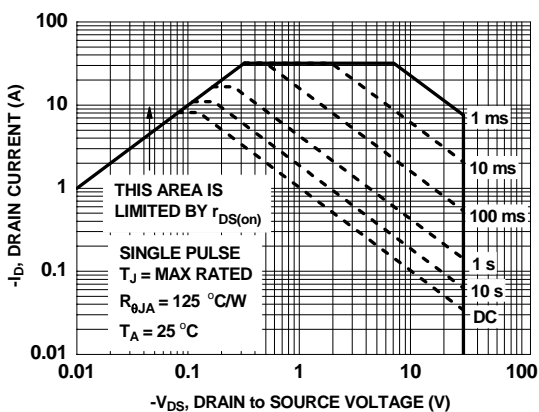
**Figure 8. Capacitance vs. Drain to Source Voltage**



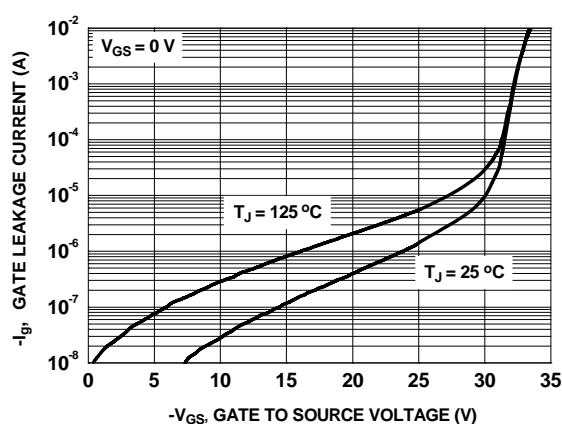
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

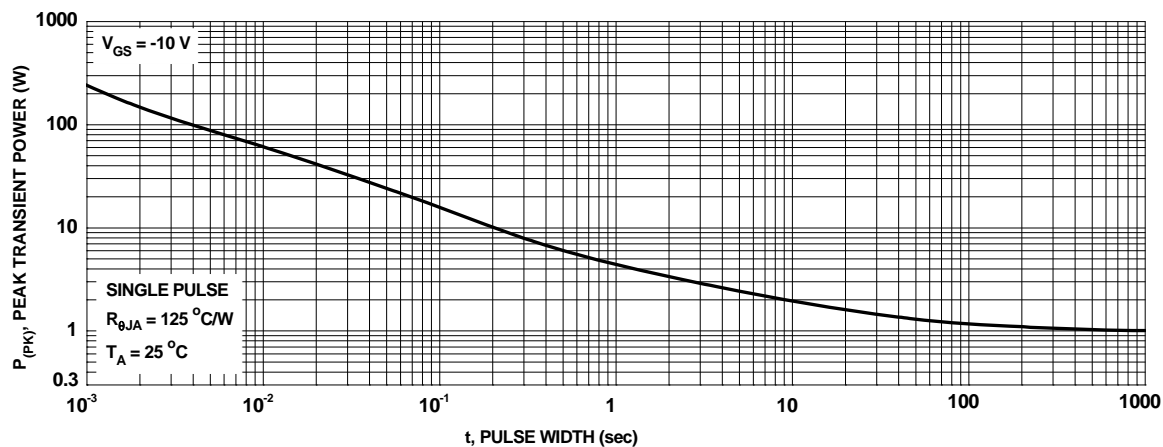


**Figure 11. Forward Bias Safe Operating Area**

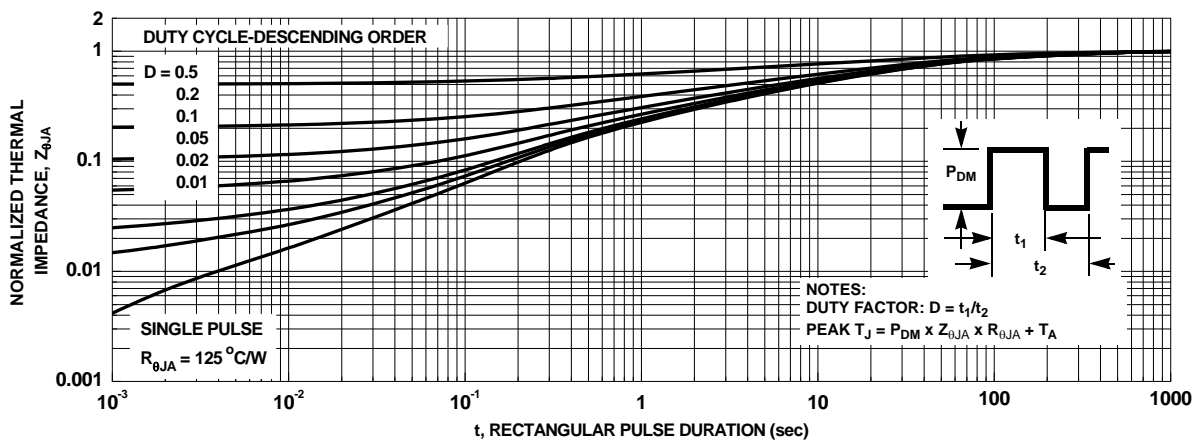


**Figure 12. Igs vs. Vgs**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

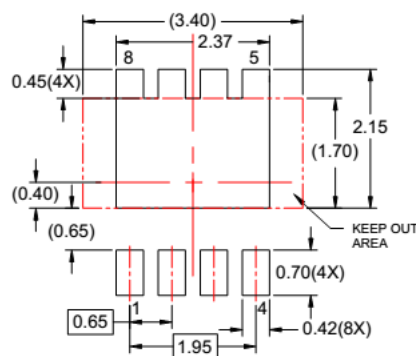
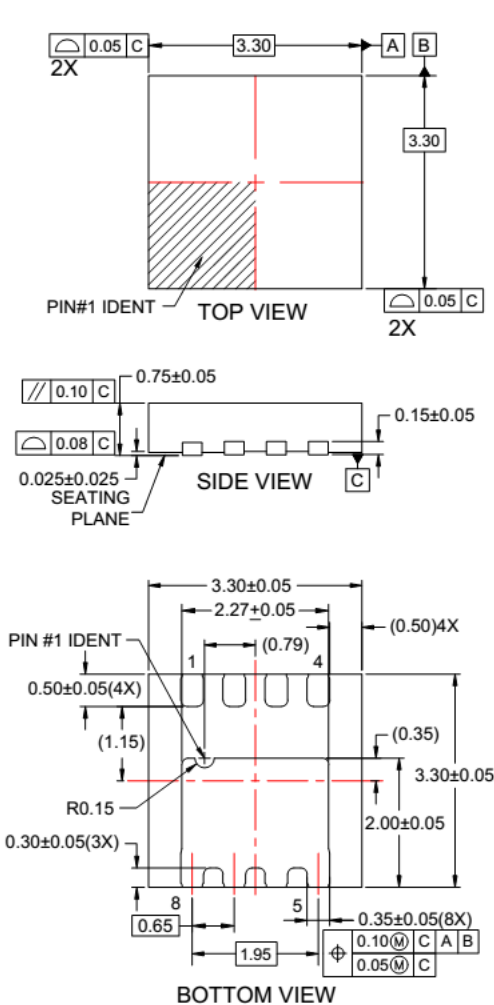


**Figure 13. Single Pulse Maximum Power Dissipation**



**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout



RECOMMENDED LAND PATTERN

### NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.




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