8-Bit Single-Chip Microcontroller

SAB 8051A Microcontroller with factory mask-programmable ROM

SAB 8031A Microcontroller for external ROM

- Version for 12MHz/16MHz/ 20 MHz operating frequency
- 4K × 8 ROM
- 128 × 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- High-performance full-duplex serial channel with flexible transmit/receive bound rate capability
- External memory expandable up to 128 Kbyte
- Compatible with SAB 8080/8085 peripherals
- Boolean processor
- 218 user bit-addressable locations
- Most instructions execute in:
  1 µs instruction cycle time at 12 MHz
  750 ns instruction cycle time at 16 MHz
  600 ns instruction cycle time at 20 MHz
- 4 µs (3 µs, 2.4 µs) multiply and divide
- Packages P-DIP-40 and PL-CC-44
- Two temperature ranges available
  0 to 70 °C
  –40 to 85 °C: T40/85

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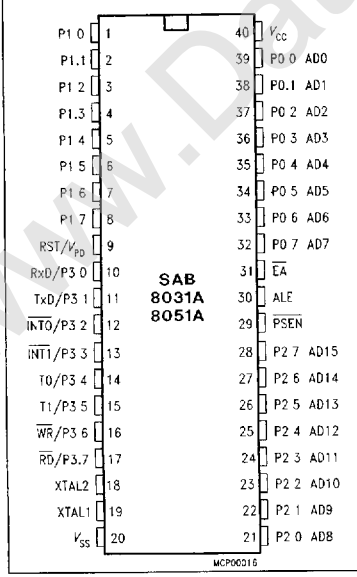
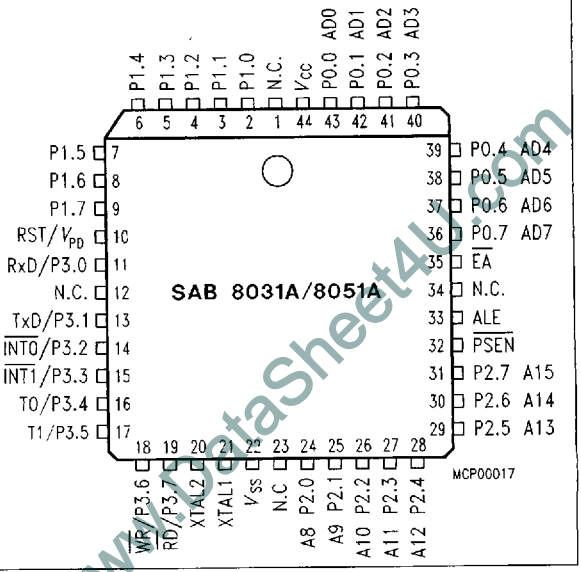
Figure 1
Pin Configuration
P-DIP-40



PL-CC-44



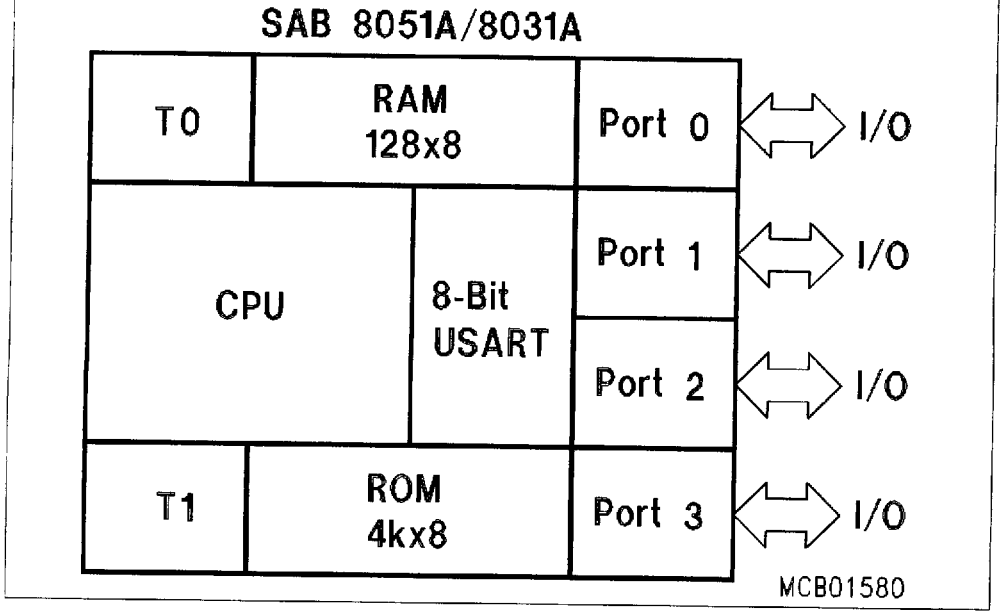
The SAB 8051A/8031A Family are standalone, high-performance single-chip microcontrollers fabricated in + 5 V advanced N-channel, silicon-gate Siemens MYMOS technology and supplied in a 40-pin plastic P-DIP or 44-pin plastic leaded chip carrier (PL-CC-44) package. It provides the hardware features, architectural enhancements and instructions that are necessary to make it a powerful and cost-effective controller for applications requiring up to 64 Kbytes of program memory and/or up to 64 Kbytes of data storage.

The SAB 8051A contains a non-volatile 4K × 8 read-only program memory; a volatile 128 × 8 read/write data memory; 32 I/O lines; two 16-bit timer/counters; a five-source, two-priority-level, nested interrupt structure; a serial I/O port for either multi-processor communications, I/O expansion, or full-duplex UART; and on-chip oscillator and clock circuits. The SAB 8031A is identical with the SAB 8051A, except that it lacks the program memory.

For systems that require extra capability, the SAB 8051A can be expanded using standard TTL-compatible memories and the byte-oriented SAB 8080 and SAB 8085 peripherals.

The parts are available for standard temperature range (0 to 70 °C) and extended temperature range (T40/85: – 40 to 85 °C).

Figure 2
SAB 8051A/8031A Family



Ordering Information

Type	Package	Description (8-bit single-chip microcontroller)
SAB 8031A-P-40/85	P-DIP-40	for external memory, 12 MHz, ext. Temp.
SAB 8031A-N-40/85	PL-CC-44	
SAB 8031A-P	P-DIP-40	for external memory, 12 MHz
SAB 8031A-N	PL-CC-44	
SAB 8031A-16-P	P-DIP-40	for external memory, 16 MHz
SAB 8031A-16-N	PL-CC-44	
SAB 8031A-20-P	P-DIP-40	for external memory, 20 MHz
SAB 8031A-20-N	PL-CC-44	
SAB 8051A-P-40/85	P-DIP-40	with 4-KByte mask-programmable ROM 12 MHz, ext. Temp.
SAB 8051A-P	P-DIP-40	with 4-KByte mask-programmable ROM 12 MHz
SAB 8051A-N	PL-CC-44	
SAB 8051A-16-P	P-DIP-40	with 4-KByte mask-programmable ROM 16 MHz
SAB 8051A-16-N	PL-CC-44	
SAB 8051A-20-P	P-DIP-40	with 4-KByte mask-programmable ROM 20 MHz
SAB 8051A-20-N	PL-CC-44	

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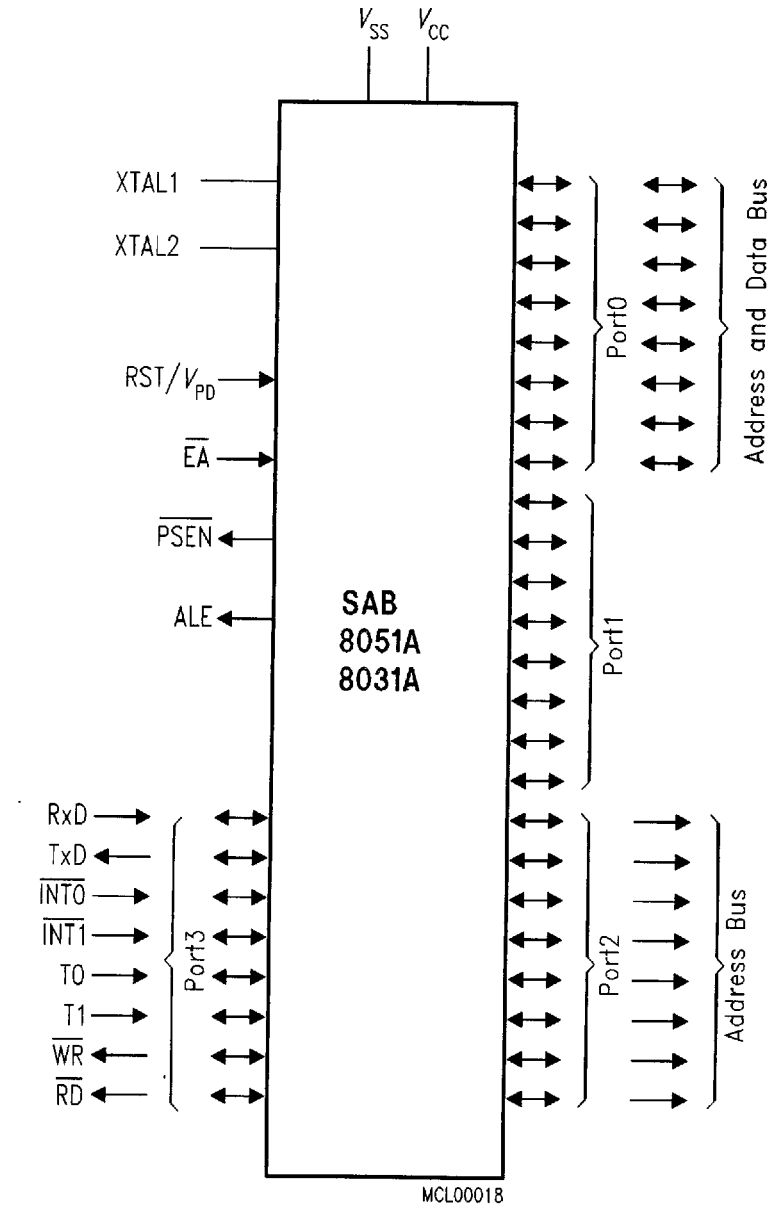
Figure 3
Logic Symbol



Pin Definitions and Functions

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
P1.0-P1.7	1-8	2-9	I/O	**PORT 1** is an 8-bit quasi-bidirectional I/O port. It is used for the low-order address byte during program verification. Port 1 can sink/source four LS TTL loads.
RST/V_{PD}	9	10	I	**RESET** A high level on this pin resets the SAB 8051A. A small internal pulldown resistor permits power-on reset using only a capacitor connected to V_{CC}. If V_{PD} is held within its spec while V_{CC} drops below spec, V_{PD} will provide standby power to the RAM. When V_{PD} is low, the RAM's current is drawn from V_{CC}.
P3.0-P3.7	10-17	11, 13-19	I/O	**PORT 3** is an 8-bit quasi-bidirectional I/O port. It also contains the interrupt, timer, serial port and $\overline{RD}$ and $\overline{WR}$ pins that are used by various options. The output latch corresponding to a secondary function must be programmed to a one (1) for that function to operate. Port 3 can sink/source four LS TTL loads. The secondary functions are assigned to the pins of port 3, as follows: –R_XD/data (P3.0). Serial port's receiver data input (asynchronous) or data input/output (synchronous). –T_XD/clock (P3.1). Serial port's transmitter data output (asynchronous) or clock output (synchronous). –$\overline{INT0}$ (P3.2). Interrupt 0 input or gate control input for counter 0. –$\overline{INT1}$ (P3.3). Interrupt 1 input or gate control input for counter 1. –T0 (P3.4). Input to counter 0. – T1 (P3.5). Input to counter 1. –$\overline{WR}$ (P3.6). The write control signal latches the data byte from port 0 into the external data memory. –$\overline{RD}$ (P3.7). The read control signal enables external data memory to port 0.
XTAL 1 XTAL 2	19 18	21 20		**XTAL 1** input to the oscillator's high gain amplifier. Required when a crystal is used. Connect to V_{SS} when external source is used on XTAL 2. **XTAL 2** output from the oscillator's amplifier. Input to the internal timing circuitry. A crystal or external source can be used.
P2.0-P2.7	21-28	24-31	I/O	**PORT 2** is an 8-bit quasi-bidirectional I/O port. It also emits the high-order address byte when accessing external memory. It is used for the high-order address and the control signals during program verification. Port 2 can sink/source four LS TTL loads.
$\overline{PSEN}$	29	32	O	The **Program Store Enable** output is a control signal that enables the external program memory to the bus during external fetch operations. It is activated every six oscillator periods, except during external data memory accesses. Remains high during internal program execution.

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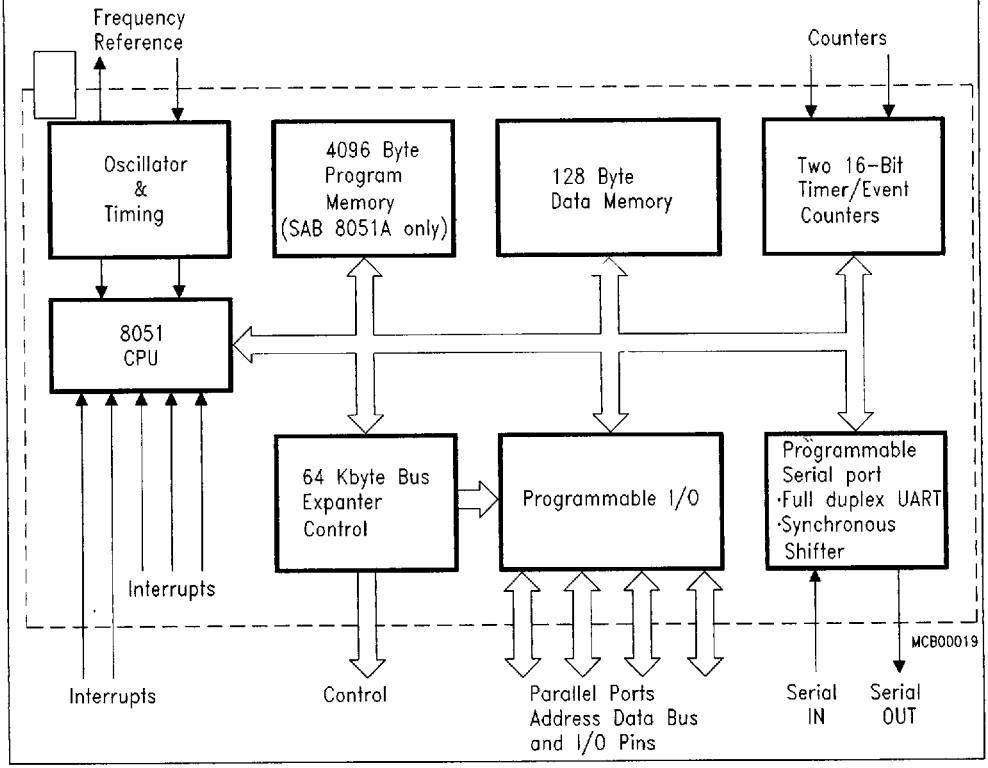
Pin Definitions and Functions (cont'd)

Symbol	Pin		Input (I) Output (O)	Function
	P-DIP-40	PL-CC-44		
ALE	30	33	O	Provides **Address Latch Enable** output used for latching the address into external memory during normal operation. It is activated every six oscillator periods except during an external data memory access.
$\overline{EA}$	31	35	I	**External Latch Enable** when held at a TTL high level, the SAB 8051A executes instructions from the internal ROM when the PC is less than 4096. When held at a TTL low level, the SAB 8051A fetches all instructions from external program memory. For the SAB 8031A this pin must be tied low.
P0.0-P0.7	39-32	43-36	I/O	**Port 0** is an 8-bit open drain bidirectional I/O port. It is also the multiplexed low-order address and data bus when using external memory. It is used for data output during program verification. Port 0 can sink/source eight LS TTL loads.
V_{CC}	40	44		+ 5 V **Power Supply** during operation and program verification.
V_{SS}	20	22		**Ground** (0 V)
NC	–	1, 12 23, 34	–	**No Connection**

Figure 4
Block Diagram



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Absolute Maximum Ratings

Ambient temperature under bias .....
SAB 8051A/8031A.....0 to 70 °C
SAB 8051A/8031A-T40/85 .....– 40 to 85 °C
Storage temperature..... – 65 to 150 °C
Voltage on V_{CC} pins with
respect to ground (V_{SS})..... – 0.5 to 7 V
Power dissipation ..... 2 W

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

V_{CC} = 5 V ± 10 %; V_{SS} = 0 V
T_A = 0 to 70 °C for the SAB 8051A/8031A
T_A = – 40 to 85 °C for the SAB 8051A/8031A-T40/85

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
V_{IL}	Input low voltage	– 0.5	0.8	V	–
V_{IH}	Input high voltage (except RST/VPD and XTAL 2)	2.0	V_{CC} + 0.5	V	–
V_{IH1}	Input high voltage to RST/VPD for reset, XTAL 2	2.5	V_{CC} + 0.5	V	XTAL1 to V_{SS}
V_{PD}	Power down voltage to RST/VPD	4.5	5.5	V	V_{CC} = 0 V
V_{OL}	Output low voltage Ports 1, 2, 3	– .	0.45	V	I_{OL} = 1.6 mA
V_{OL1}	Output low voltage Port 0, ALE, $\overline{PSEN}$	–	0.45	V	I_{OL} = 3.2 mA
V_{OH}	Output high voltage Ports 1, 2, 3	2.4	–	V	I_{OH} = – 80 µA
V_{OH1}	Output high voltage Port 0, ALE, $\overline{PSEN}$	2.4	–	V	I_{OH} = – 400 µA

DC Characteristics (cont'd)

Symbol	Parameter	Limit Values		Unit	Test Condition
		min.	max.		
I_{IL}	Logical 0 input current Ports 1, 2, 3	–	– 500	µA	V_{IL} = 0.45 V
I_{IL2}	Logical 0 input current XTAL 2 SAB 8051A/8031A-12/16/20 SAB 8051A/8031A-T40/85	 – –	 – 3.2 – 2.5	 mA mA	 XTAL1 = V_{SS} V_{IL} = 0.45 V
I_{IH1}	Input high current to RST/V_{PD} for reset	–	500	µA	V_{IN} = V_{CC} - 1.5 V
I_{LI}	Input leakage current to port 0, $\overline{EA}$	–	± 10	µA	0 V < V_{IN} < V_{CC}
I_{CC}	Power supply current SAB 8051A/8031A SAB 8051A/8031A-16 SAB 8051A/8031A-20	 – – –	 125 140 140	 mA mA mA	All outputs disconnected
I_{PD}	Power down current SAB 8051A/8031A-12/16/20 SAB 8051A/8031A-T40/85	 – –	 10 15	 mA mA	 V_{CC} = 0 V V_{PD} = 4.5 ... 5.5 V
C_{IO}	Capacitance of I/O buffer	–	10	pF	f_c = 1 MHz

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AC Characteristics for SAB 8051A/8031A

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to 70 °C for the SAB 8051A/8031A
T_A = – 40 to 85 °C for the SAB 8051A-T3/8031A-T40/85

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 12 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 12 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	127	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	53	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	48	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	233	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	58	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	215	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	150	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	63	–	$t_{CLCL}-20$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	75	–	$t_{CLCL}-8$	–	ns
t_{AVIV}	Address to valid instruction in	–	302	–	$5t_{CLCL}-115$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB8051A to devices with float times up to 75 ns is permissible. The limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

t_{RLRH}	RD pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	400	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	132	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	252	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	97	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	517	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	585	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	200	300	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	203	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	43	123	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	33	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	433	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	33	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	83.3	833.3	ns
t_{CHCX}	High time	–	–	20	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	20	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	20	ns
t_{CHCL}	Fall time	–	–	–	20	ns

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AC Characteristics for SAB 8051A/8031A-16

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and PSEN outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to + 70 °C for SAB 8051 A/8031A-16

Program Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	85	–	$2t_{CLCL}-40$	–	ns
t_{AVLL}	Address setup to ALE	33	–	$t_{CLCL}-30$	–	ns
t_{LLAX1}	Address hold after ALE	28	–	$t_{CLCL}-35$	–	ns
t_{LLIV}	ALE to valid instruction in	–	150	–	$4t_{CLCL}-100$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	38	–	$t_{CLCL}-25$	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	153	–	$3t_{CLCL}-35$	–	ns
t_{PLIV}	PSEN to valid instruction in	–	88	–	$3t_{CLCL}-100$	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXIZ}*)	Input instruction float after PSEN	–	48	–	$t_{CLCL}-15$	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	60	–	$t_{CLCL}-3$	–	ns
t_{AVIV}	Address to valid instruction in	–	223	–	$5t_{CLCL}-90$	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A-16 to devices with float times up to 55 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

AC Characteristics for SAB 8051A/8031A-16 (cont'd)

External Data Memory Characteristics

Symbol	Parameter	Limit Values				Unit
		Clock 16 MHz clock		Variable clock $1/t_{CLCL}$ = 1.2 MHz to 16 MHz		
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	275	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	90	–	$2t_{CLCL}-35$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	148	–	$5t_{CLCL}-165$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	55	–	$2t_{CLCL}-70$	ns
t_{LLDV}	ALE to valid data in	–	350	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	398	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	138	238	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	120	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	23	103	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	13	–	$t_{CLCL}-50$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	288	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	13	–	$t_{CLCL}-50$	–	ns
t_{RLAZ}	Address float after $\overline{RD}$	–	0	–	0	ns

External Clock Drive XTAL2

t_{CLCL}	Oscillator period	–	–	62.5	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

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AC Characteristics for SAB 8051A/8031A-20

V_{CC} = 5 V ± 10%; V_{SS} = 0 V
(C_L for port 0, ALE and $\overline{PSEN}$ outputs = 100 pF; C_L for all other outputs = 80 pF)
T_A = 0 to + 70 °C for SAB 8051A/8031A-20

Program Memory Characteristics

Symbol	Parameter	Clock 20 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 20 MHz		Unit
		min.	max.	min.	max.	
t_{LHLL}	ALE pulse width	60	–	$2t_{CLCL}$–40	–	ns
t_{AVLL}	Address setup to ALE	20	–	t_{CLCL}–30	–	ns
t_{LLAX1}	Address hold after ALE	20	–	t_{CLCL}–35	–	ns
t_{LLIV}	ALE to valid instruction in	–	100	–	$4t_{CLCL}$–100	ns
t_{LLPL}	ALE to $\overline{PSEN}$	25	–	t_{CLCL}–25	–	ns
t_{PLPH}	$\overline{PSEN}$ pulse width	115	–	$3t_{CLCL}$–35	–	ns
t_{PLIV}	$\overline{PSEN}$ to valid instruction in	–	75	–	$3t_{CLCL}$–75	ns
t_{PXIX}	Input instruction hold after $\overline{PSEN}$	0	–	0	–	ns
t_{PXAV}*)	Address valid after $\overline{PSEN}$	47	–	t_{CLCL}–3	–	ns
t_{PXIZ}*)	Input instruction float after $\overline{PSEN}$	–	40	–	t_{CLCL}–10	ns
t_{AVIV}	Address to valid instruction in	–	175	–	$5t_{CLCL}$–75	ns
t_{AZPL}	Address float to $\overline{PSEN}$	0	–	0	–	ns

*) Interfacing the SAB 8051A-20 to devices with float times up to 45 ns is permissible. This limited bus contention will not cause any damage to port 0 drivers.

External Data Memory Characteristics

Symbol	Parameter	Clock 20 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 20 MHz		Unit
		min.	max.	min.	max.	
t_{RLRH}	$\overline{RD}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{WLWH}	$\overline{WR}$ pulse width	200	–	$6t_{CLCL}-100$	–	ns
t_{LLAX2}	Address hold after ALE	70	–	$2t_{CLCL}-30$	–	ns
t_{RLDV}	$\overline{RD}$ to valid data in	–	100	–	$5t_{CLCL}-150$	ns
t_{RHDX}	Data hold after $\overline{RD}$	0	–	0	–	ns
t_{RHDZ}	Data float after $\overline{RD}$	–	40	–	$2t_{CLCL}-60$	ns
t_{LLDV}	ALE to valid data in	–	250	–	$8t_{CLCL}-150$	ns
t_{AVDV}	Address to valid data in	–	285	–	$9t_{CLCL}-165$	ns
t_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$	100	200	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
t_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$	70	–	$4t_{CLCL}-130$	–	ns
t_{WHLH}	$\overline{WR}$ or $\overline{RD}$ high to ALE high	20	80	$t_{CLCL}-30$	$t_{CLCL}+30$	ns
t_{QVWX}	Data valid to $\overline{WR}$ transition	5	–	$t_{CLCL}-45$	–	ns
t_{QVWH}	Data setup before $\overline{WR}$	200	–	$7t_{CLCL}-150$	–	ns
t_{WHQX}	Data hold after $\overline{WR}$	10	–	$t_{CLCL}-40$	–	ns
t_{RLAZ}	Address float after RD	–	0	–	0	ns

External Clock Drive

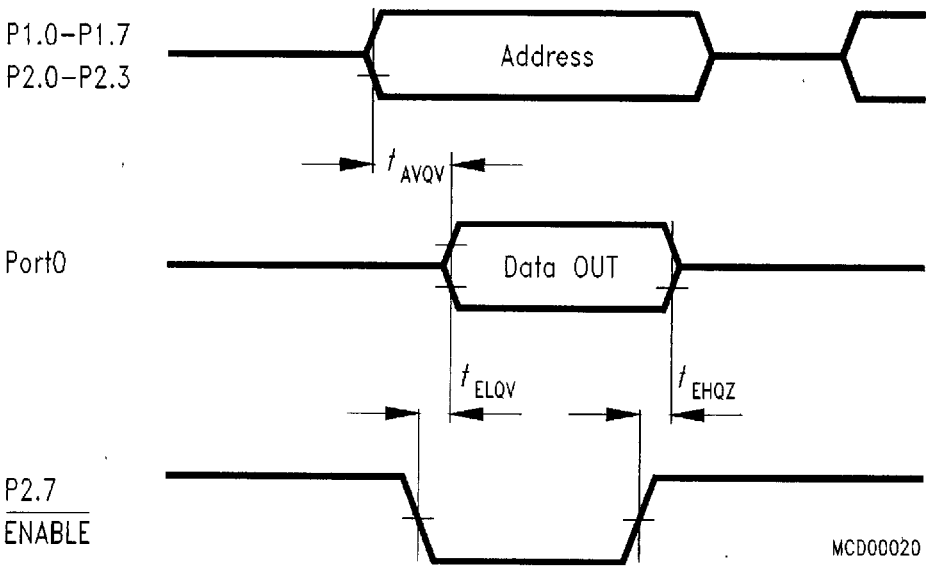
Symbol	Parameter	Clock 20 MHz clock		Variable clock 1/t_{CLCL} = 1.2 MHz to 20 MHz		Unit
		min.	max.	min.	max.	
t_{CLCL}	Oscillator period	–	–	50	833.3	ns
t_{CHCX}	High time	–	–	15	$t_{CLCL}-t_{CLCX}$	ns
t_{CLCX}	Low time	–	–	15	$t_{CLCL}-t_{CHCX}$	ns
t_{CLCH}	Rise time	–	–	–	15	ns
t_{CHCL}	Fall time	–	–	–	15	ns

ROM Verification Characteristics for SAB 8051A/8031A Family

T_A = 25 °C ± 5 °C; V_{CC} = 5 V ± 10%; V_{SS} = 0 V

Symbol	Parameter	Limit Values		Unit
		min.	max.	
t_{AVQV}	Address to valid data	–	48 t_{CLCL}	ns
t_{ELQV}	$\overline{\text{ENABLE}}$ to valid data	–	48 t_{CLCL}	ns
t_{EHQZ}	Data float after $\overline{\text{ENABLE}}$	0	48 t_{CLCL}	ns
$1/t_{CLCL}$	Oscillator frequency	4	6	MHz

Figure 5
ROM Verification



Microcontroller	Address	Data	Inputs
SAB 8051A 4K x 8	P1.0 – P1.7 = A0 – A7 P2.0 – P2.3 = A8 – A11	Port 0= D0 – D7	P2.4 – P2.6, PSEN= V_{SS} ALE, EA = V_{IH} R_{ST}/V_{PD} = V_{IH1}

Waveforms

Figure 6
Program Memory Read Cycle

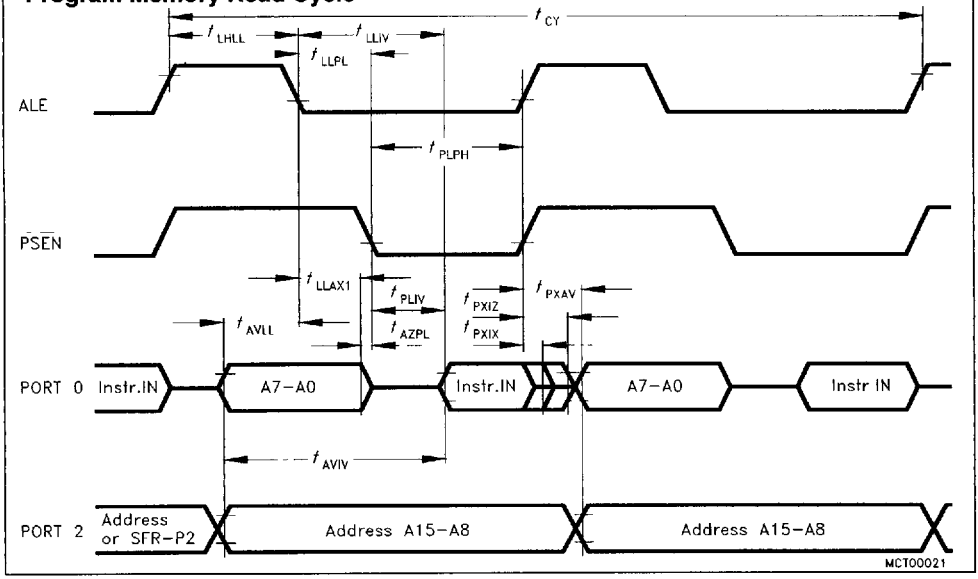


Figure 7
Data Memory Read Cycle

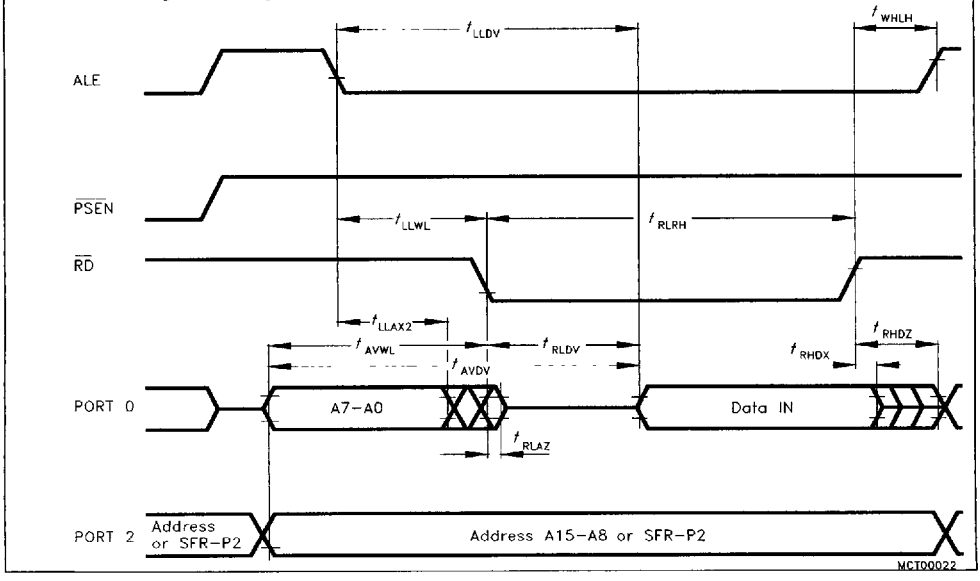


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Figure 8
Data Memory Write Cycle

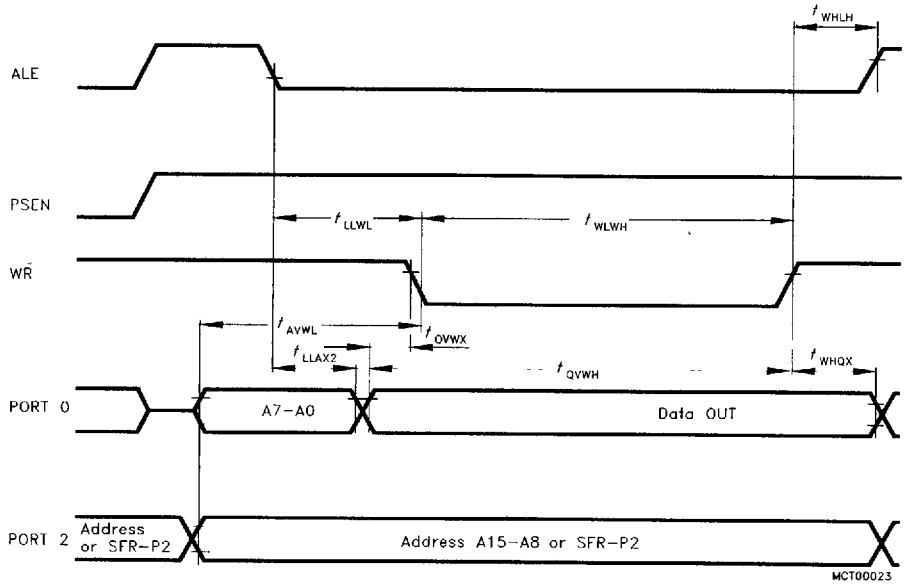
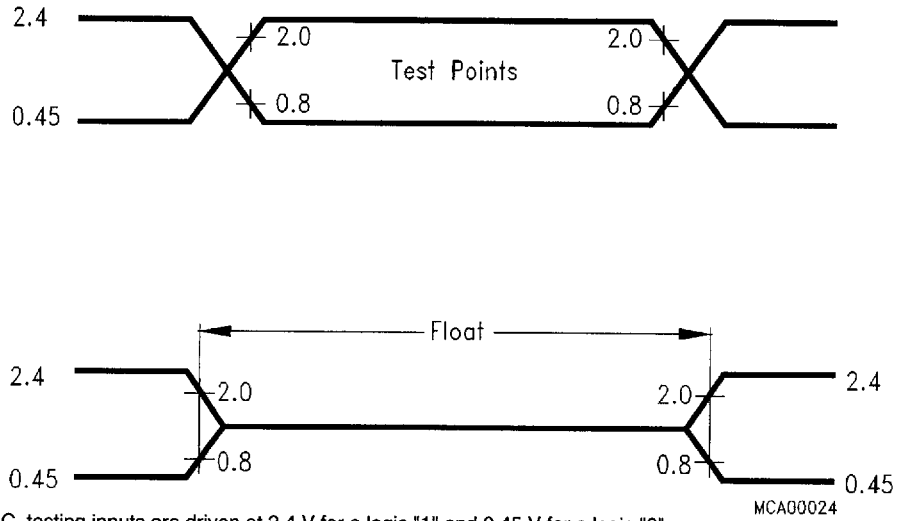
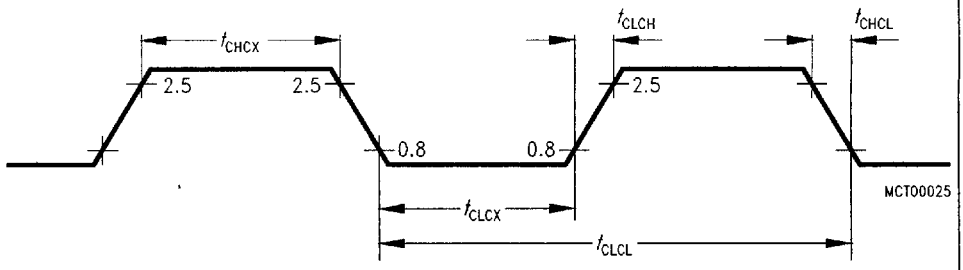


Figure 9
AC Testing Input, Output, Float Waveforms



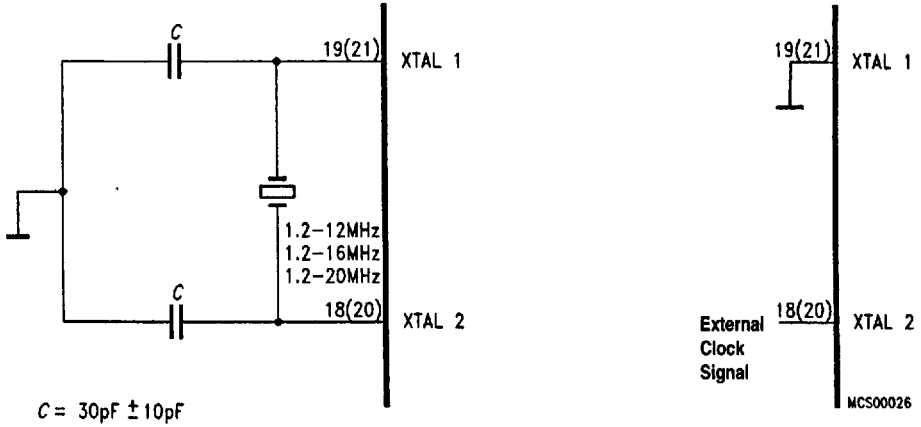
A.C. testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".
For timing purposes, the float state is defined as the point at which a P0 pin sinks 3.2 mA or sources 400 µA at the voltage test levels.

Figure 10
External Clock Cycle



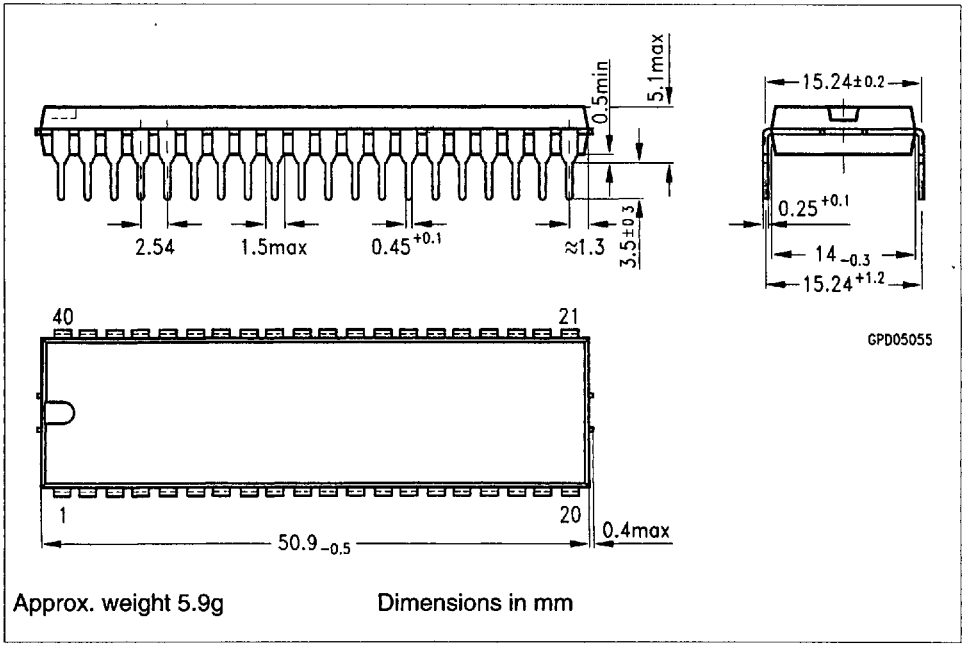
4

Figure 11
Recommended Oscillator Circuits



Pin number in (. . .) are for PL-CC-44 package

Package Outlines



Approx. weight 5.9g Dimensions in mm

Plastic Package, P-DIP-40

(Dual-In-Line Package)
20 B 40 DIN 41870 T10

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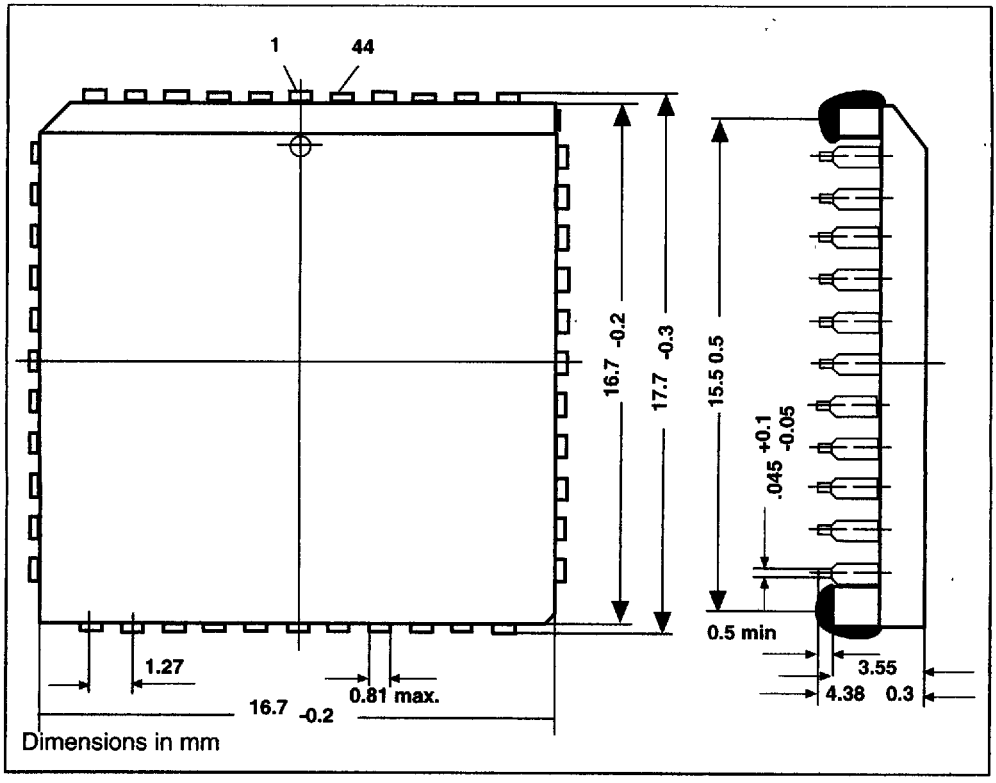
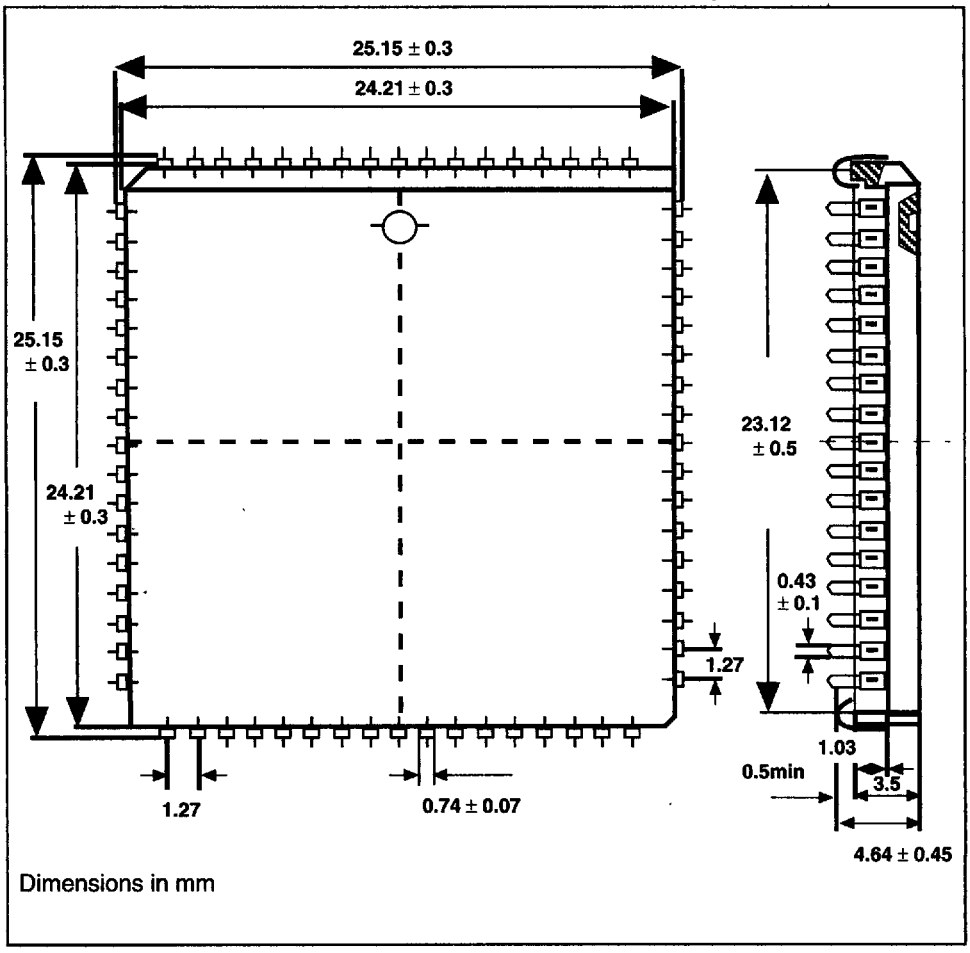
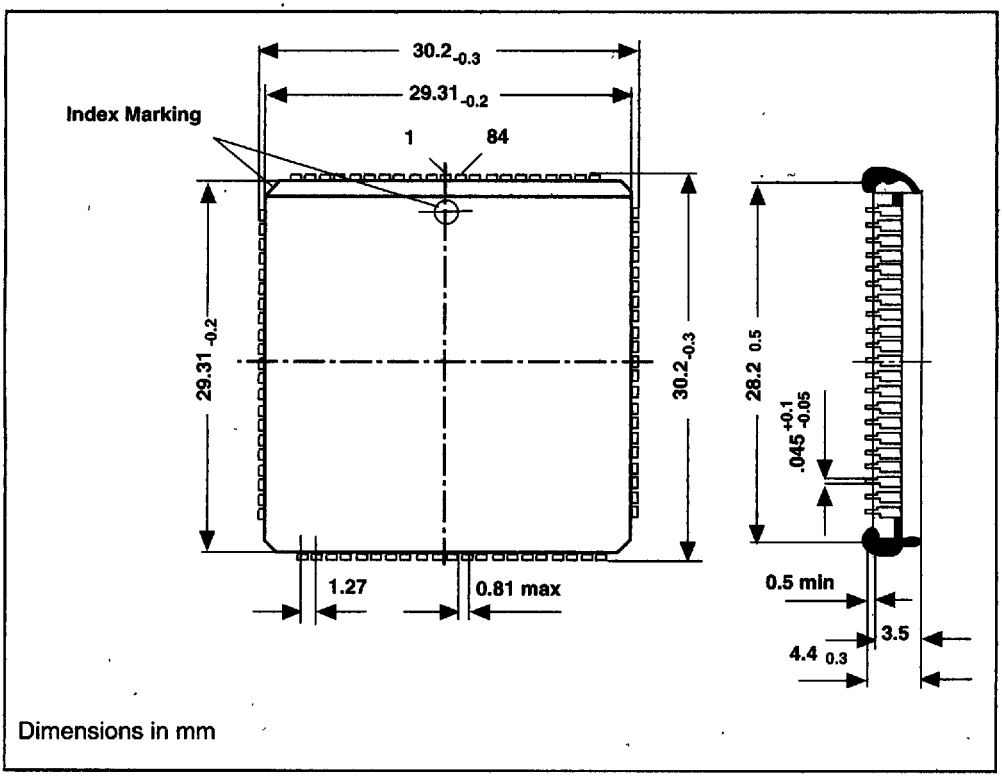


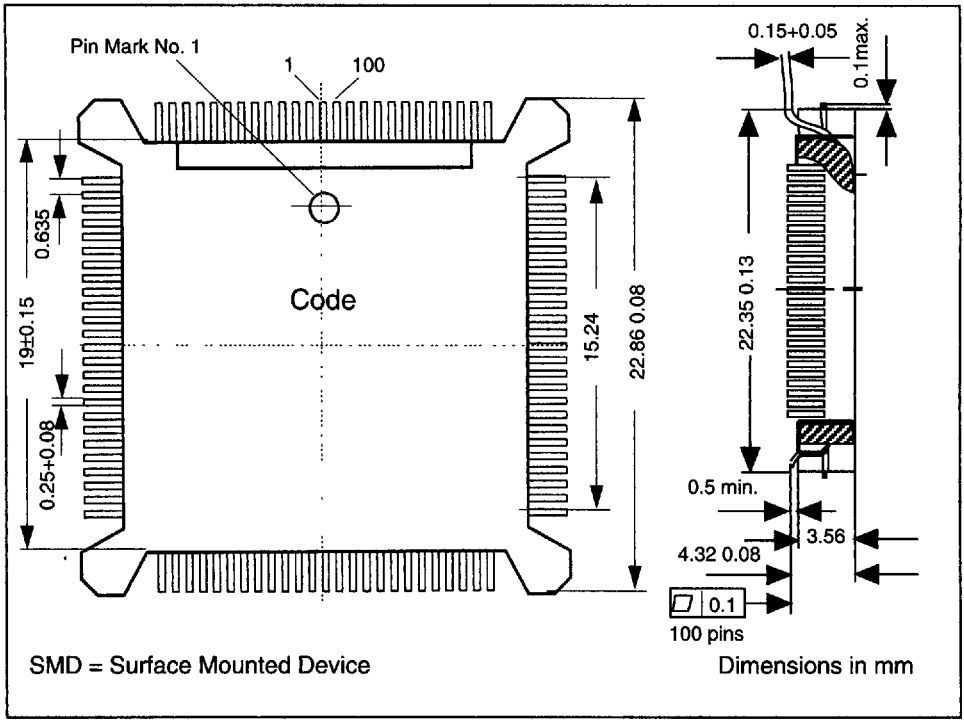
Plastic Package, P-LCC-44
(Plastic Leaded—Chip Carrier) **-SMD**



Plastic Package, PLCC-68 (SMD)
(plastic leaded chip carrier)



Plastic Package, PLCC-84 (SMD)
(plastic leaded chip carrier)



Plastic Package, P-QFP-100
(Plastic Quad-Flat-Pack) - **SMD**

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