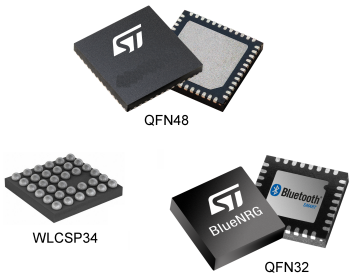
BlueNRG-LP

Datasheet

Programmable Bluetooth® Low Energy wireless SoC



Product status link
BlueNRG-LP

Product summary	
Order code	BlueNRG-3x5yz

Features

- Bluetooth Low Energy system-on-chip supporting Bluetooth 5.2 specifications
  - 2 Mbps data rate
  - Long range (Coded PHY)
  - Advertising extensions
  - Channel selection algorithm #2
  - GATT caching
- Radio
  - RX sensitivity level: -97 dBm @ 1 Mbps, -104 dBm @ 125 kbps (long range)
  - Programmable output power up to +8 dBm (at antenna connector)
  - Data rate supported: 2 Mbps, 1 Mbps, 500 kbps and 125 kbps
  - 128 physical connections
  - Integrated balun
  - Support for external PA
  - BlueNRG core coprocessor (DMA based) for Bluetooth Low Energy timing critical operation
  - 2.4 GHz proprietary radio driver
  - Suitable for systems requiring compliance with the following radio frequency regulations: ETSI EN 300 328, EN 300 440, FCC CFR47 part 15, ARIB STD-T66
- Ultra-low power radio performance
  - 10 nA in SHUTDOWN mode (1.8 V)
  - 0.6 uA in DEEPSTOP mode (with external LSE and BLE wake-up sources, 1.8 V)
  - 0.9 uA in DEEPSTOP mode (with internal LSI and BLE wake-up sources, 1.8 V)
  - 4.3 mA peak current in TX (@ 0 dBm, 3.3 V)
  - 3.4 mA peak current in RX (@ sensitivity level, 3.3V)
- High performance and ultra-low power Cortex-M0+ 32-bit, running up to 64 MHz
- Dynamic current consumption: 18 µA/MHz
- Operating supply voltage: from 1.7 to 3.6 V
- -40 °C to 105 °C temperature range
- Supply and reset management
  - High efficiency embedded SMPS step-down converter with intelligent bypass mode
  - Ultra-low power power-on-reset (POR) and power-down-reset (PDR)
  - Programmable voltage detector (PVD)
- Clock sources
  - Fail safe 32 MHz crystal oscillator with integrated trimming capacitors
  - 32 kHz crystal oscillator
  - Internal low-power 32 kHz RO
- On-chip non-volatile Flash memory of 256 kB
- On-chip RAM of 64 kB or 32 kB

- One-time-programmable (OTP) memory area of 1 kB
- Embedded UART bootloader
- Ultra-low power modes with or without timer and RAM retention
- Quadrature decoder
- Enhanced security mechanisms such as:
  - Flash read/write protection
  - SWD disabling
  - Secure bootloader
- Security features
  - True random number generator (RNG)
  - Hardware encryption AES maximum 128-bit security co-processor
  - HW public key accelerator (PKA)
  - CRC calculation unit
  - 64-bit unique ID
- System peripherals
  - 1x DMA controller with 8 channels supporting ADC, SPI, I2C, USART and LPUART
  - 1x SPI
  - 2x SPI/I2S
  - 2x I^2C (SMBus/PMBus)
  - 1x PDM (digital microphone interface)
  - 1x LPUART
  - 1x USART (ISO 7816 smartcard mode, IrDA, SPI Master and Modbus)
  - 1x independent WDG
  - 1x real time clock (RTC)
  - 1x independent SysTick
  - 1x 16-bit, 6 channel advanced timer
- Up to 32 fast I/Os
  - 28 of them with wake-up capability
  - 31 of them 5 V tolerant
- Analog peripherals
  - 12-bit ADC with 8 input channels, up to 16 bits with a decimation filter
  - Battery monitoring
  - Analog watchdog
  - Analog Mic I/F with PGA
- Development support
  - Serial wire debug (SWD)
  - 4 breakpoints and 2 watchpoints
- All packages are ECOPACK2 compliant

Applications

- Industrial
- Home and industrial automation
- Smart lighting
- Fitness,wellness and sports
- Healthcare, consumer medical
- Security/proximity
- Remote control
- Assisted living

- Mobile phone peripherals
- PC peripherals

Description

The BlueNRG-LP is an ultra-low power programmable Bluetooth® Low Energy wireless SoC solution. It embeds STMicroelectronics's state-of-art 2.4 GHz RF radio IPs combining unparalleled performance with extremely long-battery lifetime. It is compliant with Bluetooth® Low Energy SIG core specification version 5.2 addressing point-to-point connectivity and Bluetooth Mesh networking and allows large-scale device networks to be established in a reliable way. The BlueNRG-LP is also suitable for 2.4 GHz proprietary radio wireless communication to address ultra-low latency applications.

The BlueNRG-LP embeds a Cortex®-M0+ microcontroller that can operate up to 64 MHz and also the BlueNRG core coprocessor (DMA based) for Bluetooth Low Energy timing critical operations.

The main Bluetooth® Low Energy 5.2 specification supported features are:

2 Mbps data rate, long range (Coded PHY), advertising extensions, channel selection algorithm #2, GATT caching, hardware support for simultaneous connection, master/slave and multiple roles simultaneously, extended packet length support.

In addition, the BlueNRG-LP provides enhanced security hardware support by dedicated hardware functions:

True random number generator (RNG), encryption AES maximum 128-bit security co-processor, public key accelerator (PKA), CRC calculation unit, 64-bit unique ID, Flash memory read and write protection.

The BlueNRG-LP can be configured to support standalone or network processor applications. In the first configuration, the BlueNRG-LP operates as single device in the application for managing both the application code and the Bluetooth Low Energy stack.

The BlueNRG-LP embeds high-speed and flexible memory types:

Flash memory of 256 kB, RAM memory of 64 kB, one-time-programmable (OTP) memory area of 1 kB, ROM memory of 7 kB.

Direct data transfer between memory and peripherals and from memory-to-memory is supported by eight DMA channels with a full flexible channel mapping by the DMAMUX peripheral.

The BlueNRG-LP embeds a 12-bit ADC, allowing measurements of up to eight external sources and up to three internal sources, including battery monitoring and a temperature sensor.

The BlueNRG-LP has a low-power RTC and one advanced 16-bit timer.

The BlueNRG-LP features standard and advanced communication interfaces:

1x SPI, 2x SPI/I2S, 1x LPUART, 1x USART supporting ISO 7816 (smartcard mode), IrDA and Modbus mode, 2x I^2C supporting SMBus/PMBus, 1x channel PDM.

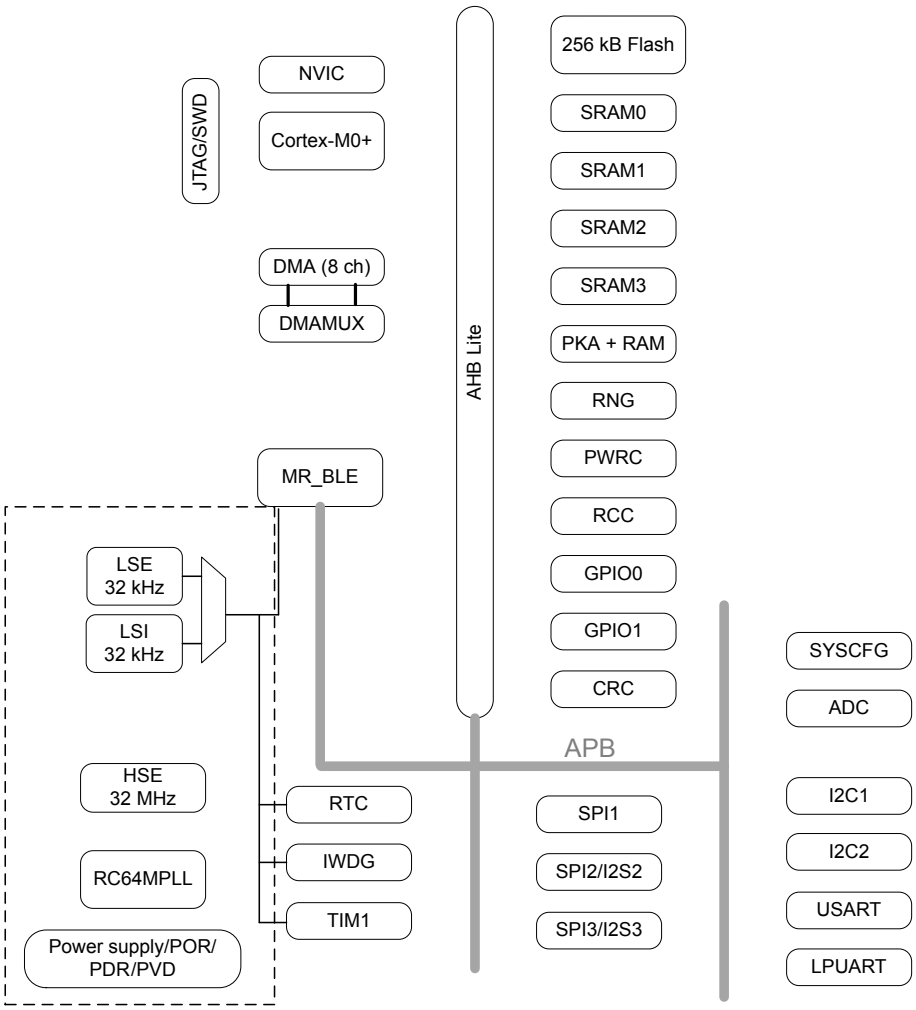
The BlueNRG-LP operates in the -40 to +105 °C temperature range from a 1.7 V to 3.6 V power supply. A comprehensive set of power-saving modes enables the design of low-power applications.

The BlueNRG-LP integrates a high efficiency SMPS step-down converter and an integrated PDR circuitry with a fixed threshold that generates a device reset when the VDD drops under 1.65 V.

The BlueNRG-LP comes in different package versions supporting up to:

32 I/Os for the QFN48 package, 20 I/Os for the QFN32 package, 30 I/Os for the WCSP49 package.

Figure 1. The BlueNRG-LP block diagram



1 Functional overview

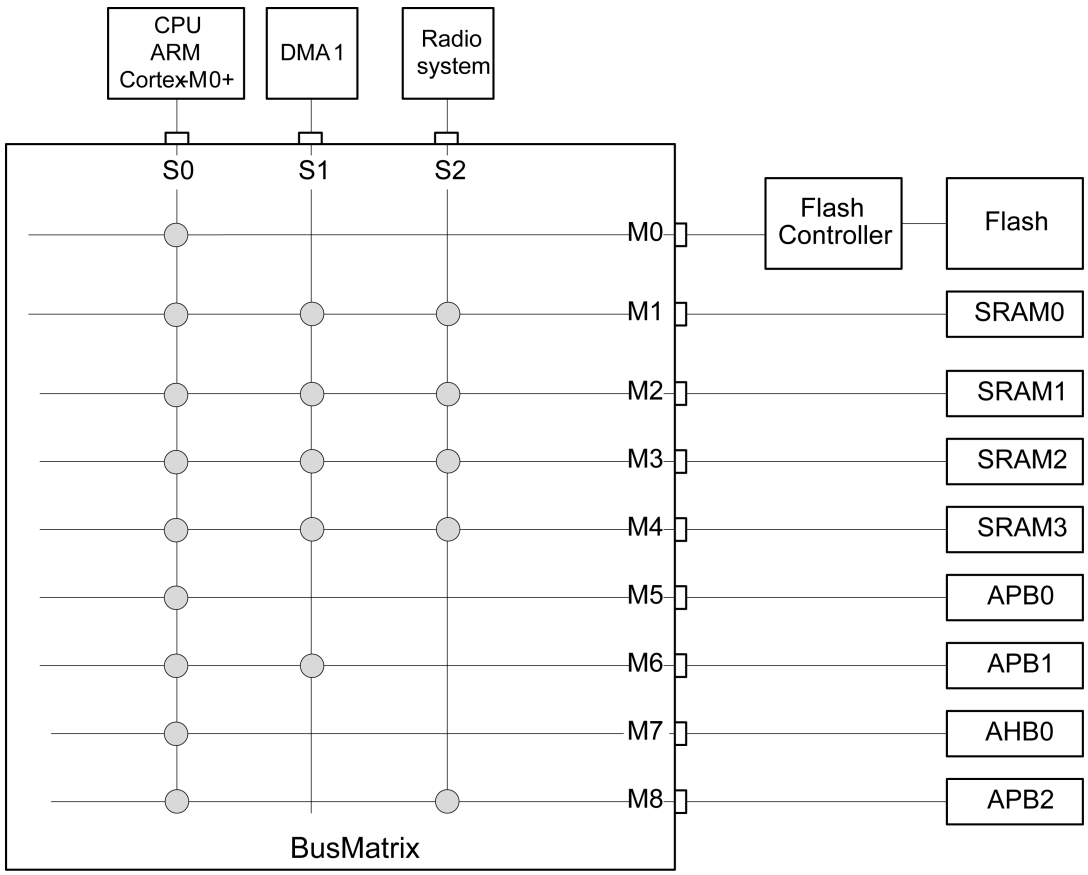
1.1 System architecture

The main system consists of 32-bit multilayer AHB bus matrix that interconnects:

- Three masters:
  - CPU (Cortex®-M0+) core S-bus
  - DMA1
  - Radio system
- Nine slaves:
  - Internal Flash memory on CPU (Cortex®-M0+) S bus
  - Internal SRAM0 (16 kB)
  - Internal SRAM1 (16 kB)
  - Internal SRAM2 (16 kB)
  - Internal SRAM3 (16 kB)
  - APB0 peripherals (through an AHB to APB bridge)
  - APB1 peripherals (through an AHB to APB bridge)
  - AHB0 peripherals
  - AHBRF including AHB to APB bridge and radio peripherals (connected to APB2)

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Bus matrix



1.2 ARM Cortex–M0+ core with MPU

The BlueNRG-LP contains an ARM Cortex-M0+ microcontroller core. The Cortex-M0+ was developed to provide a low-cost platform that meets the needs of CPU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts. The Cortex-M0+ can run from 1 MHz up to 64 MHz.

The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The interrupts are handled by the Cortex-M0+ Nested Vector Interrupt Controller (NVIC). The NVIC controls specific Cortex-M0+ interrupts as well as the BlueNRG-LP peripheral interrupts. With its embedded ARM core, the BlueNRG-LP family is compatible with all ARM tools and software.

1.3 Memories

1.3.1 Embedded Flash memory

The Flash controller implements the erase and program Flash memory operation. The flash controller also implements the read and write protection.

The Flash memory features are:

- Memory organization:
  - 1 bank of 256 kB
  - Page size: 2 kB
  - Page number 128
- 32-bit wide data read/write
- Page erase and mass erase

The Flash controller features are:

- Flash memory read operations
- Flash memory write operations: single data write or 4x32-bits burst write
- Flash memory erase operations
- Page write protect mechanism

1.3.2 Embedded SRAM

The BlueNRG-LP has a total of 64 kB of embedded SRAM, split into four banks as shown in the following table:

Table 1. SRAM overview

SRAM bank	Size	Address	Retained in DEEPSTOP
SRAM0	16 kB	0x2000 0000	Always
SRAM1	16 kB	0x2000 4000	Programmable by the user
SRAM2	16 kB	0x2000 8000	Programmable by the user
SRAM3	16 kB	0x2000 C000	Programmable by the user

1.3.3 Embedded ROM

The BlueNRG-LP has a total of 7 kB of embedded ROM. This area is ST reserved and contains:

- The UART bootloader from which the CPU boots after each reset (first 6 kB of ROM memory)
- Some ST reserved values including the ADC trimming values (the last 1 kB of ROM memory)

1.3.4 Embedded OTP

The one-time-programmable (OTP) is a memory of 1 kB dedicated for user data. The OTP data cannot be erased.

The user can protect the OTP data area by writing the last word at address 0x1000 1BFC and by performing a system reset. This operation freezes the OTP memory from further unwanted write operations.

1.3.5 Memory protection unit (MPU)

The MPU is used to manage accesses to memory to prevent one task from accidentally corrupting the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area settings, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

1.4 Security and safety

The BlueNRG-LP contains many security blocks for the BLE and the host application.

It includes:

- Flash read/write protections
- As protection against potential hacker attacks, the SWD access can be disabled
- Secure bootloader (refer to the dedicated BlueNRG-LP UART bootloader protocol application note AN5471)
- Customer storage of the BLE keys
- True random number generator (RNG)
- Private key accelerator (PKA) including:
  - Elliptic curve Diffie-Hellman (ECDH) public-private key pair calculation accelerator
  - Based on the Montgomery method for fast modular multiplications
  - Built-in Montgomery domain inward and outward transformations
    - AMBA AHB lite slave interface with a reduced command set
- Cyclic redundancy check calculation unit (CRC)

1.5 RF subsystem

The BlueNRG-LP embeds an ultra-low power radio, compliant with Bluetooth® Low Energy (BLE) specification. The BLE features 1 Mbps and 2 Mbps transfer rates as well as long range options (125 kbps, 500 kbps), supports multiple roles simultaneously acting at the same time as Bluetooth® Low Energy sensor and hub device.

The BLE protocol stack is implemented by an efficient system partitioned as follows:

- Hardware part: BlueCore handling time critical and time consuming BLE protocol parts
- Firmware part: Arm® Cortex®-M0+ core handling non time critical BLE protocol parts

1.5.1 RF front-end block diagram

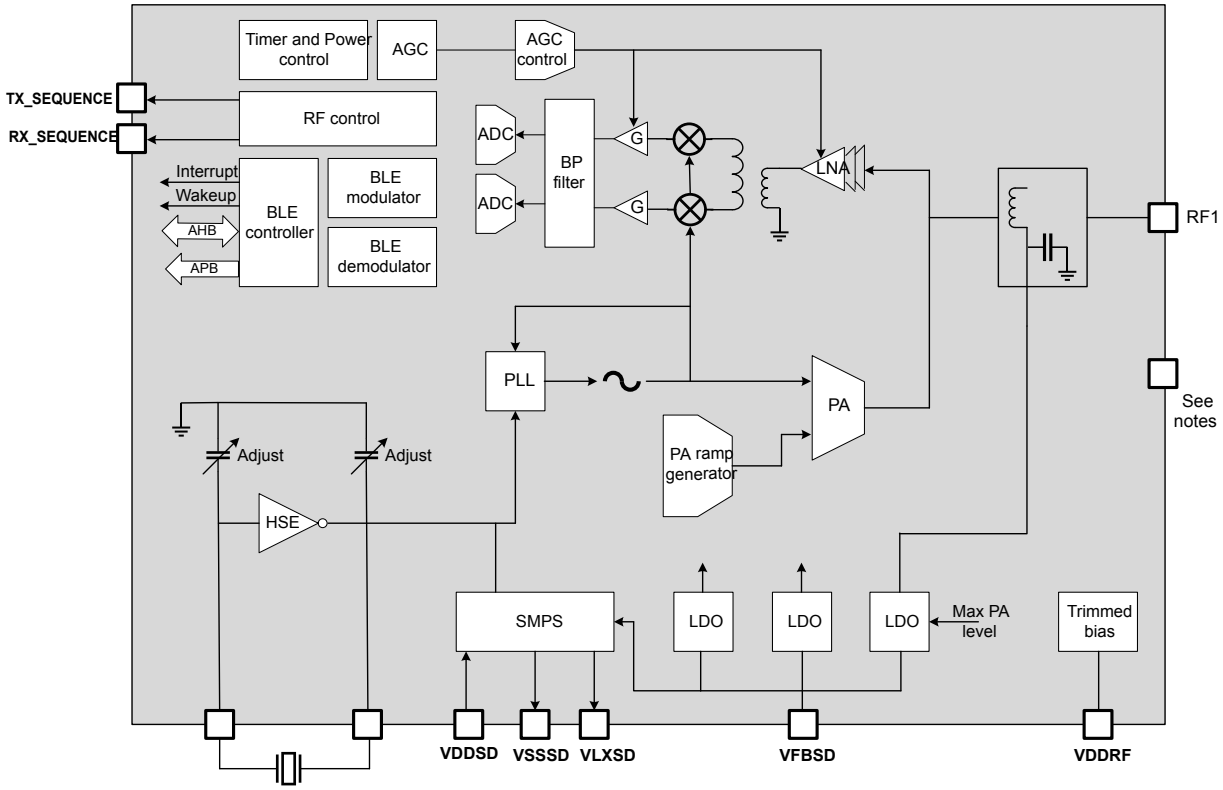
The RF front-end is based on a direct modulation of the carrier in TX, and uses a low IF architecture in RX mode.

Thanks to an internal transformer with RF pins, the circuit directly interfaces the antenna (single ended connection, impedance close to 50 Ω). The natural band pass behavior of the internal transformer simplifies outside circuitry aimed at harmonic filtering and out of band interferer rejection.

In transmit mode, the maximum output power is user selectable through the programmable LDO voltage of the power amplifier. A linearized, smoothed analog control offers a clean power ramp-up.

In receive mode, the automatic gain control (AGC) can reduce the chain gain at both RF and IF locations, for optimized interferer rejections. Thanks to the use of complex filtering and highly accurate I/Q architecture, high sensitivity and excellent linearity can be achieved.

Figure 3. BlueNRG-LP RF block diagram



Notes: QFN42 and QFN48: VSS through exposed pad,
and VSSRF pins must be connected to ground plane CSP49: VSSRF pins must be connected to ground plane.

1.6 Power supply management

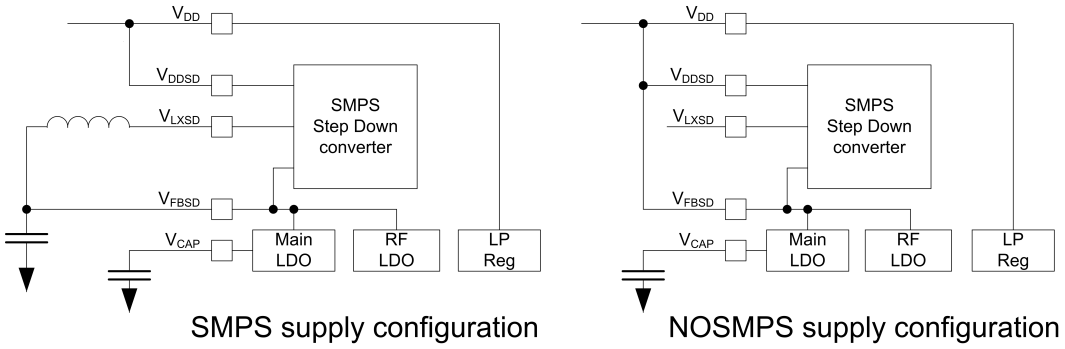
1.6.1 SMPS step-down regulator

The device integrates a step-down converter to improve low power performance when the VDD voltage is high enough. The SMPS output voltage can be programmed from 1.2 V to 1.90 V. It is internally clocked at 4 MHz or 8 MHz.

The device can be operated without the SMPS by just wiring its output to VDD. This is the case for applications where the voltage is low, or where the power consumption is not critical.

Except for the configuration SMPS OFF, an L/C BOM must be present on the board and connected to the VFBSD pad.

Figure 4. Power supply configuration

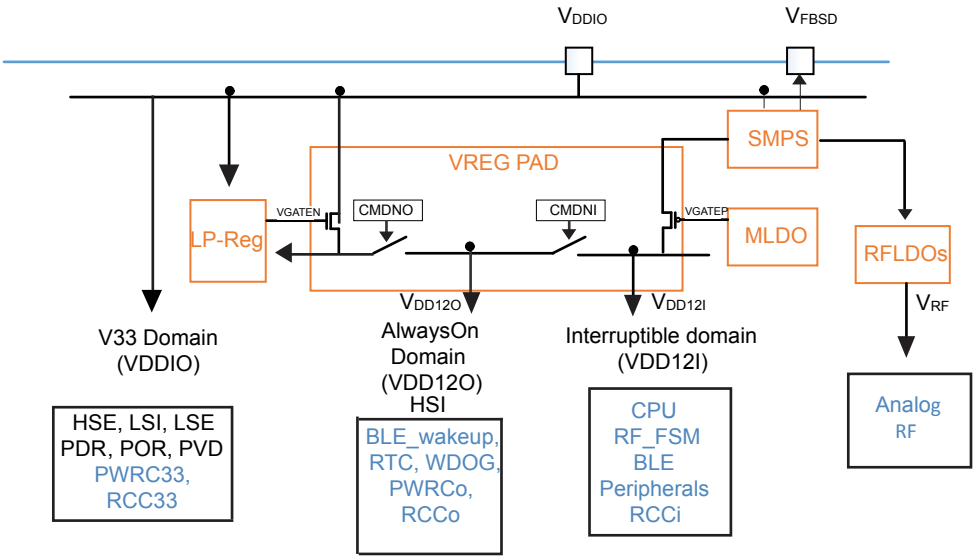


1.6.2 Power supply schemes

The BlueNRG-LP embeds three power domains:

- VDD33 (VDDIO or VDD):
  - the voltage range is between 1.7 V and 3.6 V
  - it supplies a part of the I/O ring, the embedded regulators and the system analog IPs as power management block and embedded oscillators
- VDD12o:
  - always-on digital power domain
  - this domain is generally supplied at 1.2 V during active phase of the device
  - this domain is supplied at 1.0 V during low power mode (DEEPSTOP)
- VDD12i:
  - interruptible digital power domain
  - this domain is generally supplied at 1.2 V during active phase of the device
  - this domain is shut down during low power mode (DEEPSTOP)

Figure 5. Power supply domain overview



1.6.3 Linear voltage regulators

The digital power supplies are provided by different regulators:

- The main LDO (MLDO):
  - it provides 1.2 V from a 1.4-3.3 V input voltage
  - it supplies both VDD12i and VDD12o when the device is active
  - it is disabled during the low power mode (DEEPSTOP)
- Low power LDO (LPREG):
  - it stays enabled during both active and low power phases
  - it provides 1.0 V voltage
  - it is not connected to the digital domain when the device is active
  - it is connected to the VDD12o domain during low power mode (DEEPSTOP)
- A dedicated LDO (RFLDO) to provide a 1.2 V to the analog RF block

An embedded SMPS step-down converter is available (inserted between the external power and the LDOs).

1.6.4 Power supply supervisor

The BlueNRG-LP device embeds several power voltage monitoring:

- Power-on-reset (POR): during the power-on, the device remains in reset mode if VDDIO is below a VPOR threshold (typically 1.65 V)
- Power-down-reset (PDR): during power-down, the PDR puts the device under reset when the supply voltage (VDD) drops below the VPDR threshold (around 20 mV below VPOR). The PDR feature is always enabled
- Power voltage detector (PVD): can be used to monitor the VDDIO (against a programmed threshold) or an external analog input signal. When the feature is enabled and the PVD measures a voltage below the comparator, an interrupt is generated (if unmasked)

1.7 Operating modes

Several operating modes are defined for the BlueNRG-LP:

- RUN mode
- DEEPSTOP mode
- SHUTDOWN mode

Table 2. Relationship between the low power modes and functional blocks

Mode	SHUTDOWN	DEEPSTOP	IDLE	RUN
CPU	OFF	OFF	OFF	ON
Flash	OFF	OFF	ON	ON
RAM	OFF	ON/OFF granularity 16 kB	ON/OFF	ON/OFF
Radio	OFF	OFF	ON/OFF	ON/OFF
Supply system	OFF	OFF	ON (DC-DC ON/OFF)	ON (DC-DC ON/OFF)
Register retention	OFF	ON	ON	ON
HS clock	OFF	OFF	ON	ON
LS clock	OFF	ON/OFF	ON	ON
Peripherals	OFF	OFF	ON/OFF	ON/OFF
Wake-on RTC	OFF	ON/OFF	ON/OFF	NA
Wake-on GPIOs	OFF	ON/OFF	ON/OFF	NA
Wake-on reset pin	ON	ON	ON	NA

1.7.1 RUN mode

In RUN mode the BlueNRG-LP is fully operational:

- All interfaces are active
- The internal power supplies are active
- The system clock and the bus clock are running
- The CPU core and the radio can be used

The power consumption may be reduced by gating the clock of the unused peripherals.

1.7.2 DEEPSTOP mode

The DEEPSTOP is the only low power mode of the BlueNRG-LP allowing the restart from a saved context environment and the application at wake-up to go on running.

The conditions to enter the DEEPSTOP mode are:

- The radio is sleeping (no radio activity)
- The CPU is sleeping (WFI with SLEEPDEEP bit activated)
- No unmasked wake-up sources are active

- The low power mode selection (LPMS) bit of the power controller unit is 0 (default)

In DEEPSTOP mode:

- The system and the bus clocks are stopped
- Only the essential digital power domain is ON and supplied at 1.0 V
- The bank RAM0 is kept in retention
- The other banks of RAM can be in retention or not, depending on the software configuration
- The low speed clock can be running or stopped, depending on the software configuration:
  - ON or OFF
  - Sourced by LSE or by LSI
- The RTC and the IWDG stay active, if enabled and the low speed clock is ON
- The radio wake-up block, including its timer, stay active (if enabled and the low speed clock is ON)
- Eight I/Os (PA4/ PA5/ PA6/ PA7/ PA8/ PA9/ PA10/ PA11) can be in output driving:
  - A static low or high level
  - The low speed clock
  - The RTC output

Possible wake-up sources are:

- The radio block is able to generate two events to wake up the system through its embedded wake-up timer running on low speed clock:
  - Radio wake-up time is reached
  - CPU host wake-up time is reached
- The RTC can generate a wake-up event
- The IWDG can generate a reset event
- Up to 28 GPIOs are able to wake up the system (PA0 to PA15 and PB0 to PB11)

At the wake-up, all the hardware resources located in the digital power domain that are OFF during the DEEPSTOP mode, are reset. The CPU reboots. The wake-up reason is visible in the register of the power controller.

1.7.3 SHUTDOWN mode

The SHUTDOWN mode is the least power consuming mode.

The conditions to enter SHUTDOWN mode are the same conditions needed to enter DEEPSTOP mode except that the LPMS bit of the power controller unit is 1.

In SHUTDOWN mode, the BlueNRG-LP is in ultra-low power consumption: all voltage regulators, clocks and the RF interface are not powered. The BlueNRG-LP can enter shutdown mode by internal software sequence. The only way to exit shutdown mode is by asserting and deasserting the RSTN pin.

In SHUTDOWN mode:

- The system is powered down as both the regulators are OFF
- The VDDIO power domain is ON
- All the clocks are OFF, LSI and LSE are OFF
- The I/Os pull-up and pull-down can be controlled during SHUTDOWN mode, depending on the software configuration
- The only wake-up source is a low pulse on the RSTN pin

The exit from SHUTDOWN is similar to a POR startup. The PDR feature can be enabled or disabled during SHUTDOWN.

1.8 Reset management

The BlueNRG-LP offers two different resets:

- The PORESETn: this reset is provided by the low power management unit (LPMU) analog block and corresponds to a POR or PDR root cause. It is linked to power voltage ramp-up or ramp-down. This reset impacts all resources of the BlueNRG-LP. The exit from SHUTDOWN mode is equivalent to a POR and thus generates a PORESETn. The PORESETn signal is active when the power supply of the device is below a threshold value or when the regulator does not provide the target voltage.
- The PADRESETn (system reset): this reset is built through several sources:
  - PORESETn
  - Reset due to the watchdog

    The BlueNRG-LP device embeds a watchdog timer, which may be used to recover from software crashes
  - Reset due to CPU Lockup

    The Cortex-M0+ generates a lockup to indicate the core is in the lock-up state resulting from an unrecoverable exception. The lock-up reset is masked if a debugger is connected to the Cortex-M0+
  - Software system reset

    The system reset request is generated by the debug circuitry of the Cortex®-M0+. The debugger sets the SYSRESETREQ bit of the application interrupt and reset control register (AIRCR). This system reset request through the AIRCR can also be done by the embedded software (into the hardfault handler for instance)
  - Reset from the RSTN external pin

    The RSTN pin toggles to inform that a reset has occurred

  This PADRESETn resets all resources of the BlueNRG-LP, except:
- Debug features
- Flash controller key management
- RTC timer
- Power controller unit
- Part of the RCC registers

The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of reset from the RSTN external pad, the reset pulse is generated when the pad is asserted low.

1.9 Clock management

Three different clock sources may be used to drive the system clock of the BlueNRG-LP:

- HSI: high speed internal 64 MHz RC oscillator
- PLL64M: 64 MHz PLL clock
- HSE: high speed 32 MHz external crystal

The BlueNRG-LP has also a low speed clock tree used by some timers in the radio, RTC and IWDG.

Four different clock sources can be used for this low speed clock tree:

- Low speed internal (LSI): low speed and low drift internal RC with a fixed frequency between 24 kHz and 49 kHz depending on the sample
- Low speed external (LSE) from:
  - An external crystal 32.768 kHz
  - A single-ended 32.738 kHz input signal
- A 32 kHz clock (CLK_16 MHz/512 in Figure 6. Clock tree) obtained by dividing HSI or HSE. In this case, the slow clock is not available in DEEPSTOP low power mode
- LSI_LPMU: 32 kHz clock used by the low power management unit (LPMU) analog block.

By default, after a system reset, all low speed sources are OFF.

Both the activation and the selection of the slow clock are relevant during the DEEPSTOP mode and at wakeup as slow clock generates a clock for the timers involved in wake-up event generation.

The HSI and the PLL64M clocks are provided by the same analog block called RC64MPLL. The 64 MHz clock output by this block can be:

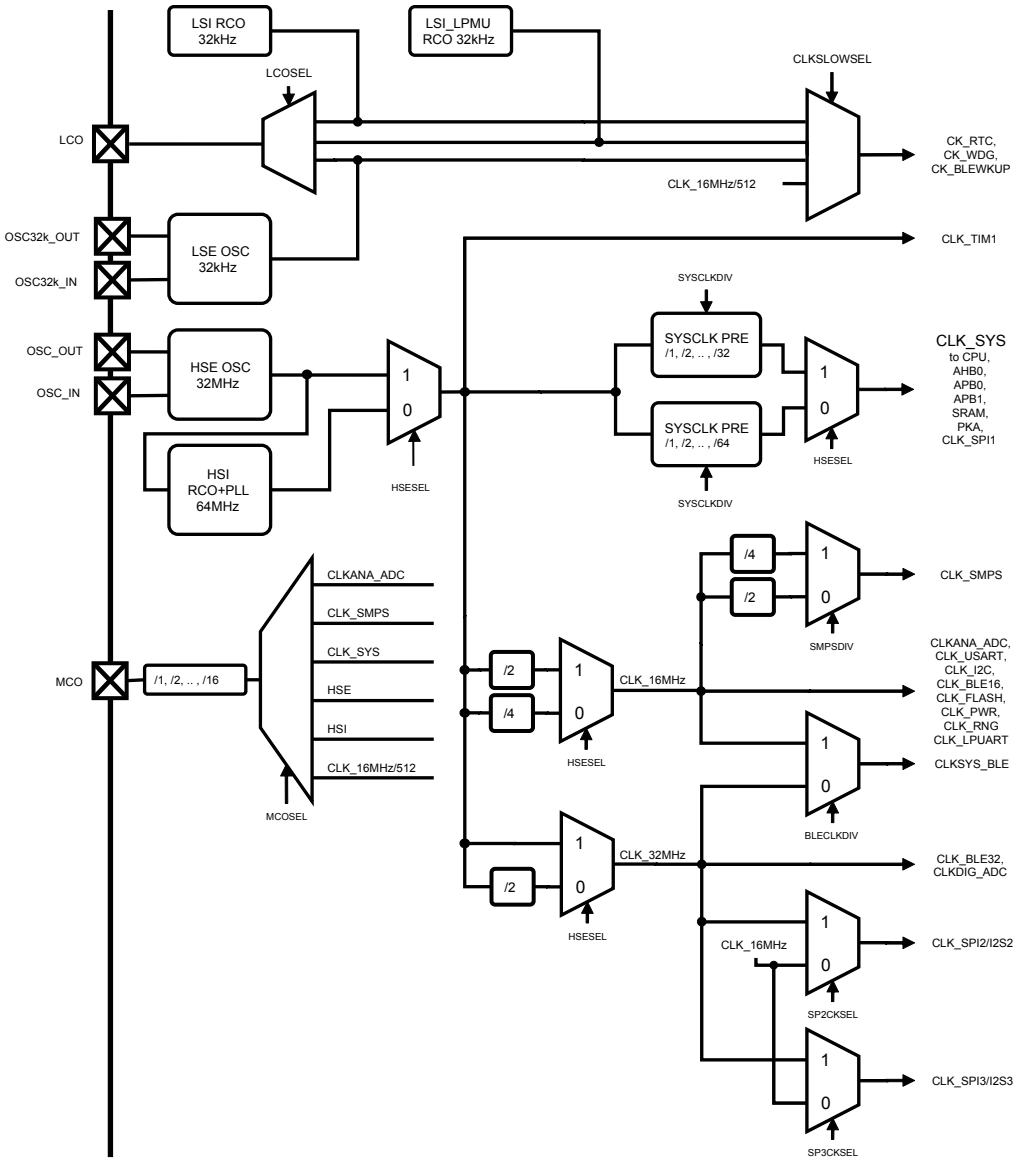
- A non-accurate clock when no external XO provides an input clock to this block (HSI)
- An accurate clock when the external XO provides the 32 MHz and once its internal PLL is locked (PLL64M)

This fast clock source is used to generate all the fast clock of the device through dividers. After reset, the CLK_SYS is divided by four to provide a 16 MHz to the whole system (CPU, DMA, memories and peripherals).

This fast clock source is also used to generate several internal fast clocks in the system:

- Always 32 MHz requested by a few peripherals like the radio
- Always 16 MHz requested by a few peripherals like serial interfaces (to maintain fixed the baud rate while system clock is switching from one frequency to another) or like the Flash controller and radio (to have a fixed reference clock to manage delays)

Figure 6. Clock tree



It is possible to output some internal clocks on external pads:

- the low speed clocks can be output on the LCO I/O

- the high speed clocks can be output on the MCO I/O

This is possible by programming the associated I/O in the correct alternate function.

Most of the peripherals only use the system clock except:

- I^2C, USART, LPUART: they always use a16 MHz clock to have a fixed reference clock for baud rate management. The goal is to allow the CPU to boost or slow down the system clock (depending on on-going activities) without impacting a potential on-going serial interface transfer on external I/Os
- SPI: when the I2S mode is used, the baud rate is always managed through the 16 MHz or 32 MHz clock. When modes other than the I2S run, the baud rate is managed by the system clock. This implies its baud rate is impacted by dynamic system clock frequency changes
- RNG: in parallel to the system clock, the RNG always uses 16 MHz clock to generate at a constant frequency the random number whatever the system clock frequency
- Flash controller: in parallel to the system clock, the Flash controller always uses 16 MHz clock to generate specific delays required by the Flash memory during programming and erase operations for example
- PKA: in parallel to the system clock, the PKA uses a clock at half of the system clock frequency
- Radio: it does not directly use the system clock for its APB/AHB interfaces, but the system clock with a potential divider (1 or 2 or 4). In parallel, the radio always uses 16 MHz and always 32 MHz for modulator, demodulator and to have a fixed reference clock to manage specific delays
- ADC: in parallel to the system clock, ADC uses a 64 MHz prescaled clock running at 16 MHz

1.10 Boot mode

Following CPU boot, the application software can modify the memory map at address 0x0000 0000. This modification is performed by programming the REMAP bit in the Flash controller.

The following memory can be remapped:

- Main Flash memory
- SRAM0 memory

1.11 Embedded UART bootloader

The BlueNRG-LP has a pre-programmed bootloader supporting UART protocol with automatic baud rate detection. The main features of the embedded bootloader are:

- Auto baud rate detection up to 1 Mbps
- Flash mass erase, section erase
- Flash programming
- Flash readout protection enable/disable

The pre-programmed bootloader is an application, which is stored in the BlueNRG-LP internal ROM at manufacturing time by STMicroelectronics. This application allows upgrading the device Flash with a user application using a serial communication channel (UART).

Bootloader is activated by hardware by forcing PA10 high during hardware reset, otherwise, application residing in Flash is launched.

Note: Bootloader protocol is described in a separate application note (the BlueNRG-LP UART bootloader protocol, AN5471)

1.12 General purpose inputs/outputs (GPIO)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB0 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

1.13 Direct memory access (DMA)

The DMA is used in order to provide high-speed data transfer between peripherals and memory as well as memory-to-memory. Data can be quickly moved by DMA without any CPU actions. In this manner, CPU resources are free for other operations.

The DMA controller has eight channels in total. Each has an arbiter to handle the priority among DMA requests.

DMA main features are:

- Eight independently configurable channels (requests)
- Each of the eight channels is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software
- Priorities among requests from channels of DMA are software programmable (four levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, and so on)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size
- Support for circular buffer management
- Three event flags (DMA half transfer, DMA transfer complete and DMA transfer error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer (RAM only)
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to SRAMs and APB1 peripherals as source and destination
- Programmable number of data to be transferred: up to 65536

1.14 Nested vectored interrupt controller (NVIC)

The interrupts are handled by the Cortex®-M0+ nested vector interrupt controller (NVIC). NVIC controls specific Cortex®-M0+ interrupts as well as the BlueNRG-LP peripheral interrupts.

The NVIC benefits are the following:

- Nested vectored interrupt controller that is an integral part of the ARM® Cortex®-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Control system exceptions and peripheral interrupts
- NVIC supports 32 vectored interrupts
- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation using the ARM® exceptions SVCall and PendSV
- Support for NMI
- ARM® Cortex® M0+ vector table offset register VTOR implemented

NVIC hardware block provides flexible interrupt management features with minimal interrupt latency.

1.15 Analog digital converter (ADC)

The BlueNRG-LP embeds a 12-bit ADC. The ADC consists of a 12-bit successive approximation analog-to-digital converter (SAR) with 2 x 8 multiplexed channels allowing measurements of up to eight external sources and up to two internal sources.

It embeds a PDM interface integrating a digital filter for processing PDM stream coming from a digital microphone. It also embeds a dedicated ECM microphone feature with which it is possible to connect an analog microphone directly to the ADC port of the BlueNRG-LP.

The ADC main features are:

- Conversion frequency is up to 1 Msps
- Three input voltage ranges are supported (0 - 1.2 V, 0 - 2.4 V, 0 - 3.6 V)
- Up to eight analog single-ended channels or four analog differential inputs or a mix of both
- One analog microphone supported through two GPIOs configured in analog mode (an input for the analog microphone and a Vbias output for the analog microphone)
- Temperature sensor conversion
- Battery level conversion up to 3.6 V

- Continuous or single acquisition
- Digital decimation filter to process a digital audio PDM stream provided by 2 GPIOs and for ADC post-processing, especially for analog audio stream
- Five modes of conversion are possible:
  - ADC continuous or single mode
  - Analog continuous audio mode
  - Occasional conversions
  - Digital continuous audio mode
  - Full mode
- ADC down-sampler for multi-purpose applications to improve analog performance while off-loading the CPU (ratio adjustable from 1 to 128)
- A watchdog feature to inform when data is outside thresholds (available for all modes except the digital audio mode)
- DMA capability
- Interrupt sources with flags

1.15.1 Digital microphone MEMS interface

The digital microphone MEMS interface aims to interconnect with an external digital MEMS microphone. The BlueNRG-LP can configure two GPIOs as PDM interface. The PDM_CLK provides the clock output signal, programmable in frequency, to the microphone, while the PDM_DATA receives the PDM output data from the microphone. The decimation filter and the digital control resources are used to handle the PDM data stream.

1.15.2 Analog microphone interface

The analog microphone interface is dedicated to the analog microphone signal. The input audio signal is amplified with a programmable gain amplifier (PGA) from 0 dB to 30 dB, then the data stream is sampled by ADC and processed through the decimation filter.

1.15.3 Temperature sensor

The temperature sensor (TS) generates a voltage that varies linearly with temperature. The temperature sensor is internally connected to the ADC input channel, which is used to convert the sensor output voltage into a digital value.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

1.16 True random number generator (RNG)

RNG is a random number generator based on a continuous analog noise that provides a 16-bit value to the host when read. The minimum period is 1.25 us, corresponding to 20 RNG clock cycles between two consecutive random number.

1.17 Timers and watchdog

The BlueNRG-LP includes one advanced 16-bit timer, one watchdog timer and a SysTick timer.

1.17.1 Advanced control timer (TIM1)

The advanced-control timer can be considered as a three-phase PWM multiplexed on six channels. The six channels have complementary PWM outputs with programmable inserted dead-times.

They can also be used as general-purpose timers for:

- Input capture (except channels 5 and 6)
- Output compare
- PWM generation (edge and center-aligned mode)
- One-pulse mode output

1.17.2 Independent watchdog (IWDG)

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from the LS clock and it can operate in DEEPSTOP mode. It can also be used as a watchdog to reset the device when a problem occurs.

1.17.3 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0

1.18 Real-time clock (RTC)

The RTC is an independent BCD timer/counter. The RTC provides a time of day/clock/calendar with programmable alarm interrupt. RTC includes also a periodic programmable wake-up flag with interrupt capability. The RTC provides an automatic wake-up to manage all low power modes.

Two 32-bit registers contain seconds, minutes, hours (12- or 24-hour format), day (day of week), date (day of month), month, and year, expressed in binary coded decimal format (BCD). The sub-second value is also available in binary format. Compensations for 28-, 29- (leap year), 30-, and 31-day months are performed automatically. Daylight saving time compensation can also be performed. Additional 32-bit registers contain the programmable alarm sub seconds, seconds, minutes, hours, day, and date.

A digital calibration circuit with 0.95 ppm resolution is available to compensate for quartz crystal inaccuracy. After power-on reset, all RTC registers are protected against possible parasitic write accesses. As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (RUN mode, low power mode or under system reset). The RTC counter does not freeze when CPU is halted by a debugger.

1.19 Inter-integrated circuit interface (I^2C)

The BlueNRG-LP embeds two I^2Cs. The I^2C bus interface handles communications between the microcontroller and the serial I^2C bus. It controls all I^2C bus-specific sequencing, protocol, arbitration and timing.

The I^2C peripheral supports:

- I^2C bus specification and user manual rev. 5 compatibilities:
  - Slave and master modes
  - Multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (fm+), with a bitrate up to 1 Mbit/s and 20 mA output driver I/Os
  - 7-bit and 10-bit addressing mode
  - Multiple 7-bit slave addresses (2 addresses, 1 with configurable mask)
  - All 7-bit address acknowledge mode
  - General call
  - Programmable setup and hold times
  - Easy to use event management
  - Optional clock stretching
  - Software reset
- System management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - Host and device support
  - SMBus alert
  - Timeouts and idle condition detection

- Power system management protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I²C communication speed to be independent from the PCLK reprogramming
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

1.20 Universal synchronous/asynchronous receiver transmitter (USART)

USART offers flexible full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. USART is able to communicate with a speed up to 2 Mbit/s. Furthermore, USART is able to detect and automatically set its own baud rate, based on the reception of a single character.

The USART peripheral supports:

- Synchronous one-way communication
- Half-duplex single wire communication
- Local interconnection network (LIN) master/slave capability
- Smart card mode, ISO 7816 compliant protocol
- IrDA (infrared data association) SIR ENDEC specifications
- Modem operations (CTS/RTS)
- RS485 driver enable
- Multiprocessor communications
- SPI-like communication capability

High speed data communication is possible by using DMA (direct memory access) for multibuffer configuration.

1.21 LPUART

LPUART is a UART which allows bidirectional UART communications. It supports half-duplex single wire communications and modem operations (CTS/RTS). It also supports multiprocessor communications. DMA (direct memory access) can be used for data transmission/reception.

1.22 Serial peripheral interface (SPI)

The BlueNRG-LP has three SPI interfaces (SPI1, SPI2, SPI3) allowing communication up to 32 Mbit/s in both master and slave modes. The SPI peripheral supports:

- Master or slave operation
- Multimaster support
- Full-duplex synchronous transfers on three lines
- Half-duplex synchronous transfer on two lines (with bidirectional data line)
- Simplex synchronous transfers on two lines (with unidirectional data line)
- Serial communication with external devices
- NSS management by hardware or software for both master and slave: dynamic change of master/slave operations
- SPI Motorola support
- SPI TI mode support
- Hardware CRC feature for reliable communication

All SPI interfaces can be served by the DMA controller.

1.23 Inter-IC sound (I2S)

The BlueNRG-LP SPI interfaces: SPI2 and SPI3 support the I2S protocol. The I2S interface can operate in slave or master mode with full duplex and half-duplex communication. It can address four different audio standards:

- Philips I2S standard
- MSB-justified standards (left-justified)
- LSB-justified standards (right-justified)
- PCM standard.

The I2S interfaces DMA capability for transmission and reception.

1.24 Serial wire debug port

The BlueNRG-LP embeds an ARM SWD interface that allows interactive debugging and programming of the device. The interface is composed of only two pins: SWDIO and SWCLK. The enhanced debugging features for developers allow up to 4 breakpoints and up to 2 watchpoints.

1.25 TX and RX event alert

The BlueNRG-LP is provided with the TX_SEQUENCE and RX_SEQUENCE signals which alert, respectively, transmission and reception activities.

A signal can be enabled for TX and RX on two pins, through alternate functions:

- TX_SEQUENCE is available on PA10 (AF2) or PB15 (AF1).
- RX_SEQUENCE is available on PA8 (AF2) or PA11 (AF2).

The signal is high when radio is in TX (or RX), low otherwise.

The signals can be used to control external antenna switching and support coexistence with other wireless technologies.

2 Pinouts and pin description

The BlueNRG-LP comes in three package versions: QFN48 offering 32 GPIOs, WCSP49 offering 30 GPIOs and QFN32 offering 20 GPIOs.

Figure 7. Pinout top view (QFN48 package)

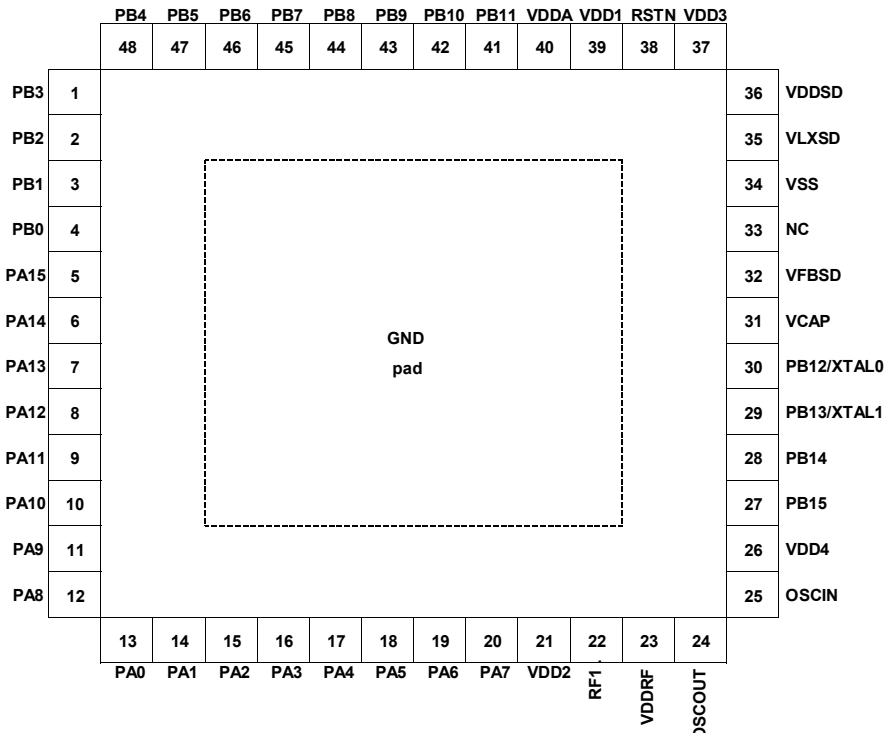


Figure 8. **Pinout top view (QFN32 package)**

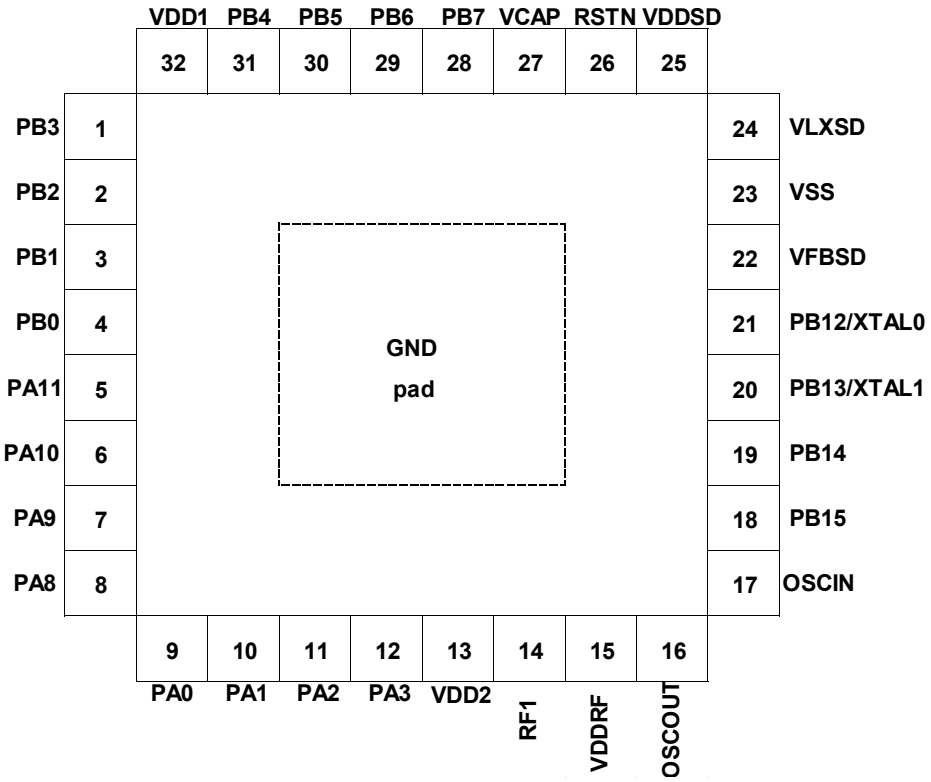


Figure 9. **Pinout top view (WLCSP49 package)**

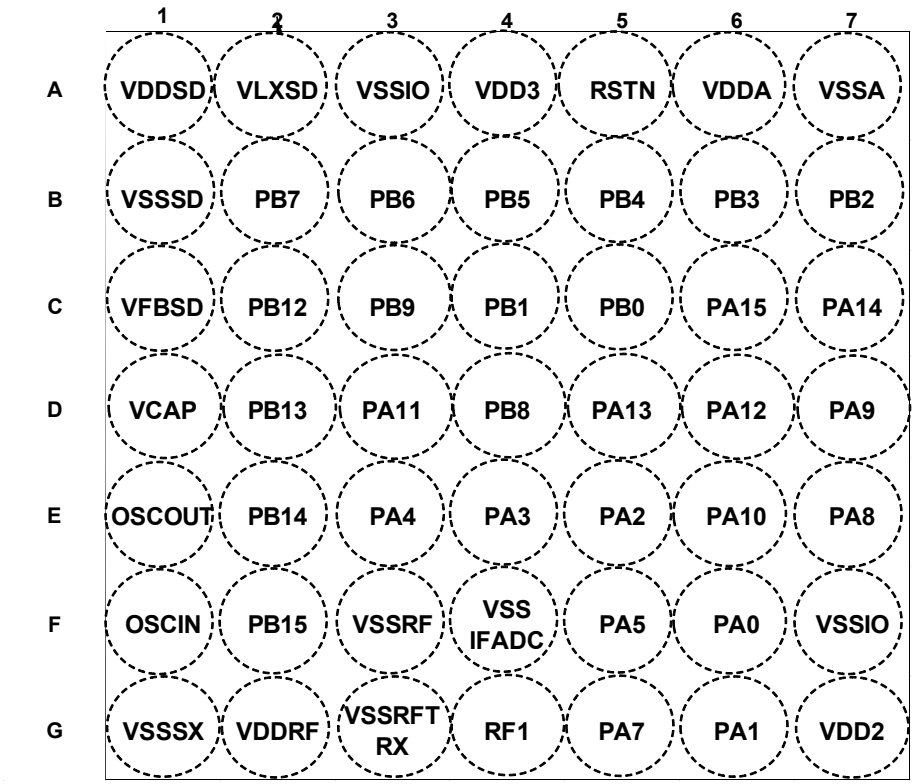


Table 3. **Pin description**

Pin number			Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
QFN48	QFN32	WLCSP49					
1	1	B6	PB3	I/O	FT_a	USART_CTS, LPUART_TX, TIM1_CH4	ADC_VINP0, wakeup
2	2	B7	PB2	I/O	FT_a	USART_RTS_DE, PDM_DATA, TIM1_CH3	ADC_VINM0, wakeup
3	3	C4	PB1	I/O	FT_a	SPI1_NSS, PDM_CLK, TIM1_ETR	ADC_VINP1, wakeup
4	4	C5	PB0	I/O	FT_a	USART_RX, LPUART_RTS_DE, TIM1_CH2N	ADC_VINM1, wakeup
5	-	C6	PA15	I/O	FT_a	I2C2_SMBA, SPI1_MOSI, TIM1_BKIN2	ADC_VINP2, wakeup
6	-	C7	PA14	I/O	FT_a	I2C2_SDA, SPI1_MISO, TIM1_BKIN	ADC_VINM2, wakeup
7	-	D5	PA13	I/O	FT_a	I2C2_SCL, SPI1_SCK, SPI2_MISO, TIM1_ETR, I2S2_MISO	ADC_VINP3, wakeup
8	-	D6	PA12	I/O	FT_a	I2C1_SMBA, SPI1_NSS, SPI2_MOSI,TIM1_CH1, I2S2_SD	ADC_VINM3, wakeup

Pin number			Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
QFN48	QFN32	WLCSP49					
9	5	D3	PA11	I/O	FT	MCO, SPI1_NSS, RX_SEQUENCE, SPI3_MOSI, TIM1_CH6, I2S3_SD	Wakeup, GPIO in DEEPSTOP, RTC_OUT
10	6	E6	PA10	I/O	FT	LCO, SPI1_MISO, TX_SEQUENCE, SPI3_MCK, TIM1_CH5, I2S3_MCK	BOOT, wakeup, GPIO in DEEPSTOP, LCO
11	7	D7	PA9	I/O	FT	USART_TX, SPI1_SCK, RTC_OUT, SPI3_NSS, TIM1_CH4, I2S3_WS	Wakeup, GPIO in DEEPSTOP, LCO
12	8	E7	PA8	I/O	FT	USART_RX, SPI1_MOSI, RX_SEQUENCE, SPI3_MISO, TIM1_CH3, I2S3_MISO	Wakeup, GPIO in DEEPSTOP, RTC_OUT
13	9	F6	PA0	I/O	FT_f	I2C1_SCL, USART_CTS, SPI2_MCK, TIM1_CH3, I2S2_MCK	Wakeup
14	10	G6	PA1	I/O	FT_f	I2C1_SDA, SPI2_MISO, USART_TX, TIM1_CH4, I2S2_MISO	Wakeup
15	11	E5	PA2	I/O	FT	SWDIO, USART_CK, TIM_BKIN, SPI3_MCK, TIM1_CH5, I2S3_MCK	Wakeup
16	12	E4	PA3	I/O	FT	SWCLK, USART_RTS_DE, TIM_BKIN2, SPI3_SCK, TIM1_CH6, I2S3_SCK	Wakeup
17	-	E3	PA4	I/O	FT	LCO, SPI2_NSS, LPUART_TX, TIM1_CH1, I2S2_WS	Wakeup, GPIO in DEEPSTOP, LCO
18	-	F5	PA5	I/O	FT	MCO, SPI2_SCK, LPUART_RX, TIM1_CH2, I2S2_SCK	Wakeup, GPIO in DEEPSTOP, LCO
19	-	-	PA6	I/O	FT	LPUART_CTS, SPI2_MOSI, SPI2_NSS, TIM1_CH1, I2S2_SD, I2S2_WS	Wakeup, GPIO in DEEPSTOP, LCO
20	-	G5	PA7	I/O	FT	LPUART_RTS_DE, SPI2_MISO, SPI2_SCK, TIM1_CH2, I2S2_MISO, I2S2_SCK	Wakeup, GPIO in DEEPSTOP, RTC_OUT
21	13	G7	VDD2	S	-	--	1.7-3.6 battery voltage input
22	14	G4	RF1	I/O	RF	-	RF input/output. Impedance 50 Ω
23	15	G2	VDDRF	S	-	-	1.7-3.6 battery voltage input
24	16	E1	OSCOUT	I/O	RF	-	32 MHz crystal
25	17	F1	OSCIN	I/O	RF	-	32 MHz crystal
26	-	-	VDD4	S	-	-	1.7-3.6 battery voltage input

Pin number			Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
QFN48	QFN32	WLCSP49					
27	18	F2	PB15	I/O	FT	I2C1_SMBA, TX_SEQUENCE, MCO, TIM1_CH4N, TIM1_CH6, USART_TX	-
28	19	E2	PB14	I/O	FT_a	SPI1_MOSI, I2C2_SDA, TIM1_ETR, TIM1_CH3N, TIM1_CH5, USART_RX	VIN_PVD
29	20	D2	PB13	I/O	FT	SPI1_MISO, I2C2_SCL, PDM_CLK, TIM1_BKIN2, TIM1_CH4	SXTAL1
30	21	C2	PB12	I/O	FT	SPI1_SCK, LCO, PDM_DATA, TIM1_BKIN, TIM1_CH3	SXTAL0
31	27	D1	VCAP	S	-	-	1.2 Vdigital core
32	22	C1	VFBSD	S	-	-	SMPS output
33			NC	S	-	-	-
34	23	B1	VSSSD	S	-	-	SMPS Ground
35	24	A2	VLXSD	S	-	-	SMPS input/output
36	25	A1	VDDSD	S	-	-	1.7-3.6 battery voltage input
37	-	A4	VDD3	S	-	-	1.7-3.6 battery voltage input
38	26	A5	RSTN	I/O	RST	-	Reset pin
39	32	-	VDD1	S	-	-	1.7-3.6 battery voltage input
40	-	A6	VDDA	S	-	-	1.2 V analog ADC core
41	-	-	PB11	I/O	FT	SPI1_SCK, SPI2_NSS, I2C1_SCL, TIM1_CH1, TIM1_CH4N, I2S2_WS	Wakeup
42	-	-	PB10	I/O	FT	SPI1_NSS, SPI2_SCK, I2C1_SDA, TIM1_CH2, TIM1_CH3N, I2S2_SCK	Wakeup
43	-	C3	PB9	I/O	FT	USART_TX, LPUART_CTS, SPI2_MCK, TIM1_CH1N, TIM1_CH2N, I2S2_MCK	Wakeup
44	-	D4	PB8	I/O	FT	USART_CK, LPUART_RX, TIM1_CH4, TIM1_CH1N	Wakeup
45	28	B2	PB7	I/O	FT_f	I2C2_SDA, SPI2_SCK, LPUART_RX, TIM1_CH2, I2S2_SCK	Wakeup
46	29	B3	PB6	I/O	FT_f	I2C2_SCL, SPI2_NSS, LPUART_TX, TIM1_CH1, I2S2_WS	Wakeup
47	30	B4	PB5	I/O	TT	LPUART_RX, SPI2_MOSI, PDM_CLK, I2S2_SD	PGA_VBIAS_MIC(1), wakeup
48	31	B5	PB4	I/O	FT	LPUART_TX, SPI2_MISO, PDM_DATA, I2S2_MISO	PGA_VIN, wakeup
-	-	A7	VSSA	S	-	-	Ground analog ADC core

Pin number			Pin name (function after reset)	Pin type	I/O structure	Alternate functions	Additional functions
QFN48	QFN32	WLCSP49					
-	-	A3	VSSIO	S	-	-	Ground I/O
-	-	F7	VSSIO	S	-	-	Ground I/O
-	-	F4	VSSIFADC	S	-	-	Ground analog RF
-	-	G1	VSSSX	S	-	-	Ground analog RF
-	-	G3	VSSRFTRX	S	-	-	Ground analog RF
-	-	F3	VSSRF	S	-	-	Ground analog RF
Exposed pad	Exposed pad	-	GND	S	-	-	Ground

1. *This pin is not 5 V tolerant.*

Table 4. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below, the pin name and the pin function during and after reset are the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		TT	3.6 V tolerant I/O
		RF	RF I/O
		RST	Bidirectional reset pin with weak pull-up resistor
		Options for TT or FT I/Os	
		_f(1).	I/O, Fm+ capable
		_a(2).	I/O, with analog switch function supplied by IO BOOSTER(3)
Notes		Unless otherwise specified by a note, all I/Os are set as analog inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

1. *The related I/O structures in Table 3. Pin description are: FT_f*
2. *The related I/O structures in Table 3. Pin description are: FT_a*
3. *IO BOOSTER block allows the good behavior of those switches to be guaranteed when the VBAT goes below 2.7 V. Refer to the BlueNRG-LP reference Manual (RM0479) for more details.*

Table 5. Alternate function port A

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		I2C1/I2C2/ SYS_AF LPUART/ USART	SPI1/SPI2/ SYS_AF/ USART/I2S2	SPI1/ SPI2/RTC USART/ TIM/ I2S2	SPI2/ SPI3 LPUART/ I2S2/ I2S3	TIM1	SYS_AF	-	SYS_AF
Port A	PA0	I2C1_SCL	USART_CTS	SPI2_MCK/ I2S2_MCK	-	TIM1_CH3	-	-	-

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		I2C1/I2C2/ SYS_AF LPUART/ USART	SPI1/SPI2/ SYS_AF/ USART/I2S2	SPI1/ SPI2/RTC USART/ TIM/ I2S2	SPI2/ SPI3 LPUART/ I2S2/ I2S3	TIM1	SYS_AF	-	SYS_AF
Port A	PA1	I2C1_SDA	SPI2_MISO/ I2S2_MISO	USART_TX	-	TIM1_CH4	-	-	-
	PA2	TMS_SWDIO	USART_CK	TIM_BKIN	SPI3_MCK/ I2S3_MCK	TIM1_CH5	TMS_SWDIO	-	TMS_SWDIO
	PA3	TCK_SWCLK	USART_RTS_DE	TIM_BKIN2	SPI3_SCK/ I2S3_SCK	TIM1_CH6	TCK_SWCLK	-	TCK_SWCLK
	PA4	LCO	SPI2_NSS/ I2S2_WS	-	LPUART_TX	TIM1_CH1	-	-	-
	PA5	MCO	SPI2_SCK/ I2S2_SCK	-	LPUART_RX	TIM1_CH2	-	-	-
	PA6	LPUART_CTS	SPI2_MOSI/ I2S2_SD	-	SPI2_NSS/ I2S2_WS	TIM1_CH1	-	-	-
	PA7	LPUART_RTS_DE	SPI2_MISO/ I2S2_MISO	-	SPI2_SCK/ I2S2_SCK	TIM1_CH2	-	-	-
	PA8	USART_RX	SPI1_MOSI	-	SPI3_MISO/ I2S3_MISO	TIM1_CH3	-	-	-
	PA9	USART_TX	SPI1_SCK	RTC_OUT	SPI3_NSS/ I2S3_WS	TIM1_CH4	-	-	-
	PA10	LCO	SPI1_MISO	-	SPI3_MCK/ I2S3_MCK	TIM1_CH5	-	-	-
	PA11	MCO	SPI1_NSS	-	SPI3_MOSI/ I2S3_SD	TIM1_CH6	-	-	-
	PA12	I2C1_SMBA	TMS_SWDIO	SPI1_NSS	SPI2_MOSI/ I2S2_SD	TIM1_CH1	-	-	-
	PA13	I2C2_SCL	TCK_SWCLK	SPI1_SCK	SPI2_MISO/ I2S2_MISO	TIM1_ETR	-	-	-
	PA14	I2C2_SDA	-	SPI1_MISO		TIM1_BKIN	-	-	-
	PA15	I2C2_SMBA	-	SPI1_MOSI	-	TIM1_BKIN2	-	-	-

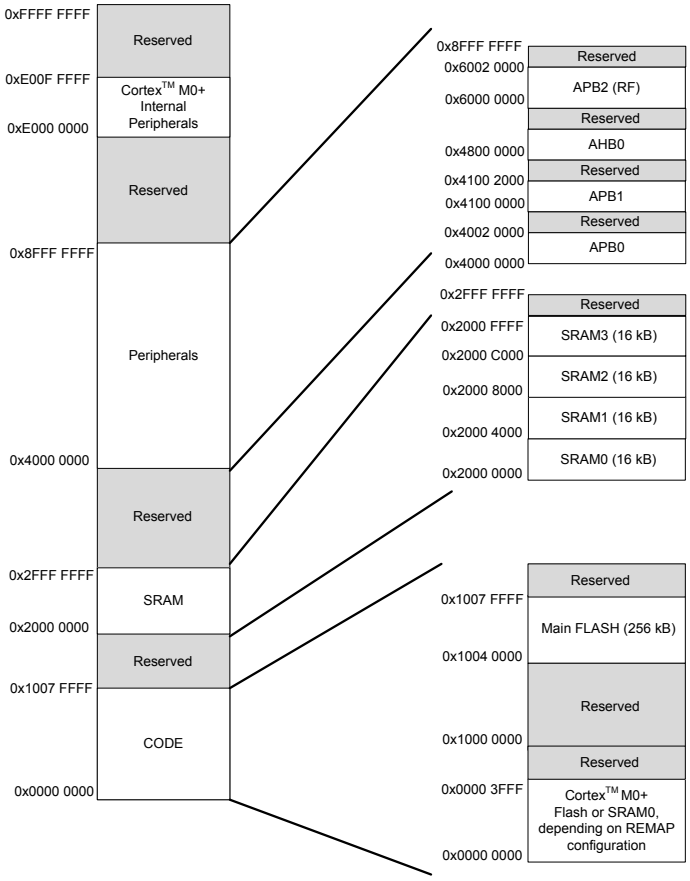
Table 6. Alternate function port B

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SPI1/I2C2 USART/LPUART	PDM/SYS_AF/I2C2 LPUART/SPI2/I2S2	SPI2/ I2C1/PDM TIM1/ SYS_AF/ I2S2	TIM1/PDM LPUART	TIM1	-	-	USART
Port B	PB0	USART_RX	LPUART_RTS_DE	-	TIM1_CH2N	-	-	-	-
	PB1	SPI1_NSS	PDM_CLK	-	TIM1_ETR	-	-	-	-
	PB2	USART_RTS_DE	PDM_DATA	-	TIM1_CH3	-	-	-	-
	PB3	USART_CTS	LPUART_TX	-	TIM1_CH4	-	-	-	-
	PB4	LPUART_TX	SPI2_MISO/ I2S2_MISO	-	PDM_DATA	-	-	-	-
	PB5	LPUART_RX	SPI2_MOSI/ I2S2_SD	-	PDM_CLK	-	-	-	-
	PB6	I2C2_SCL	SPI2_NSS/ I2S2_WS	-	LPUART_TX	TIM1_CH1	-	-	-
	PB7	I2C2_SDA	SPI2_SCK/ IS2S_SCK	-	LPUART_RX	TIM1_CH2	-	-	-
	PB8	USART_CK	LPUART_RX	-	TIM1_CH4	TIM1_CH1N	-	-	-
	PB9	USART_TX	LPUART_CTS	SPI2_MCK/ I2S2_MCK	TIM1_CH1N	TIM1_CH2N	-	-	-
	PB10	SPI1_NSS	SPI2_SCK/ I2S2_SCKK	I2C1_SDA	TIM1_CH2	TIM1_CH3N	-	-	-
	PB11	SPI1_SCK	SPI2_NSS/ I2S2_WS	I2C1_SCL	TIM1_CH1	TIM1_CH4N	-	-	-
	PB12	SPI1_SCK	LCO	PDM_DATA	TIM1_BKIN	TIM1_CH3	-	-	-
	PB13	SPI1_MISO	I2C2_SCL	PDM_CLK	TIM1_BKIN2	TIM1_CH4	-	-	-
	PB14	SPI1_MOSI	I2C2_SDA	TIM1_ETR	TIM1_CH3N	TIM1_CH5	-	-	USART_RX
	PB15	I2C1_SMBA	TX_SEQUENCE	MCO	TIM1_CH4N	TIM1_CH6	-	-	USART_TX

3 Memory mapping

Program memory, data memory and registers are organized within the same linear 4-Gbyte address space. The detailed memory map and the peripheral mapping of the BlueNRG-LP can be found in the reference manual (RM0479).

Figure 10. Memory map



4 Application circuits

The schematics below are purely indicative.

Figure 11. Application circuit: DC-DC converter, QFN48 package

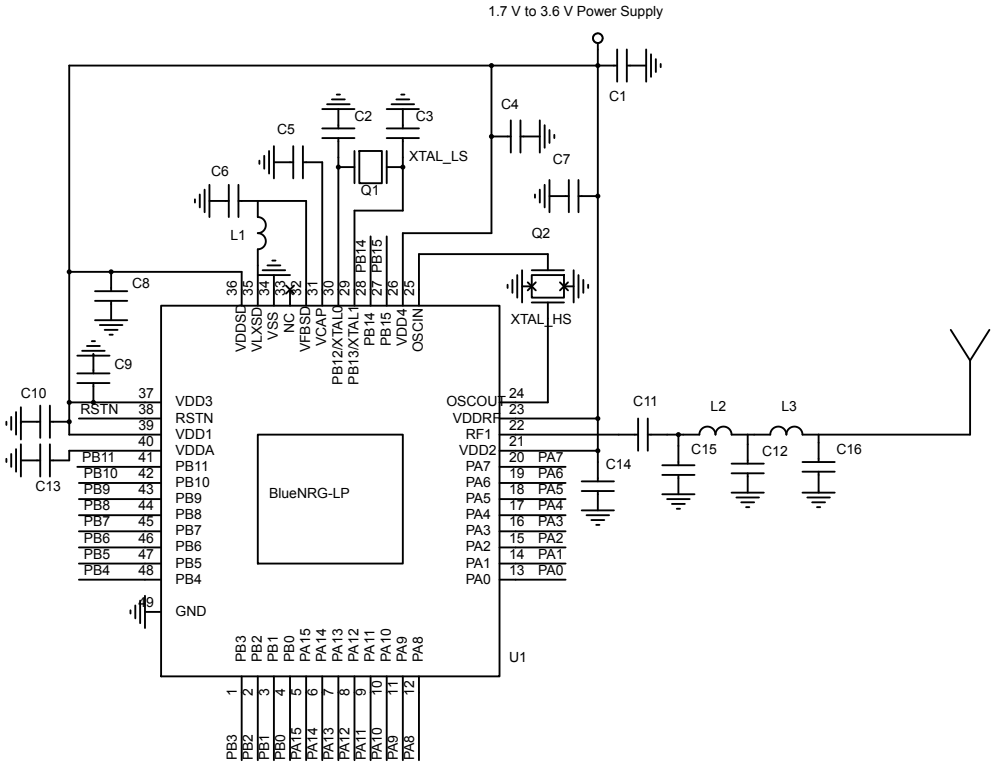


Figure 12. **Application circuit: DC-DC converter, WCSP49 package**

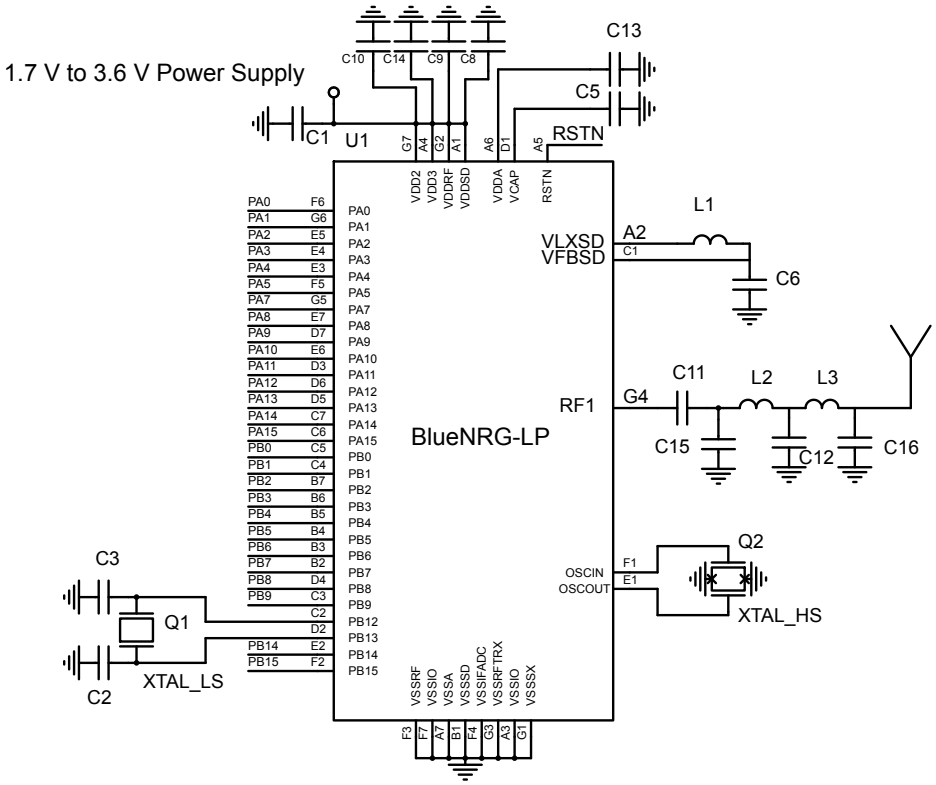


Figure 13. **Application circuit: DC-DC converter, QFN32 package**

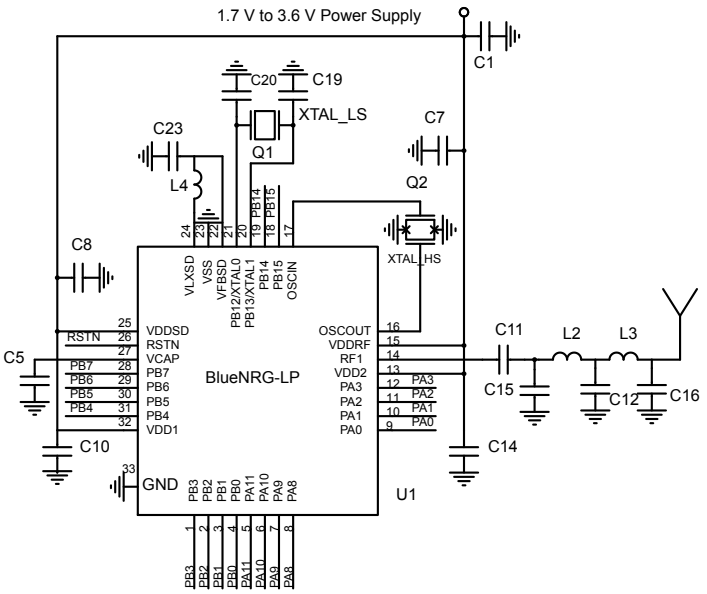


Table 7. Application circuit external components

Component	Description
C1	Decoupling capacitor
C2	32 kHz crystal loading capacitor
C3	32 kHz crystal loading capacitor
C4	Decoupling capacitor
C5	Decoupling capacitor for digital regulator
C6	DC – DC converter output capacitor
C7	Decoupling capacitor
C8	Decoupling capacitor
C9	DC-DC converter output inductor
C10	Decoupling capacitor
C11	Decoupling capacitor
C12	RF matching capacitor
C13	Decoupling capacitor
C14	Decoupling capacitor
C15	RF matching capacitor
C16	RF matching capacitor
L1	DC-DC converter output inductor
L2	RF matching inductor
L3	RF matching capacitor
Q1	Low speed crystal
Q2	High speed crystal
U1	BlueNRG-LP
U2	Low/band pass filter

Note: In order to make the board DC–DC OFF, the inductance L1 must be removed and the supply voltage must be applied to the VFBSD pin.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to ground (GND).

5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the following standard conditions:

- Ambient temperature is T_A = 25 °C
- Supply voltage is V_{DD}: 3.3 V
- System clock frequency is 32 MHz (clock source HSI)
- SMPS clock frequency is 4 MHz

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, VDD = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ± 2σ).

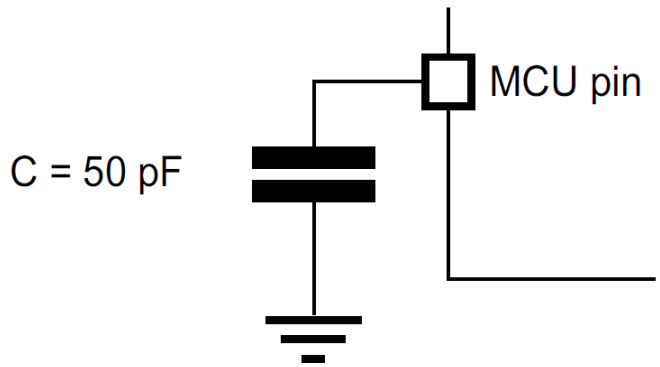
5.1.3 Typical curves

Unless otherwise specified, all typical curves are only given as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure below.

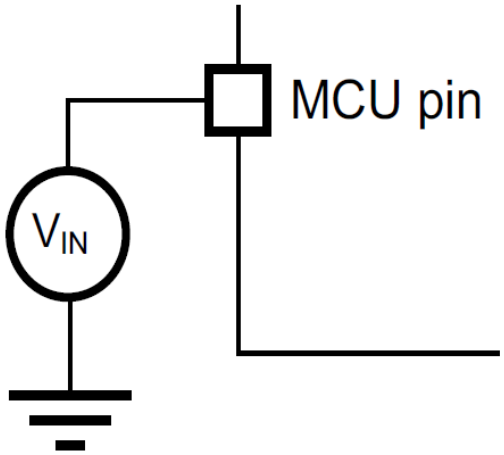
Figure 14. Pin loading conditions



5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure below.

Figure 15. **Pin input voltage**



5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in the tables below, may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Min.	Max.	Unit
VDD1, VDD2, VDD3, VDD4, VDDRF, VDDSD	DC-DC converter supply voltage input and output	-0.3	+3.9	V
VCAP, VDDA	DC voltage on linear voltage regulator	-0.3	+1.32	
PA0 to PA15, PB0 to PB4, PB6 to PB15	DC voltage on digital input/output pins	-0.3	+3.9	
VLXSD, VFBSD	DC voltage on analog pins			
XTAL0/PB12, XTAL1/PB13, OSCIN, OSCOUT, PB5	DC voltage on XTAL pins and PGA_VBIAS_MIC	-0.3	+3.6	
RF1	DC voltage on RF pin		+1.4	
$\lvert\Delta V_{DD}\rvert$	Variations between different V_{DDX} power pins of the same domain		50	mV

Note: All the main power and ground pins must always be connected to the external power supply, in the permitted range.

Table 9. Current characteristics

Symbol	Ratings	Max.	Unit
ΣIV_{DD}	Total current into sum of all VDD power lines (source)	130	mA
ΣIV_{GND}	Total current out of sum of all ground lines (sink)	130	
$IV_{DD(PIN)}$	Maximum current into each VDD power pin (source)	100	
$IV_{GND(PIN)}$	Maximum current out of each ground pin (sink)	100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	20	
	Output current sourced by any I/O and control pin	20	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins	100	
	Total output current sourced by sum of all I/Os and control pins	100	

Table 10. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-40 to -125	°C
T_J	Maximum junction temperature	125	

5.3 Operating conditions

5.3.1 Summary of main performance

Table 11. Main performance SMPS ON

Symbol	Parameter	Test conditions	Typ. VDD = 1.8 V	Typ. VDD = 3.3 V	Unit
I_{CORE}	Core current consumption	SHUTDOWN	8	19	nA
		DEEPSTOP, no timer, wake-up GPIO, RAM0 retained	0.44	0.46	µA
		DEEPSTOP, no timer, wakeup GPIO, all RAM retained	0.62	0.64	
		DEEPSTOP (32 kHz LSI), RAM0 retained	0.94	1.06	
		DEEPSTOP (32 kHz LSI), all RAMs retained	1.12	1.24	
		DEEPSTOP (32 kHz LSE), RAM0 retained	0.64	0.75	
		DEEPSTOP (32 kHz LSE), all RAM retained	0.83	0.94	
		CPU in RUN (64 MHz). Dhrystone, clock source PLL64		2719	uA
		CPU in RUN (32 MHz). Dhrystone, clock source PLL64		2188	
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64		1708	
		Radio RX at sensitivity level		3350	
		Radio TX 0 dBm output power		4300	
$I_{DYNAMIC}$	Dynamic current	Computed value: (CPU 64 MHz Dhrystone - CPU 32 MHz Dhrystone) / 32		18	µA/MHz

Table 12. Main performance SMPS bypassed

Symbol	Parameter	Test conditions	Typ. VDD = 1.8 V	Typ. VDD = 3.3 V	Unit
I_{CORE}	Core current consumption	SHUTDOWN	8	19	nA
		DEEPSTOP, no timer, wake-up GPIO, RAM0 retained	0.44	0.46	µA
		DEEPSTOP, no timer, wake-up GPIO, all RAM retained	0.62	0.64	
		DEEPSTOP (32 kHz LSI), RAM0 retained	0.94	1.06	
		DEEPSTOP (32 kHz LSI), all RAMs retained	1.12	1.24	
		DEEPSTOP (32 kHz LSE), RAM0 retained	0.64	0.75	
		DEEPSTOP (32 kHz LSE), all RAM retained	0.83	0.94	
		CPU in RUN (64 MHz). Dhrystone, clock source PLL64		4482	
		CPU in WFI (64 MHz), all peripherals off, clock source PLL64		2230	
		Radio RX at sensitivity level		6700	
		Radio TX 0 dBm output power		8900	

Table 13. Peripheral current consumption at VDD = 3.3 V, sysclk at 32 MHz, SMPS on

Parameter	Test conditions	Typ.	Unit
ADC		80	µA
DMA		39	
GPIOA		2	
GPIOB		2	
I2C1		40	
I2C2		39	
I2S2	Peripheral clock at 32 MHz	46	
I2S3	Peripheral clock at 32 MHz	47	
IWDG		11	
LPUART		52	
PKA		50	
RNG		64	

Parameter	Test conditions	Typ.	Unit
RTC		14	µA
SPI1		35	
SPI2	Peripheral clock at 16 MHz	40	
SPI3	Peripheral clock at 16 MHz	42	
Systick		8	
TIM1		248	
USART		81	
SYSCFG		33	
THSENS		301	
CRC		9	

5.3.2 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency		1	64	MHz
f_{PCLK0}	Internal APB0 clock		1	64	
f_{PCLK1}	Internal APB1 clock frequency		1	64	
f_{PCLK2}	Internal APB2 clock frequency		16	32	
V_{DD}	Standard operating voltage		1.7	3.6	V
V_{FBSMPS}	SMPS feedback voltage		1.4	3.6	
V_{DDRF}	Minimum RF voltage		1.7	3.6	
V_{IN}	I/O input voltage		-0.3	VDD+0.3	
P_D	Power dissipation at T_A=105 °C(1)	QFN48 package		30	mW
		QFN32 package			
T_A	Ambient temperature	Maximum power dissipation	-40	105	°C
T_J	Junction temperature range		-40	105	

1. *T_A cannot exceed the T_J max.*

5.3.3 RF general characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 15. Bluetooth Low Energy RF general characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
F_{RANGE}	Frequency range(1)		2400		2483.5	MHz
RF_{CH}	RF channel center frequency(1)		2402		2480	
PLL_{RES}	RF channel spacing(1)			2		MHz
ΔF	Frequency deviation(1)			250		kHz

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Δf1	Frequency deviation average(1)		450		550	kHz
C_{Fdev}	Center frequency deviation(1)	During the packet and including both initial frequency offset and drift			±150	kHz
Δfa	Frequency deviation Δf2 (average) / Δf1 (average)(1)		0.80			
R_{gfsk}	On-air data rate(1)		1		2	Mbps
STacc	Symbol time accuracy(1)				±50	ppm
MOD	Modulation scheme			GFSK		
BT	Bandwidth-bit period product			0.5		
Mindex	Modulation index(1)		0.45	0.5	0.55	
PMAX	Maximum output	At antenna connector, VSMPS = 1.9 V, LDO code		+8		dBm
PMIN	Minimum output	At antenna connector		-20		dBm
PRFC	RF power accuracy	@ 27 °C		±1.5		dB
		All temperatures		±2.5		

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

5.3.4 RF transmitter characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 16. Bluetooth Low Energy RF transmitter characteristics at 1 Mbps not coded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW1M}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	500			kHz
P_{RF1}, 1 Ms/s	In-band emission at ±2 MHz(1)	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
P_{RF2}, 1 Ms/s	In-band emission at ±[3+n]MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector			-30	dBm
PS_{PUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=2,3,4..k	-50		+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23		+23	kHz
$Int_{Freqdrift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20		+20	kHz
Drift Rate max	Maximum drift rate(1)	Between any two 10-bit groups separated by 50 µs	-20		+20	kHz/50 µs
Z_{RF1}	Optimum RF load (impedance at RF1 pin)	@ 2440 MHz		40		Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

Table 17. Bluetooth Low Energy RF transmitter characteristics at 2 Mbps not coded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW1M}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	670			kHz
P_{RF1}, 2 Ms/s	In-band emission at ±4 MHz(1)	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
P_{RF2}, 2 Ms/s	In-band emission at±5 MHz(1)	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
P_{RF3}, 2 Ms/s	In-band emission at ±[6+n]MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector			-30	dBm
P_{SPUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=2,3,4..k	-50		+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #1 – integration interval #0	-23		+23	kHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-5), where n=6,7,8..k	-20		+20	kHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 20-bit groups separated by 50 µs	-20		+20	kHz/50µs
Z_{RF1}	Optimum RF load (impedance at RF1 pin)	@ 2440 MHz		40		Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

Table 18. Bluetooth Low Energy RF transmitter characteristics at 1 Mbps LE coded (S=8)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{BW}	6 dB bandwidth for modulated carrier	Using resolution bandwidth of 100 kHz	500			kHz
$P_{RF1, LE}$ coded	In-band emission at ±2 MHz(1)	Using resolution bandwidth of 100 kHz and average detector			-20	dBm
$P_{RF2, LE}$ coded	In-band emission at ±[3+n] MHz, where n=0,1,2..(1)	Using resolution bandwidth of 100 kHz and average detector			-30	dBm
PS_{PUR}	Spurious emission	Harmonics included. Using resolution bandwidth of 1 MHz and average detector			-41	dBm
$Freq_{drift}$	Frequency drift(1)	Integration interval #n – integration interval #0, where n=1,2,3..k	-50		+50	kHz
$IFreq_{drift}$	Initial carrier frequency drift(1)	Integration interval #3 – integration interval #0	-19.2		+19.2	kHz
$IntFreq_{drift}$	Intermediate carrier frequency drift(1)	Integration interval #n – integration interval #(n-3), where n=7,8,9..k	-19.2		+19.2	kHz
$DriftRate_{max}$	Maximum drift rate(1)	Between any two 16-bit groups separated by 48 µs	-19.2		+19.2	kHz/48 µs
Z_{RF1}	Optimum RF load (Impedance at RF1 pin)	@ 2440 MHz		40		Ω

1. *Tested according to Bluetooth SIG radio frequency physical layer (RF PHY) test suite (not tested in production).*

5.3.5 RF receiver characteristics

All performance data are referred to a 50 Ω antenna connector, via reference design.

Table 19. Bluetooth Low Energy RF receiver characteristics at 1 Msym/s uncoded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-97		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal = -67 dBm, PER < 30.8%		8		dBc
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -67 dBm, PER < 30.8%		-1		dBc
$C/I_{2\ MHz}$	Adjacent Interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -67 dBm, PER < 30.8%		-35		dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -67 dBm, PER < 30.8%		-47		dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -67 dBm, PER < 30.8%		-25		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal= -67 dBm, PER < 30.8%		-25		dBc
Out of band blocking (interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30 MHz – 2000 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 10 MHz		5		dBm
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 3 MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal = -67 dBm, PER < 30.8%, measurement resolution 25 MHz		10		dBm
Intermodulation characteristics (CW signal at f_1, BLE interfering signal at f_2)						
P_IM(3)	Input power of IM interferer at 3 and 6 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%		-27		dBm
P_IM(-3)	Input power of IM interferer at -3 and -6 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%		-40		dBm
P_IM(4)	Input power of IM interferer at ±4 and ±8 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%		-32		dBm
P_IM(5)	Input power of IM interferer at ±5 and ±10 MHz distance from wanted signal	Wanted signal = -64 dBm, PER < 30.8%		-32		dBm

Table 20. Bluetooth Low Energy RF receiver characteristics at 2 Msym/s uncoded

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%		-94		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source	@ 2440 MHz		40		Ω

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	(impedance at RF1 pin)					
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal= -67 dBm, PER < 30.8%		8		dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -67 dBm, PER < 30.8%		-14		dBc
$C/I_{4\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 4$ MHz	Wanted signal = -67 dBm, PER < 30.8%		-41		dBc
$C/I_{6\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (6+2n)$ MHz [n = 0,1,2…]	Wanted signal = -67 dBm, PER < 30.8%		-45		dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image\text{-}2M}$	Wanted signal = -67 dBm, PER < 30.8%		-25		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel-to-image frequency $f_{interference} = f_{image\text{-}2M} \pm 2$ MHz	Wanted signal= -67 dBm, PER < 30.8%		-14		dBc
Out of band blocking (interfering signal CW)						
C/I_{Block}	Interfering signal frequency 30 MHz – 2000 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 10 MHz		5		dBm
C/I_{Block}	Interfering signal frequency 2003 MHz – 2399 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 2484 MHz – 2997 MHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 3 MHz		-5		dBm
C/I_{Block}	Interfering signal frequency 3000 MHz – 12.75 GHz	Wanted signal= -67 dBm, PER < 30.8%, measurement resolution 25 MHz		10		dBm
Intermodulation characteristics (CW signal at f_1, BLE interfering signal at f_2)						
P_IM(6)	Input power of IM interferer at 6 and 12 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%		-27		dBm
P_IM(-6)	Input power of IM interferer at -6 and -12 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%		-30		dBm
P_IM(8)	Input power of IM interferer at ±8 and ±16 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%		-30		dBm
P_IM(10)	Input power of IM interferer at ±10 and ±20 MHz distance from wanted signal	Wanted signal= -64 dBm, PER < 30.8%		-28		dBm

Table 21. Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=2)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-100		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
C/I_{CO}-channel	Co-channel interference	Wanted signal = -79 dBm, PER < 30.8%		2		dBc

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	$f_{RX} = f_{interference}$					
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-5		dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-38		dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -79 dBm, PER < 30.8%		-50		dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -79 dBm, PER < 30.8%		-30		dBc
$C/I_{Image\pm1\ MHz}$	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-34		dBc

Table 22. Bluetooth Low Energy RF receiver characteristics at 1 Msym/s LE coded (S=8)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
RX_{SENS}	Sensitivity	PER < 30.8%	-	-104		dBm
P_{SAT}	Saturation	PER < 30.8%		8		dBm
Z_{RF1}	Optimum RF source (impedance at RF1 pin)	@ 2440 MHz		40		Ω
RF selectivity with BLE equal modulation on interfering signal						
$C/I_{CO\text{-}channel}$	Co-channel interference $f_{RX} = f_{interference}$	Wanted signal = -79 dBm, PER < 30.8%		1		dBc
$C/I_{1\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 1$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-4		dBc
$C/I_{2\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm 2$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-39		dBc
$C/I_{3\ MHz}$	Adjacent interference $f_{interference} = f_{RX} \pm (3+n)$ MHz [n = 0,1,2…]	Wanted signal = -79 dBm, PER < 30.8%		-53		dBc
C/I_{Image}	Image frequency interference $f_{interference} = f_{image}$	Wanted signal = -79 dBm, PER < 30.8%		-33		dBc
$C/I_{Image} \pm 1$ MHz	Adjacent channel-to-image frequency $f_{interference} = f_{image} \pm 1$ MHz	Wanted signal = -79 dBm, PER < 30.8%		-32		dBc

5.3.6 Embedded reset and power control block characteristics

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
TRSTTEMPO	Reset temporization after PDR is detected	VDD rising			500	us
VPDR	Power-down reset threshold			1.63		V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
VPVD0	PVD threshold 0	Falling edge		2.02		V
VPVD1	PVD threshold 1	Falling edge		2.17		
VPVD2	PVD threshold 2	Falling edge		2.33		
VPVD3	PVD threshold 3	Falling edge		2.49		
VPVD4	PVD threshold 4	Falling edge		2.61		
VPVD5	PVD threshold 5	Falling edge		2.78		
VPVD6	PVD threshold 6	Falling edge		2.87		

5.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as: the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is put under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

Table 24. Current consumption

Symbol	Parameter	Conditions	Typ.			Unit
			25 °C	85 °C	105 °C	
I_{DD}(RUN)	Supply current in RUN mode	f_{HCLK} = 64 MHz All peripherals disabled	2.40	2.49	2.54	mA
		f_{HCLK} = 32 MHz All peripherals disabled	1.98	2.03	2.08	
		f_{HCLK} = 16 MHz All peripherals disabled	1.62	1.67	1.71	
I_{DD}(DEEPSTOP)	Supply current in DEEPSTOP(1)	Timer OFF	0.65	6.73	15.73	µA
		Timer source LSI	1.25	7.41	16.46	
		Timer source LSI RTC ON	1.30	7.56	16.70	
		Timer source LSI IWDG ON	1.27	7.47	16.55	
		Timer source LSI RTC and IWDG ON	1.33	7.61	16.79	
		Timer source LSE	1.00	7.16	16.22	
		Timer source LSE RTC ON	1.06	7.31	16.45	
		Timer source LSE IWDG ON	1.02	7.22	16.30	
		Timer source LSE RTC and IWDG ON	1.07	7.36	16.54	

Symbol	Parameter	Conditions	Typ.			Unit
			25 °C	85 °C	105 °C	
I_{DD}(SHUTDOWN)	Supply current in SHUTDOWN		0.02	0.46	1.36	µA
I_{DD}(RST)	Current under reset condition		1.34	1.45	1.55	mA

1. *The current consumption in DEEPSTOP is measured considering the entire SRAM retained.*

5.3.8 Wake-up time from low power modes

The wake-up times reported are the latency between the event and the execution of the instruction. The device goes to low-power mode after WFI (wait for interrupt) instructions.

Table 25. Low power mode wake-up timing

Symbol	Parameter	Conditions	Typ.	Unit
$T_{WUDEEPSTOP}$	Wake-up time from DEEPSTOP mode to RUN mode	Wake-up from GPIO VDD = 3.3 V Flash memory	110	µs

5.3.9 High speed crystal requirements

The high speed external oscillator must be supplied with an external 32 MHz crystal that is specified for a 6 to 8 pF loading capacitor. The BlueNRG-LP includes internal programmable capacitances that can be used to tune the crystal frequency in order to compensate the PCB parasitic one. These internal load capacitors are made by a fixed one, in parallel with a 6-bit binary weighted capacitor bank. Thanks to low CL step size (LSB is typically 0.07 pF), very fine crystal tuning is possible. With a typical XTAL sensitivity of -14 ppm/pF, it is possible to trim a 32 MHz crystal, with a resolution of 1 ppm.

The requirements for the external 32 MHz crystal are reported in the table below.

Table 26. HSE crystal requirements

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Oscillator frequency			32		MHz
f_{TOL}	Frequency tolerance	Includes initial accuracy, stability over temperature, aging and frequency pulling due to incorrect load capacitance			±50	ppm
ESR	Equivalent series resistance				100	Ω
P_D	Drive level				100	µW
CL	HSE crystal load capacitance	27 °C, typical corner GMCONF = 3	5 (1)	7(2)	9.2(3)	pF
CLstep	HSE crystal load capacitance LSB value	27 °C, GMCONF = 3 XOTUNE code between 32 and 33		0.07		pF

1. *XOTUNE programed at minimum code = 0*
2. *XOTUNE programed at center code = 32*
3. *XOTUNE programed at maximum code = 63*

5.3.10 Low speed crystal requirements

Low speed clock can be supplied with an external 32.768 kHz crystal oscillator. Requirements for the external 32.768 kHz crystal are reported in the table below.

Table 27. **LSE crystal requirements**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency			32.768		kHz
ESR	Equivalent series resistance				90	kΩ
P_D	Drive level				0.1	µW

5.3.11 High speed ring oscillator characteristics

Table 28. **HSI oscillator characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency			64		MHz

5.3.12 Low speed ring oscillator characteristics

Table 29. **LSI oscillator characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{NOM}	Nominal frequency			33		kHz
$\Delta F_{RO\_\Delta T}/F_{RO}$	Frequency spread vs. temperature	Standard deviation		140		ppm/°C

5.3.13 PLL characteristics

Characteristics measured over recommended operating conditions unless otherwise specified.

Table 30. **PLL characteristics**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PN_{SYNTH}	RF carrier phase noise	At ±1 MHz offset from carrier (measured at 2.4 GHz)		-110		dBc/Hz
		At 2.4 GHz ±3 MHz offset from carrier (measured at 2.4 GHz)		-114		dBc/Hz
		At 2.4 GHz±6 MHz offset from carrier (measured at 2.4 GHz)		-128		dBc/Hz
		At ±25 MHz offset from carrier		-135		dBc/Hz
$LOCK_{TIMETX}$	PLL lock time to TX	With calibration @2.5 ppm		150		µs
$LOCK_{TIMERX}$	PLL lock time to RX	With calibration @2.5 ppm		110		µs
$LOCK_{TIMERXTX}$	PLL lock time RX to TX	Without calibration @2.5 ppm		47		µs
$LOCK_{TIMETXRX}$	PLL lock time TX to RX	Without calibration @2.5 ppm		32		µs

5.3.14 Flash memory characteristics

The characteristics below are guaranteed by design.

Table 31. Flash memory characteristics

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
t_{prog}	32-bit programming time		20	40	µs
t_{prog_burst}	4x32-bit burst programming time		20	40	
t_{ERASE}	Page (2 kbyte) erase time		20	40	ms
t_{ME}	Mass erase time		20	40	
I_{DD}	Average consumption from VDD	Write mode	3		mA
		Erase mode	3		
		Mass erase	5		

Table 32. Flash memory endurance and data retention

Symbol	Parameter	Test conditions	Min.	Unit
N_{END}	Endurance	T_A = -40 to +105 °C	10	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	Years

5.3.15 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts x (n + 1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 33. ESD absolute maximum ratings

Symbol	Parameter	Conditions	Class	Max.(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	Conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CBM)}$	Electrostatic discharge voltage (charge device model)	Conforming to ANSI/ESDA/STM5.3.1 JS-002	C2a	500	

1. *Guaranteed by design.*

5.3.16 I/O port characteristics

Unless otherwise specified, the parameters given in the tables below are derived from tests performed under the conditions summarized in Section 5.3.2 General operating conditions. All I/Os are designed as CMOS-compliant. The characteristics below are guaranteed by characterization.

Table 34. I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	1.62 V < VDD < 3.6 V			0.3 x VDD	V
V_{IH}	I/O input high level voltage		0.7 x VDD			
I_{lkg}	Input leakage current	0 <= VIN <= Max(VDDx)(1)			+/-100	nA
		Max(VDDx)(1) <= VIN <= Max(VDDx)(1) +1 V			650	
		Max(VDDx)(1) + 1 V < VIN <= 5.5 V			200	
R_{PU}	Pull-up resistor	VIN = GND	25	40	55	kΩ
R_{PD}	Pull-down resistor	VIN = VDD	25	40	55	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C_{IO}	I/O pin capacitance			5		pF

1. *Max(VDDx) is the maximum value among all the I/O supplies.*

All I/Os are CMOS-compliant (no software configuration required).

GPIOs (general purpose input/outputs) can sink or source up to ±8 mA and sink or source up to ± 20 mA (with a relaxed V_{OL} / V_{OH}).

In the user application, the number of I/O pins that can drive current must be limited to respect the absolute maximum rating specified.

- The sum of currents sourced by all I/Os on VDD, plus the maximum consumption of MCU sourced on VDD, cannot exceed the absolute maximum rating ΣIVDD
- The sum of currents sunk by all I/Os on VSS, plus the maximum consumption of the MCU sunk on GND, cannot exceed the absolute maximum rating ΣIVGND

The characteristics below are guaranteed by characterization.

Table 35. Output voltage characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OL}	Output low level voltage for I/O pin	CMOS port(1) |IIO| = 8 mA VDD ≥ 2.7 V		0.4	V
V_{OH}	Output high level voltage for I/O pin		VDD -0.4		
V_{OL}	Output low level voltage for I/O pin	|IIO| = 20 mA VDD ≥ 2.7 V		1.3	
V_{OH}	Output high level voltage for I/O pin		VDD -1.3		
V_{OL}	Output low level voltage for I/O pin	|IIO| = 4 mA VDD ≥ 1.62 V		0.4	
V_{OH}	Output high level voltage for I/O pin		VDD-0.45		

1. *CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.*

5.3.17 RSTN pin characteristics

The RSTN pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, RPU.

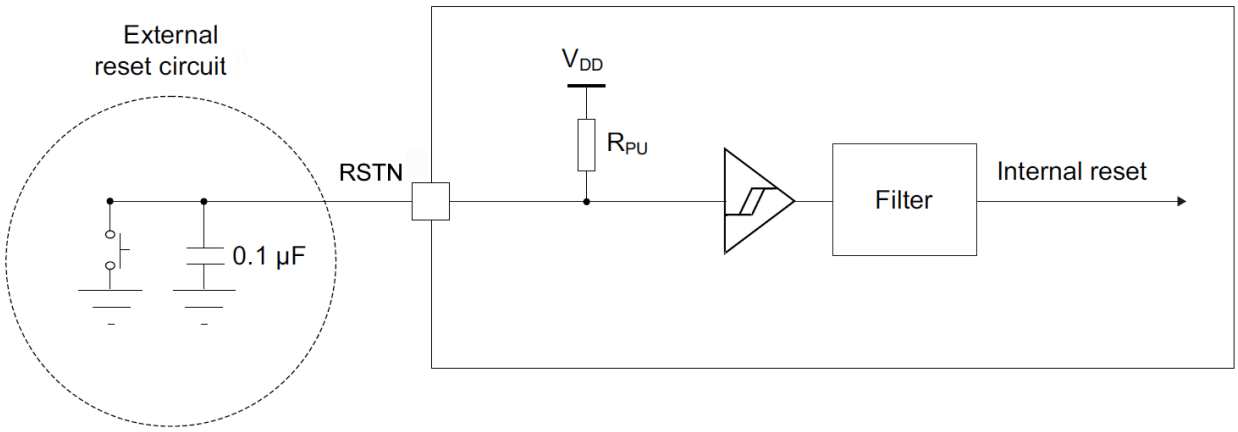
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Section 5.3.2 General operating conditions.

The characteristics below are guaranteed by design.

Table 36. RSTN pin characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
$V_{IL(RSTN)}$	RSTN input low level voltage				0.3 x VDD	V
$V_{IH(RSTN)}$	RSTN input high level voltage		0.7 x VDD			
$V_{hys(RSTN)}$	RSTN Schmitt trigger voltage hysteresis			200		mV
RPU	Weak pull-up equivalent resistor	VIN=GND	25	40	55	kΩ

Figure 16. **Recommended RSTN pin protection**



Note: The external reset circuit protects the device against parasitic resets.
The user must ensure that the level on the RSTN pin can go below the V_{IL}(RSTN) max. level specified in the table, otherwise the reset is not taken into account by the device. The external capacitor on RSTN must be placed as close as possible to the device.

5.3.18 ADC characteristics

Table 37. **ADC characteristics (HSI must be set to PLL mode)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
Ch_diff_num	Number of channels for differential mode	QFN48, WLCSP49			4	
Ch_se_num	Number of channels for single ended mode	QFN48, WLCSP49			8	
$IBAT_{ADCBIAS}$	ADC biasing consumption at battery	Biasing blocks turned on		145		mA
$IBAT_{ADCACTIVE}$	ADC active consumption at battery	ADC activated in differential mode		185		mA
VDDA	Analog supply voltage		1.2		1.32	V
R_{AIN}	Input impedance	In DC		250		kΩ
R_{in}	Internal access resistance	VBOOST is enabled for VDD < 2.7 V			550	Ω
C_{in}	Input sampling capacitor			4		pF
T_s	Sampling period			1		µs
T_{sw}	Sampling time			125		ns
DR	Output data rate			200		k samples/s
$FRMT_{output}$	Output data format			16		bits
TL	Latency time	200 kSps		5		µs
$T_{STARTUP}$	Start-up time	From ADC enable to conversion start			1	µs
DNL	Differential non-linearity			±0.7		LSB

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Units
INL	Integral non-linearity			±1		LSB
SNR Diff	Signal to noise ratio	Differential input @1 kHz, -1 dBFs		72		dB
STHD Diff	Signal to THD ratio (10 harmonics)	Differential input @1 kHz, -1 dBFs		80		dB
ENOB Diff	Effective number of bits	Differential input @1 kHz, -1 dBFs		11.5		bits
SNR SE	Signal-to-noise ratio	Single ended @1 kHz, -1 dBFs		70		dB
STHD SE	Signal-to THD ratio (10 harmonics)	Single ended @1 kHz, -1 dBFs		75		dB
ENOB SE	Effective number of bits	Single ended @1 kHz, -1 dBFs		11		bits
	ADC_ERR_1V7	Absolute error when used for battery measurements at 1.7 V, 2.4 V, 3.0 V, 3.6 V		13		mV
	ADC_ERR_2V4			0		
	ADC_ERR_3V0			-9		
	ADC_ERR_3V6			-22		

5.3.19 Temperature sensor characteristics

Table 38. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{rERR}	Error in temperature		±4		°C
T_{SLOPE}	Average temperature coefficient		8		LSB/°C
T_{ICC}	Current consumption		415		µA
T_{TS-OUT}	Output code at 30 °C (+/-5 °C)		2533		LSB

5.3.20 Timer characteristics

The characteristics below are guaranteed by design.

Table 39. TIM1 characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{res(TIM)}$	Timer resolution time	$f_{TIMxCLK}$ = 64 MHz		15.625		ns
R_{esTIM}	Timer resolution			16		bit
$t_{COUNTER}$	16-bit counter clock period	$f_{TIMxCLK}$ = 64 MHz	0.015625		1024	µs
t_{MAX_COUNT}	Maximum possible count time	$f_{TIMxCLK}$= 64			67.10	s

Table 40. **IWDG min./max. timeout period at 32 kHz (LSE)**

Prescaler divider	PR[2:0] bits	Min. timeout RL[11:0] = 0x000	Max. timeout RL[11:0] = 0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 or 7	8.0	32768	

5.3.21 I²C interface characteristics

The I²C interface meets the timing requirements of the I²C-Bus specifications and user manual rev. 03 for:

- Standard-mode (Sm): bit rate up to 100 kbit/s
- Fast-mode (Fm): bit rate up to 400 kbit/s
- Fast-mode plus (Fm+): bit rate up to 1 Mbit/s

SDA and SCL I/O requirements are met with the following restrictions: SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present. The 20 mA output drive requirement in fast-mode plus is supported partially.

This limits the maximum load C_{load} supported in fast-mode plus, given by these formulas:

- $t_r(SDA/SCL) = 0.8473 \times R_p \times C_{load}$
- $R_p(min.) = [V_{DD} - V_{OL}(max)] / I_{OL}(max)$

where R_p is the I²C lines pull-up.

All I²C SDA and SCL I/Os embed an analog filter.

The characteristics below are guaranteed by design.

Table 41. I²C analog filter characteristics

Symbol	Parameter	Min.	Max.	Unit
tAF	Maximum pulse width of spikes that are suppressed by the analog filter	50	110	ns

5.3.22 SPI characteristics

The parameters for SPI are derived from tests performed according to f_{PCLKx} frequency and supply voltage conditions.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

The characteristics below are guaranteed by design.

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCK}	SPI clock frequency	Master mode		-	32	MHz
		Slave mode			32(1)	
tsu(NSS)	NSS setup time		4 / f_{PCLK}	-	-	-
th(NSS)	NSS hold time		2 / f_{PCLK}	-	-	-
tw(SCKH)	SCK high and low time	Master mode	1 / f_{PCLK} - 1.5	1 / f_{PCLK}	1 / f_{PCLK}+1	ns
tw(SCKL)			1 / f_{PCLK}- 1.5	1 / f_{PCLK}	1 / f_{PCLK}+1	
tsu(MI)	Data input set-up time	Master mode	1	-	-	
tsu(SI)	Data input set-up time	Slave mode	1	-	-	
th(MI)	Data input hold time	Master mode	3	-	-	
th(SI)	Data input hold time	Slave mode	1	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	5	-	40	
$t_{dis(SO)}$	Data output disable time	Slave mode	5	-	38	
$t_{v(MO)}$	Data output valid time	Master mode	-	2	8	
$t_{v(SO)}$		Slave mode	-	12	39	

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$t_{h(MO)}$	Data output hold time	Master mode	2		-	ns
$t_{h(SO)}$		Slave mode	4			

1. *The maximum frequency in slave transmitter mode is determined by the sum of tv(SO) and tsu(MI), which has to fit SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having tsu(MI) = 0 while duty(SCK) = 50 %.*

Figure 17. SPI timing diagram - slave mode and CPHA = 0

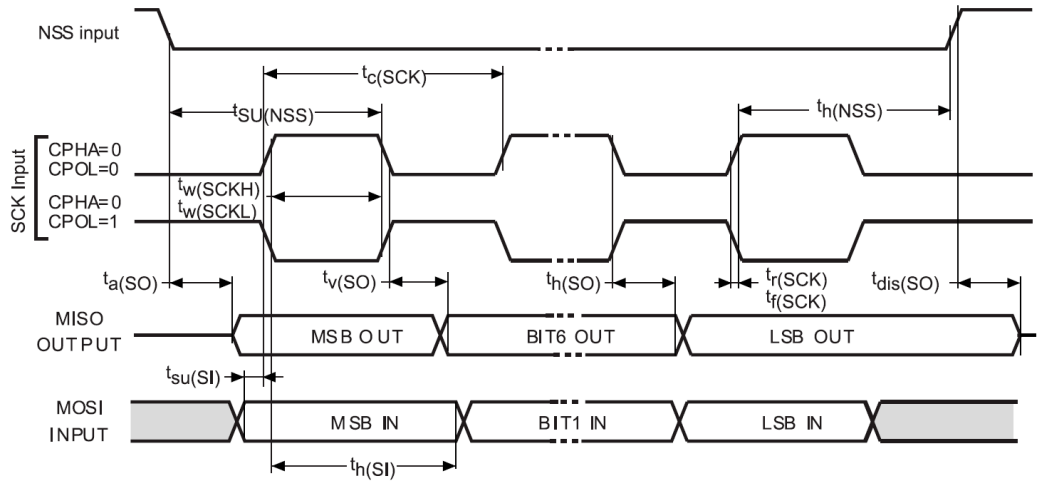


Figure 18. SPI timing diagram - slave mode and CPHA = 1

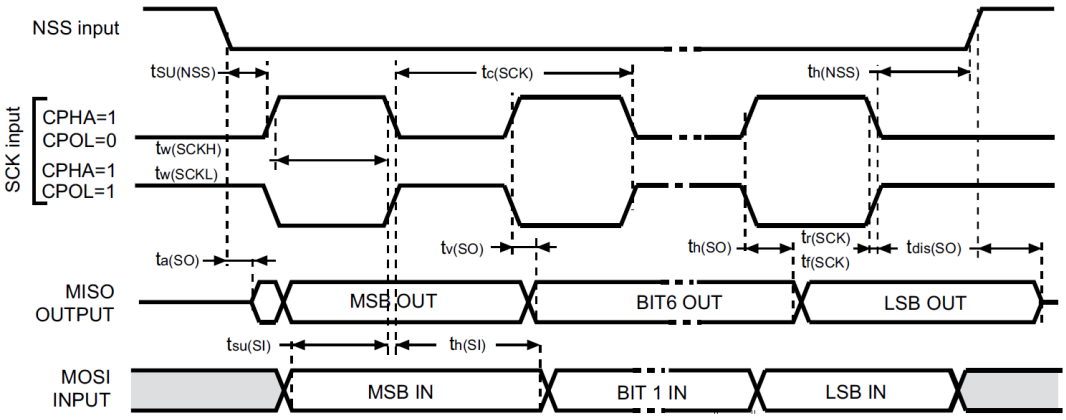
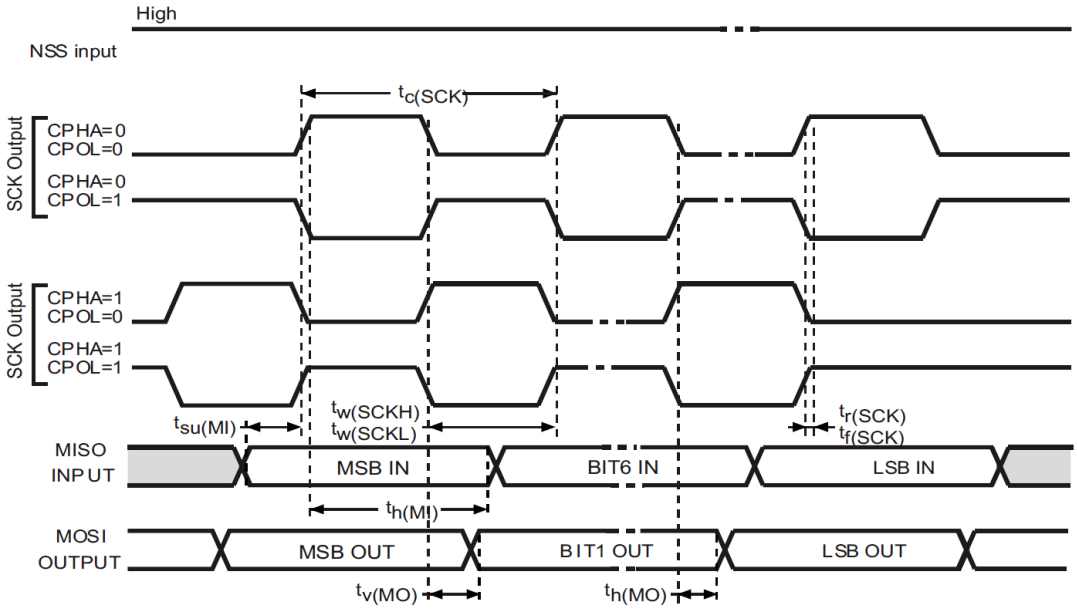


Figure 19. **SPI timing diagram - master mode**



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 QFN48 (6x6x0.9, pitch 0.4 mm) package information

Figure 20. QFN48 (6x6x0.9, pitch 0.4 mm) package outline

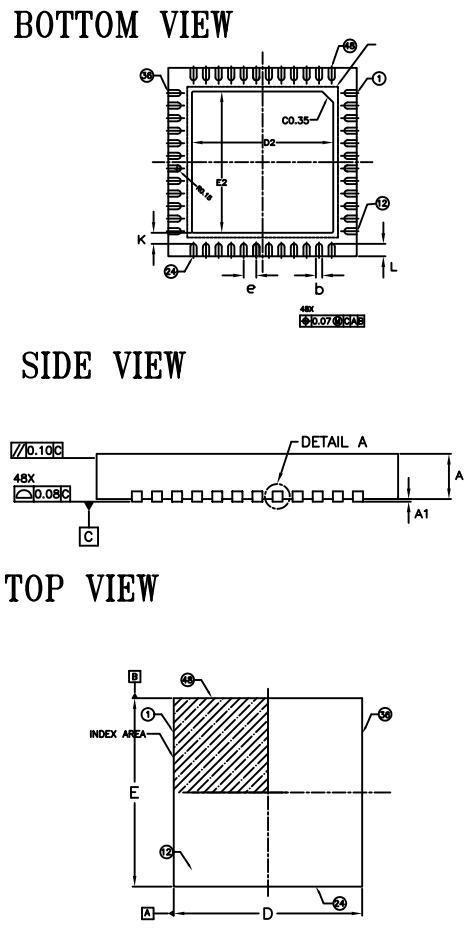


Table 43. QFN48 (6x6x0.9, pitch 0.4 mm) mechanical data

Symbol	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0.0		0.05
A3		0.20 Ref	
b	0.17	0.20	0.25
D	5.95	6.00	6.05
D2	4.40	4.50	4.60
e		0.40 BSC	
E	5.95	6.00	6.05
E2	4.40	4.50	4.60
L	0.30	0.40	0.50
K		0.50	

Table 44. Tolerance of form and position

Symbol	Databook
aaa	0.10
bbb	0.10
ccc	0.008
ddd	0.10

Figure 21. QFN48 (6x6x0.9, pitch 0.4 mm) detail A package information

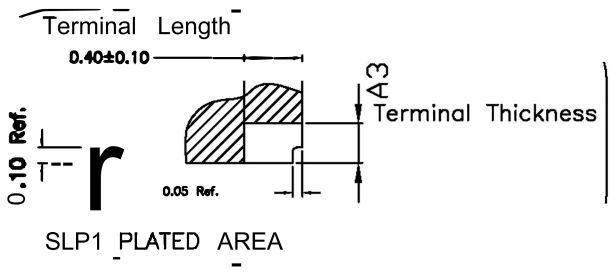
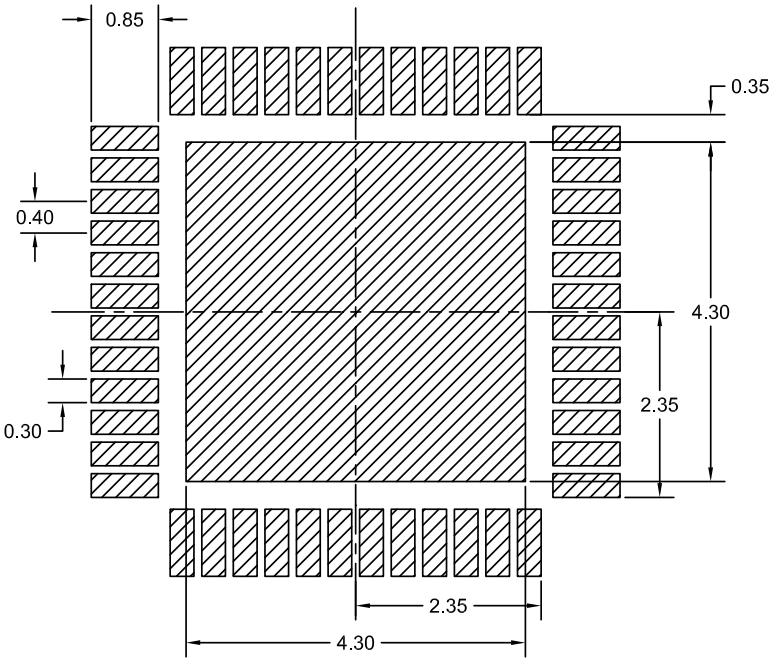


Figure 22. **QFN48 (6x6x0.9, pitch 0.4 mm) recommended footprint**



6.2 QFN32 (5x5x0.9, pitch 0.5 mm) package information

Figure 23. **QFN32 (5x5x0.9, pitch 0.5 mm) package outline**

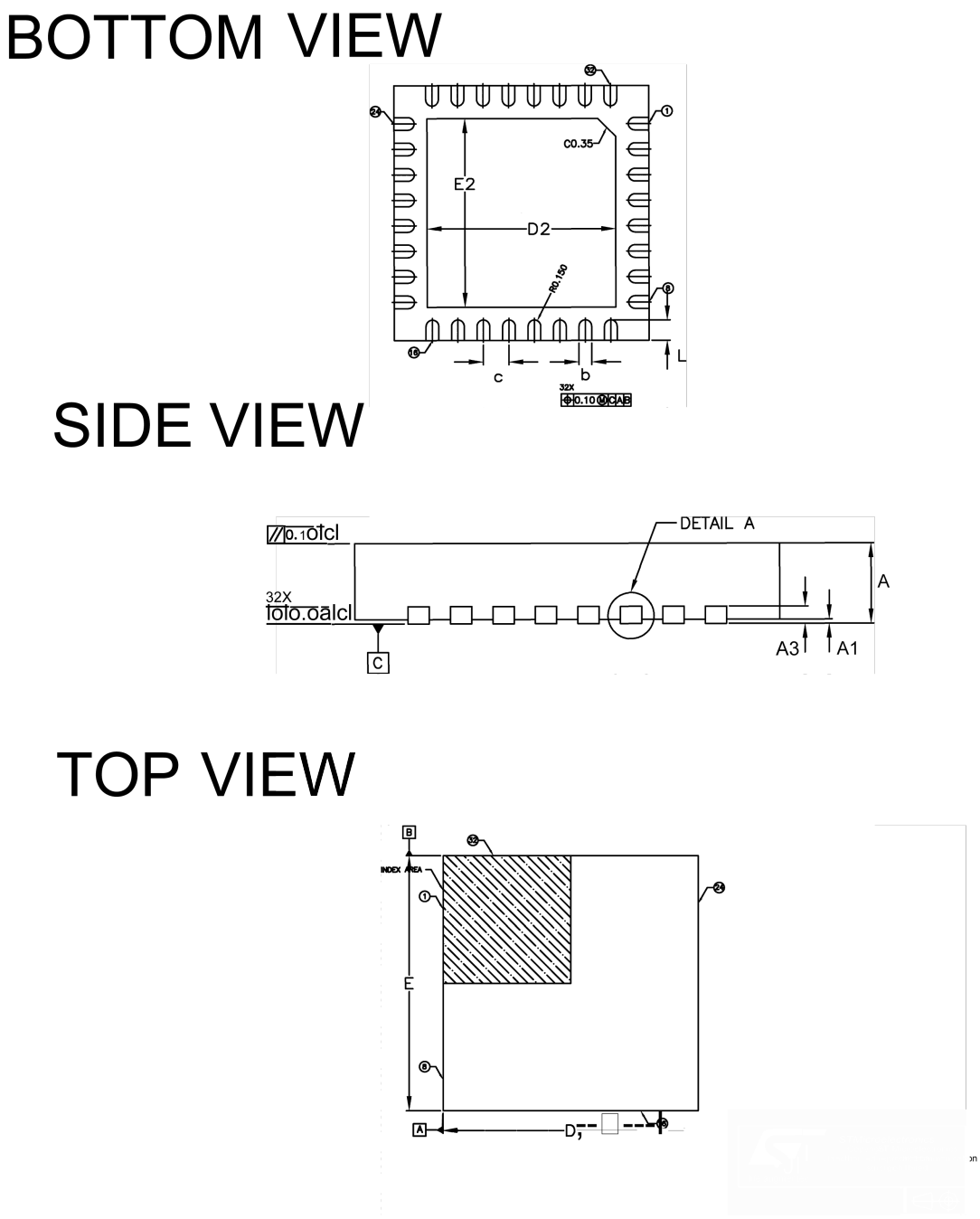


Table 45. **QFN32 (5x5x0.9, pitch 0.5 mm) package information mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0		0.05
A3		0.20	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
c		0.50 BSC	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.40	0.50

Note: D and E, package outline exclusive of any mold flashes dimensions and metal burrs.

Table 46. **Tolerance of form and position**

Symbol	Databook
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.05

Figure 24. **Detail A**

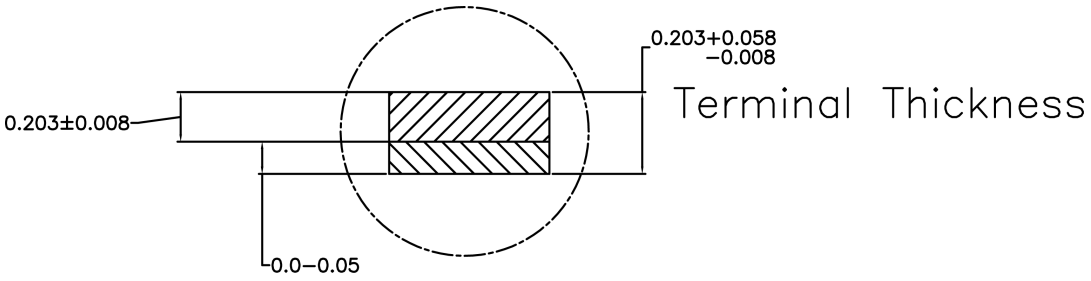
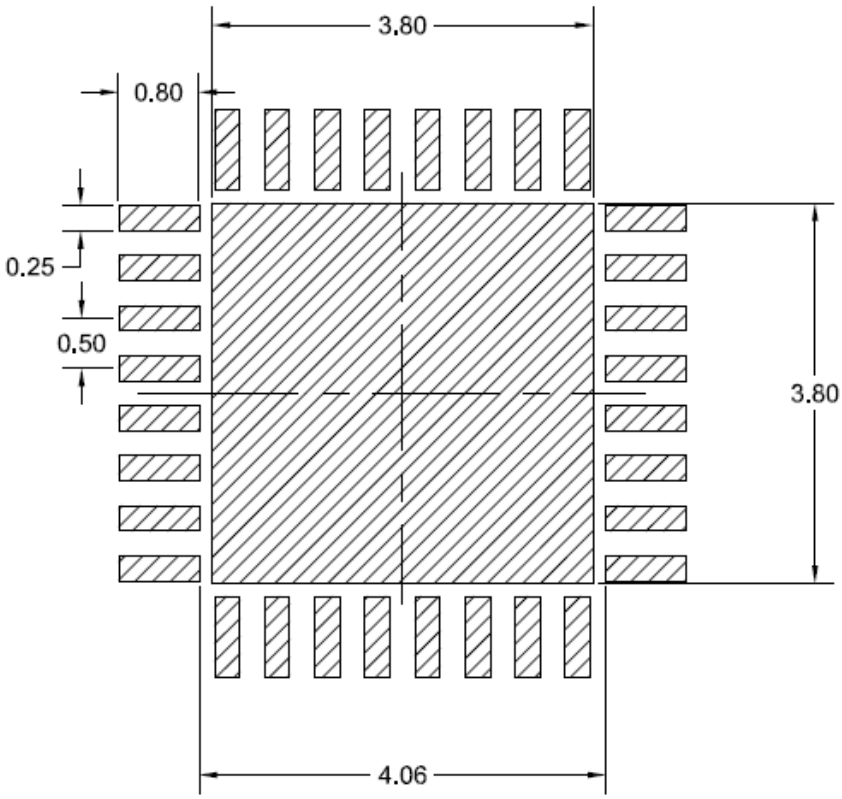


Figure 25. **QFN32 (5x5x0.9, pitch 0.5 mm) package information recommended footprint**



6.3 WLCSP49 (3.14x3.14x0.4, pitch 0.4 mm) package information

Figure 26. **WLCSP49 (3.14x3.14x0.4, pitch 0.4 mm) package outline (bumps view)**

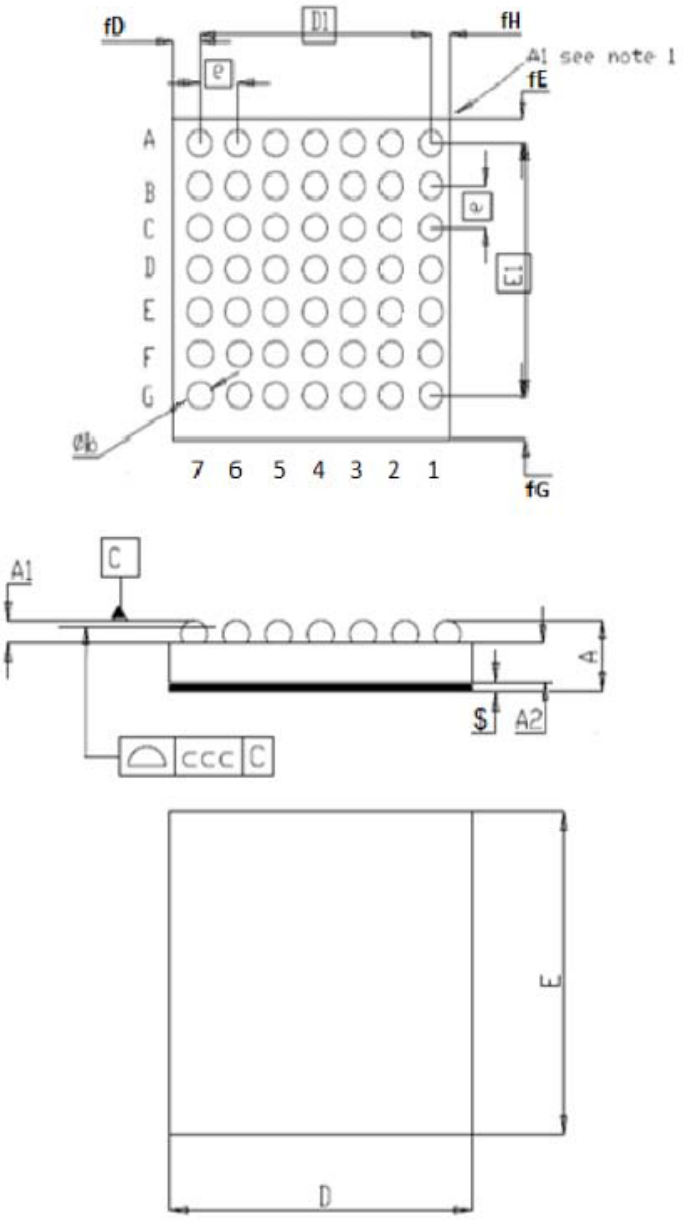
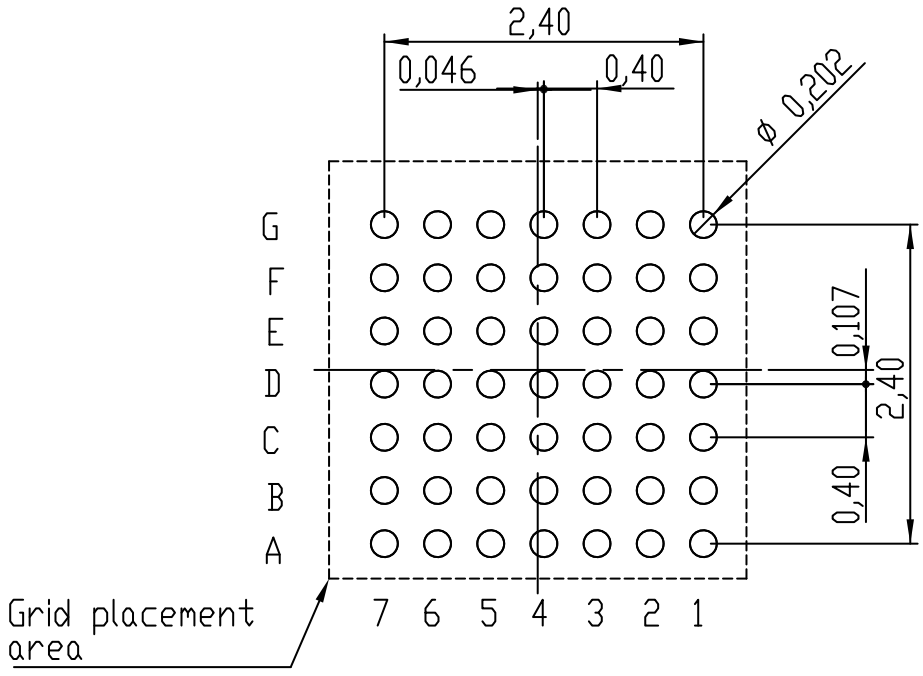


Table 47. **WLCSP49 (3.14x3.14x0.4, pitch 0.4 mm) mechanical data**

Symbol	Milimeters		
	Min.	Typ.	Max.
A	0.380	0.400	0.420
A1	0.135	0.150	0.165
A2	0.212	0.225	0.238
b	0.214	0.218	0.222
D	3.120	3.140	3.160
D1		2.400	
E	3.120	3.140	3.160
E1		2.400	
e		0.400	
fD		0.416	
fE		0.263	
fG		0.477	
fH		0.324	
$	0.022	0.025	0.028
ccc		0.060	

Figure 27. **WLCSP49 (3.14x3.14x0.4, pitch 0.4 mm) recommended footprint**



6.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax.}$) must never exceed the values in general operating conditions.

The maximum chip-junction temperature, T_J max., in degrees Celsius, can be calculated using the equation:

$$T_J\text{max.} = T_A\text{max.} + (PD\text{max} \times \theta JA) \quad (1)$$

where:

- T_A max. is the maximum ambient temperature in °C
- ΘJA is the package junction-to-ambient thermal resistance, in °C/W
- PD max. is the sum of PINT max. and PI/O max. (PD max. = PINT max. + PI/O max.)
- PINT max. is the product of IDD and VDD, expressed in Watt. This is the maximum chip internal power

PI/O max represents the maximum power dissipation on output pins:

- PI/O max. = Σ (VOL × IOL) + Σ ((VDD – VOH) × IOH)

taking into account the actual VOL / IOL and VOH / IOH of the I/Os at low and high level in the applications.

Note: When the SMPS is used, a portion of the power consumption is dissipated into the external inductor, therefore reducing the chip power dissipation. This portion depends mainly on the inductor ESR characteristics.

Note: As the radiated RF power is quite low (< 4 mW), it is not necessary to remove it from the chip power consumption.

Note: RF characteristics (such as: sensitivity, Tx power, consumption) are provided up to 85 °C.

Table 48. Package thermal characteristics

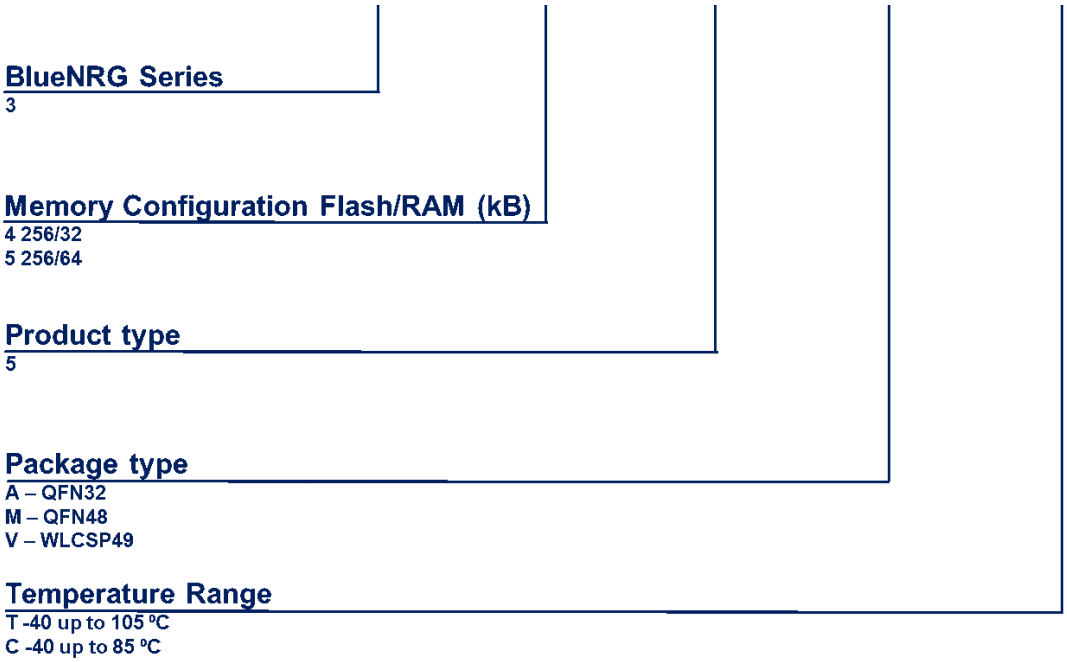
Symbol	Parameter	Value	Unit
ΘJA	Thermal resistance junction-ambient QFN48 – 6 mm x 6 mm	25.1	°C/W
	Thermal resistance junction-ambient QFN32 - 5 mm x 5 mm	26.9	
	Thermal resistance junction-ambient WCSP49 – 0.4 mm pitch	-	

7 Ordering information

Table 49. **Ordering information**

Order code	Package	Packing
BLUENRG-3x5yz	QFN32, QFN48, WLCSP49	Tape and reel

Figure 28. **Ordering information**



Revision history

Table 50. **Document revision history**

Date	Version	Changes
02-Jul-2020	1	Initial release.
24-Sep-2020	2	Updated cover page. Updated Table 3. Pin description, Table 10. Thermal characteristics, Table 14. General operating conditions and Table 49. Ordering information. Updated Figure 6. Clock tree. Added Table 4. Legend/abbreviations used in the pinout table.
01-Feb-2021	3	Updated Section Features, Section Description, Figure 4. Power supply configuration and Figure 16. Recommended RSTN pin protection.

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