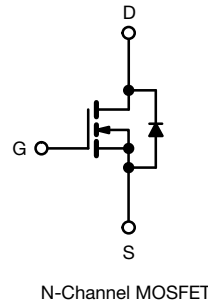
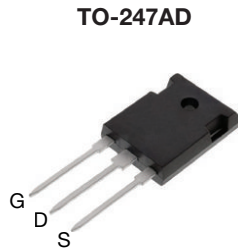


## Automotive E Series Power MOSFET with Fast Body Diode

PRODUCT SUMMARY	
$V_{DS}$ (V) at $T_J$ max.	700
$R_{DS(on)}$ typ. at 25 °C ( $\Omega$ )	$V_{GS} = 10$ V   0.045
$Q_g$ typ. (nC)	229
$Q_{gs}$ (nC)	53
$Q_{gd}$ (nC)	91
Configuration	Single



### FEATURES

- Fast body diode MOSFET using Automotive Grade E series technology
- Reduced  $t_{rr}$ ,  $Q_{rr}$ , and  $I_{RRM}$
- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Low switching losses due to reduced  $Q_{rr}$
- 175 °C operating temperature
- AEC-Q101 qualified
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### APPLICATIONS

- Automotive onboard charger
- Automotive DC/DC converter


ORDERING INFORMATION	
Package	TO-247AD
Lead (Pb)-Free and Halogen-Free	SQW61N65EF-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	$V_{DS}$	650	V
Gate-Source Voltage	$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 175$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	187	
Linear Derating Factor		4.2	W/°C
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	1323	mJ
Maximum Power Dissipation	$P_D$	625	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	°C
Drain-Source Voltage Slope	$dV/dt$	70	V/ns
Reverse Diode $dV/dt$ <sup>d</sup>		50	
Soldering Recommendations (Peak temperature) <sup>c</sup>	For 10 s	260	°C

### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$  V, starting  $T_J = 25$  °C,  $L = 73.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 6$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $di/dt = 470$  A/ $\mu$ s, starting  $T_J = 25$  °C

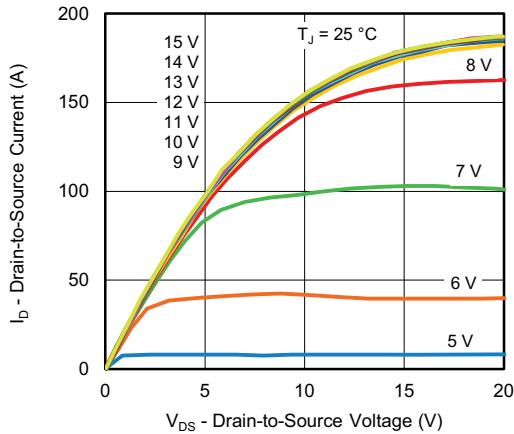
THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	40	°C/W
Maximum Junction-to-Case (Drain)	$R_{thJC}$	0.24	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	650	-	-	V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 30\text{ mA}$	-	0.77	-	V/°C	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V	
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 100$	nA	
		$V_{GS} = \pm 30\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$	
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}$	-	0.045	0.052	$\Omega$	
Forward Transconductance	$g_{fs}$	$V_{DS} = 30\text{ V}, I_D = 32\text{ A}$	-	28	-	S	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 100\text{ V}, f = 1\text{ MHz}$	-	7379	-	pF	
Output Capacitance	$C_{oss}$		-	310	-		
Reverse Transfer Capacitance	$C_{rss}$		-	4	-		
Effective Output Capacitance, Energy Related <sup>a</sup>	$C_{o(er)}$		$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$	-	213		-
Effective Output Capacitance, Time Related <sup>b</sup>	$C_{o(tr)}$			-	841		-
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}, I_D = 32\text{ A}, V_{DS} = 520\text{ V}$	-	229	344	nC	
Gate-Source Charge	$Q_{gs}$		-	53	-		
Gate-Drain Charge	$Q_{gd}$		-	91	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 32\text{ A}, V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$	-	65	98	ns	
Rise Time	$t_r$		-	107	161		
Turn-Off Delay Time	$t_{d(off)}$		-	252	378		
Fall Time	$t_f$		-	102	153		
Gate Input Resistance	$R_g$		$f = 1\text{ MHz}, \text{ open drain}$	0.5	1		2
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	62	A	
Pulsed Diode Forward Current	$I_{SM}$		-	-	187		
Diode Forward Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 32\text{ A}, V_{GS} = 0\text{ V}$	-	0.9	1.2	V	
Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 30.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$	-	204	408	ns	
Reverse Recovery Charge	$Q_{rr}$		-	1.9	3.8	$\mu\text{C}$	
Reverse Recovery Current	$I_{RRM}$		-	18	-	A	

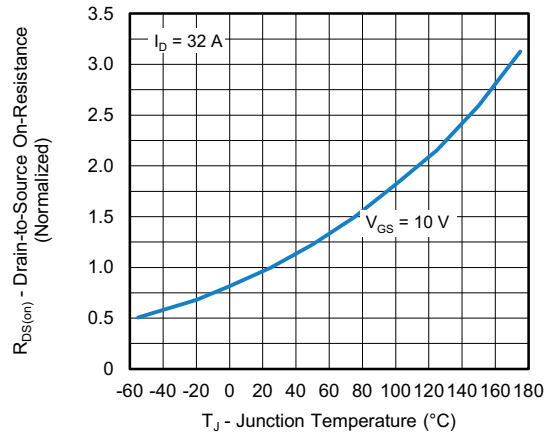
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

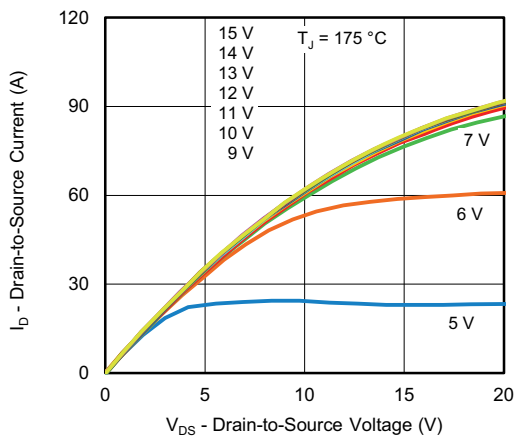
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



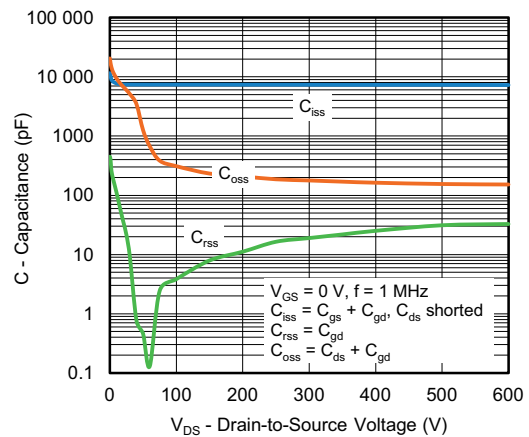
**Fig. 1 - Typical Output Characteristics**



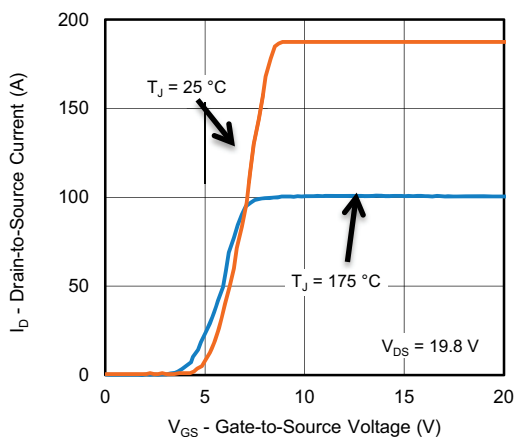
**Fig. 4 - Normalized On-Resistance vs. Temperature**



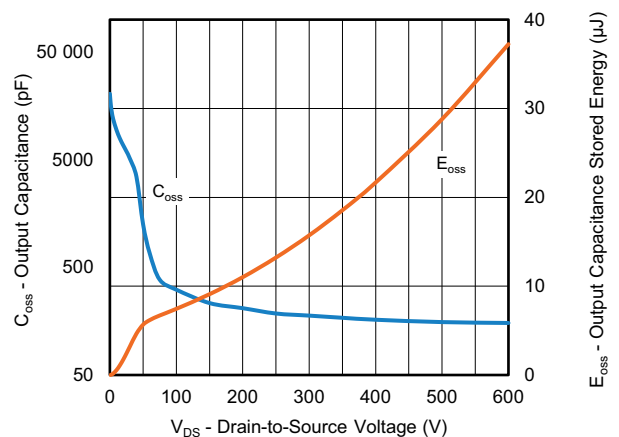
**Fig. 2 - Typical Output Characteristics**



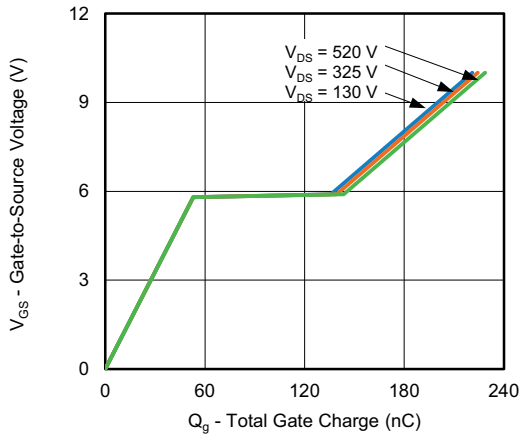
**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



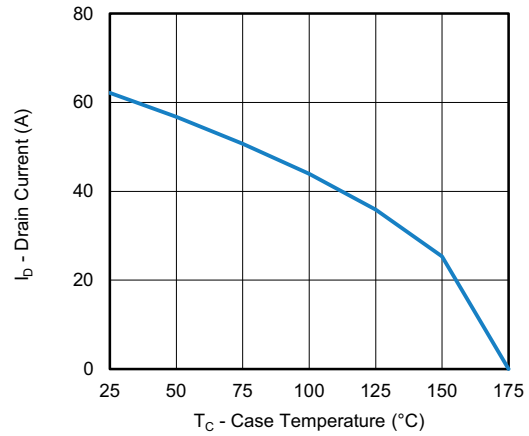
**Fig. 3 - Typical Transfer Characteristics**



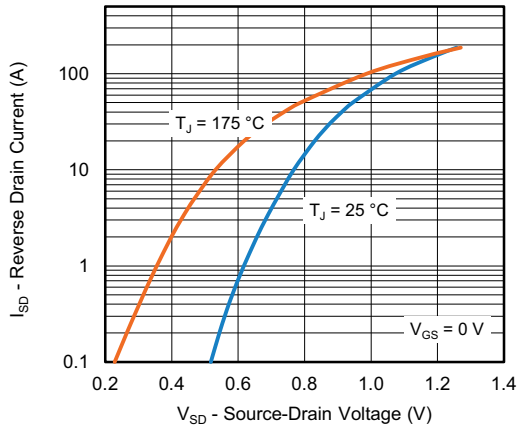
**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**



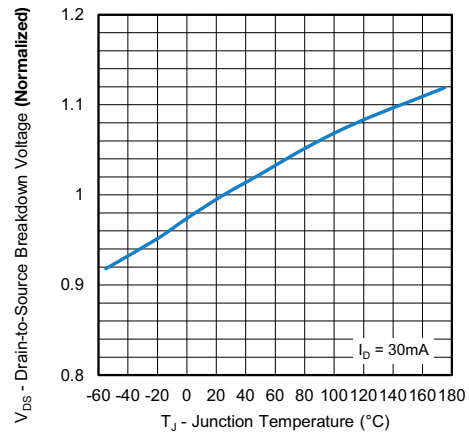
**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**



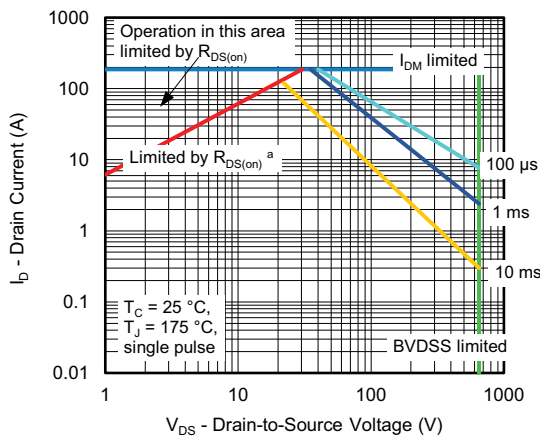
**Fig. 10 - Maximum Drain Current vs. Case Temperature**



**Fig. 8 - Typical Source-Drain Diode Forward Voltage**



**Fig. 11 - Temperature vs. Drain-to-Source Voltage**



**Fig. 9 - Maximum Safe Operating Area**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

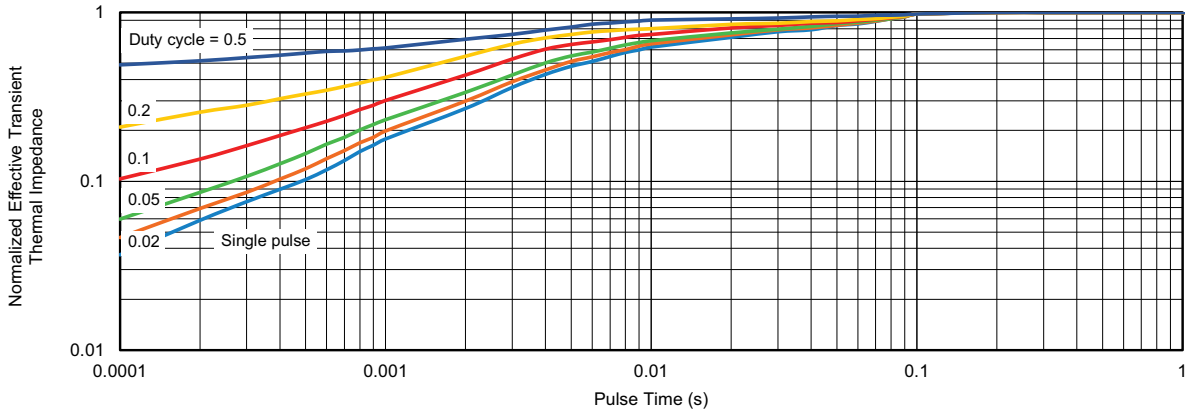


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

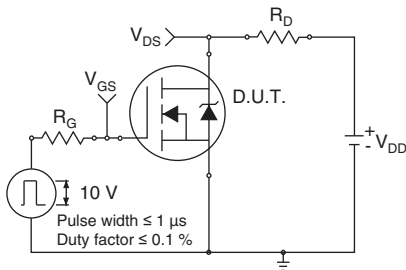


Fig. 13 - Switching Time Test Circuit

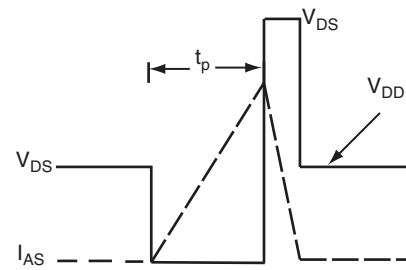


Fig. 16 - Unclamped Inductive Waveforms

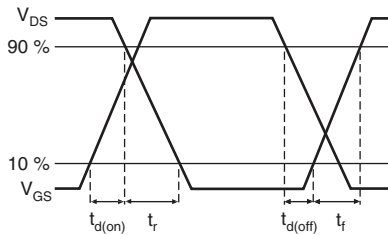


Fig. 14 - Switching Time Waveforms

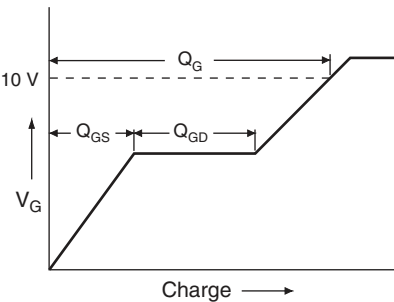


Fig. 17 - Basic Gate Charge Waveform

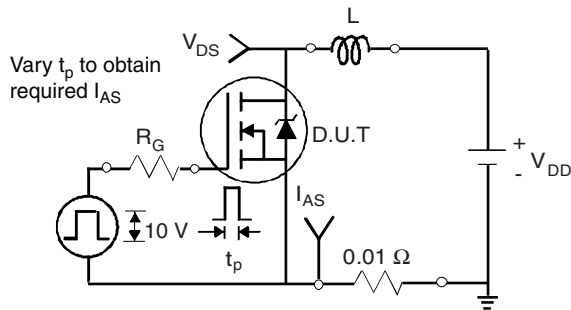


Fig. 15 - Unclamped Inductive Test Circuit

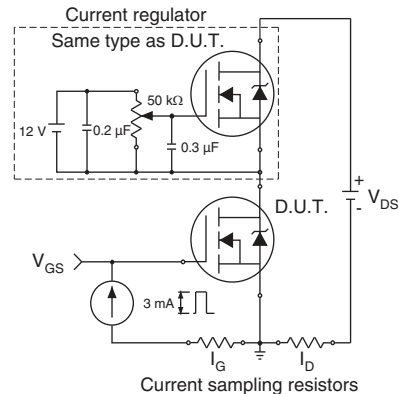
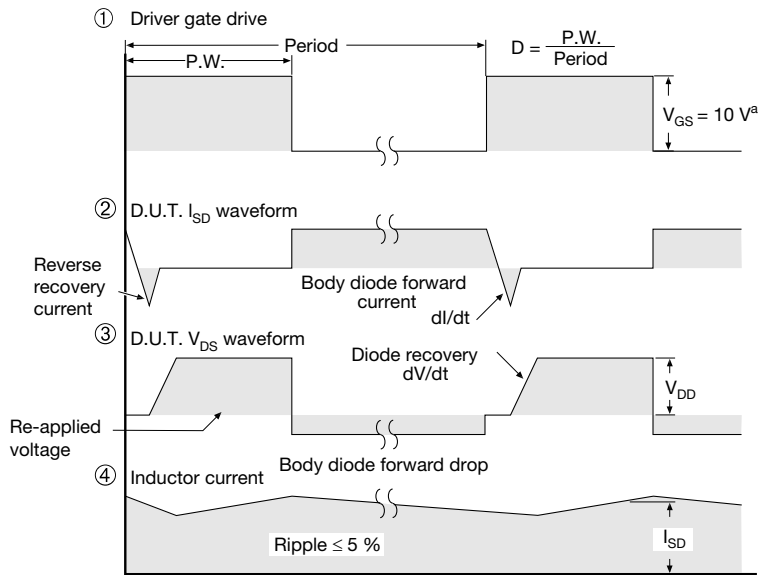
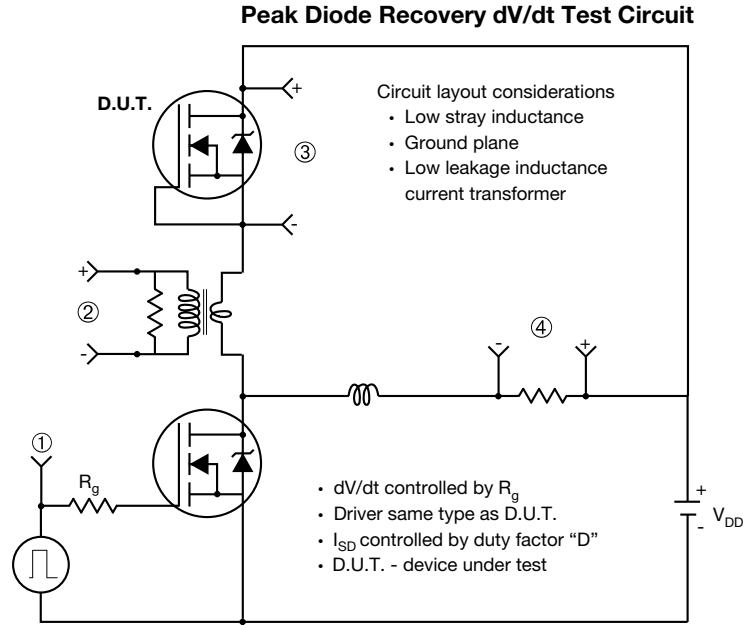


Fig. 18 - Gate Charge Test Circuit



**Note**  
a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 19 - For N-Channel**

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