



## ISO124 Precision Lowest-Cost Isolation Amplifier

### 1 Features

- 100% Tested for High-Voltage Breakdown
- Rated 1500 Vrms
- High IMR: 140 dB at 60 Hz
- 0.010% Maximum Nonlinearity
- Bipolar Operation:  $V_O = \pm 10$  V
- DIP-16 and SO-28
- Ease of Use: Fixed Unity Gain Configuration
- $\pm 4.5$ -V to  $\pm 18$ -V Supply Range

### 2 Applications

- Industrial Process Control:
  - Transducer Isolator, Isolator for Thermocouples, RTDs, Pressure Bridges, and Flow Meters, 4-mA to 20-mA Loop Isolation
- Ground Loop Elimination
- Motor and SCR Control
- Power Monitoring
- PC-Based Data Acquisition
- Test Equipment

### 3 Description

The ISO124 is a precision isolation amplifier incorporating a novel duty cycle modulation-demodulation technique. The signal is transmitted digitally across a 2-pF differential capacitive barrier. With digital modulation, the barrier characteristics do not affect signal integrity, thus resulting in excellent reliability and good high-frequency transient immunity across the barrier. Both barrier capacitors are imbedded in the plastic body of the package.

The ISO124 is easy to use. No external components are required for operation. The key specifications are 0.010% maximum nonlinearity, 50-kHz signal bandwidth, and 200- $\mu$ V/ $^{\circ}$ C  $V_{OS}$  drift. A power supply range of  $\pm 4.5$  V to  $\pm 18$  V and quiescent currents of  $\pm 5$  mA on  $V_{S1}$  and  $\pm 5.5$  mA on  $V_{S2}$  make the ISO124 ideal for a wide range of applications.

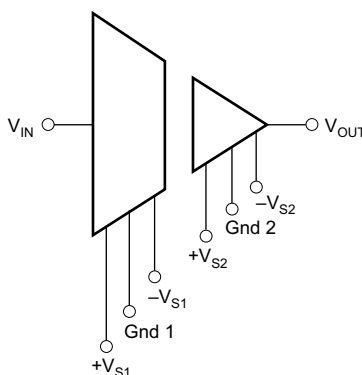
The ISO124 is available in PDIP-16 and SOIC-28 plastic surface-mount packages.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO124	PDIP (16)	17.90 mm x 7.50 mm
	SOIC (28)	20.01 mm x 6.61 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



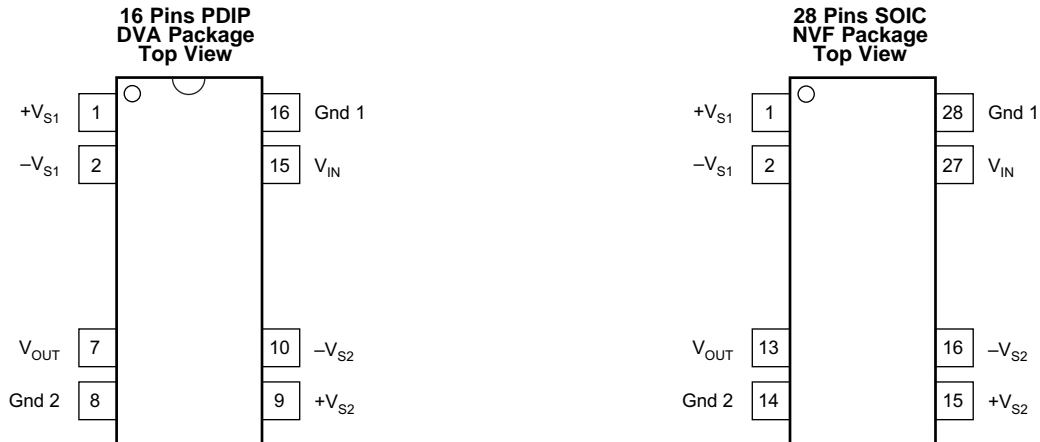
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## 5 Revision History

Changes from Revision C (September 2005) to Revision D	Page
<ul style="list-style-type: none"> <li>Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> </ul>	<b>1</b>

## 6 Pin Configuration and Functions



**Pin Functions**

PIN			I/O	DESCRIPTION
NAME	PDIP	SOIC		
GND	8	14	-	Low-side ground reference
	16	28	-	High-side ground reference
$V_{IN}$	15	27	I	High-side analog input
$V_{OUT}$	7	13	O	Low-side analog output
$+V_{S1}$	1	1	-	High-side positive analog supply
$-V_{S1}$	2	2	-	High-side negative analog supply
$+V_{S2}$	9	15	-	Low-side positive analog supply
$-V_{S2}$	10	16	-	Low-side negative analog supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage		±18	V
V <sub>IN</sub>		100	V
Continuous isolation voltage		1500	V <sub>rms</sub>
Junction temperature		125	°C
Output short to common		Continuous	
Storage temperature, T <sub>stg</sub>	–40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
T <sub>A</sub>	–25		85	°C
V <sub>S1</sub>		±15		V
V <sub>S2</sub>		±15		V
V <sub>IN</sub>		±10		V

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO124		UNIT
		DVA (PDIP)	NVF (SOIC)	
		16 PINS	28 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	79.8	51.0	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	32.9	32.4	
R <sub>θJB</sub>	Junction-to-board thermal resistance	42.2	29.5	
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.6	10.4	
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	40.9	29.0	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

At  $T_A = +25^\circ\text{C}$ ,  $V_{S1} = V_{S2} = \pm 15\text{ V}$ , and  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	ISO124P, U			UNIT
			MIN	TYP	MAX	
ISOLATION						
Rated Voltage, continuous ac 60 Hz			1500		Vac	
100% Test <sup>(1)</sup>		1s, 5pc PD	2400		Vac	
Isolation Mode Rejection		60 Hz	140		dB	
Barrier Impedance			10 <sup>14</sup>    2		Ω    pF	
Leakage Current at 60 Hz		V <sub>ISO</sub> = 240 Vrms	0.18	0.5	μArms	
GAIN						
Nominal Gain		V <sub>O</sub> = ±10 V	1		V/V	
Gain Error			±0.05	±0.50	%FSR	
Gain vs Temperature			±10		ppm/°C	
Nonlinearity <sup>(2)</sup>			±0.005	±0.010	%FSR	
INPUT OFFSET VOLTAGE						
Initial Offset			±20	±50	mV	
vs Temperature			±200		μV/°C	
vs Supply			±2		mV/V	
Noise			4		μV/√Hz	
INPUT						
Voltage Range			±10	±12.5	V	
Resistance			200		kΩ	
OUTPUT						
Voltage Range			±10	±12.5	V	
Current Drive			±5	±15	mA	
Capacitive Load Drive			0.1		μF	
Ripple Voltage <sup>(3)</sup>			20		mVp-p	
FREQUENCY RESPONSE						
Small-Signal Bandwidth			50		kHz	
Slew Rate			2		V/μs	
Settling Time 0.10%		V <sub>O</sub> = ±10 V	50		μs	
Settling Time 0.01%			350		μs	
Overload Recovery Time			150		μs	
POWER SUPPLIES						
Rated Voltage			±15		V	
Voltage Range			±4.5	±18	V	
V <sub>S1</sub>	Quiescent Current		±5.0	±7.0	mA	
V <sub>S2</sub>			±5.5	±7.0		
TEMPERATURE RANGE						
Specification			-25	85	°C	
Operating			-25	85	°C	
Storage			-40	125	°C	
R <sub>θJA</sub>	Thermal Resistance		100		°C/W	
R <sub>θJC</sub>			65		°C/W	

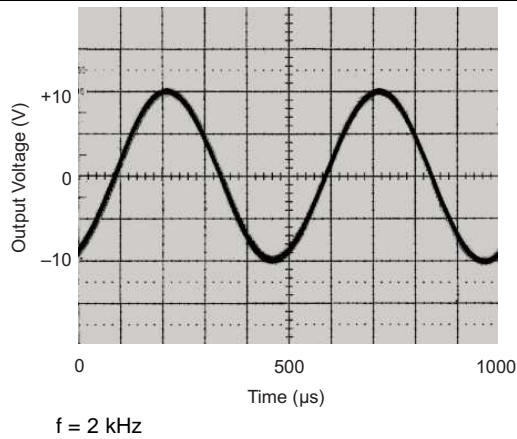
(1) Tested at 1.6 X rated, fail on 5 pC partial discharge.

(2) Nonlinearity is the peak deviation of the output voltage from the best-fit straight line. It is expressed as the ratio of deviation to FSR.

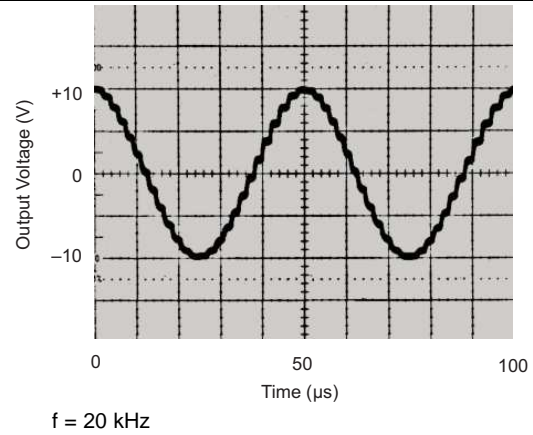
(3) Ripple frequency is at carrier frequency (500 kHz).

## 7.6 Typical Characteristics

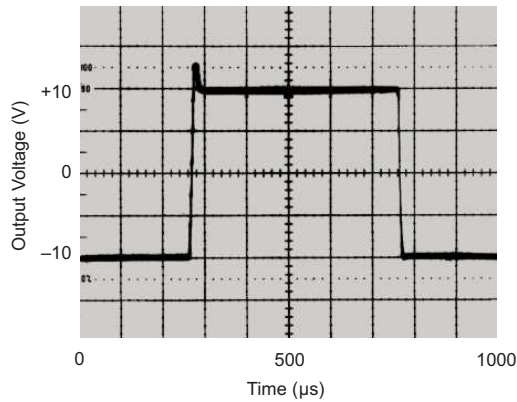
At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{ V}$ , unless otherwise noted.



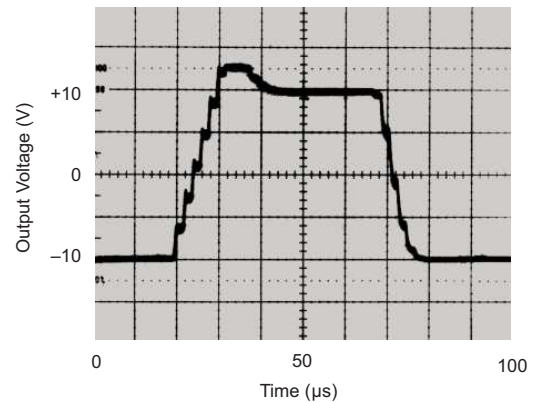
**Figure 1. Sine Response**



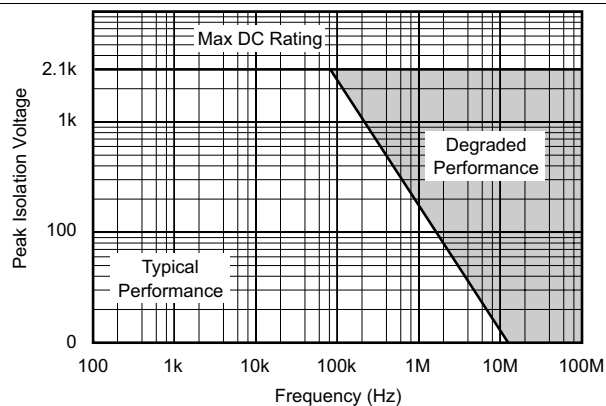
**Figure 2. Sine Response**



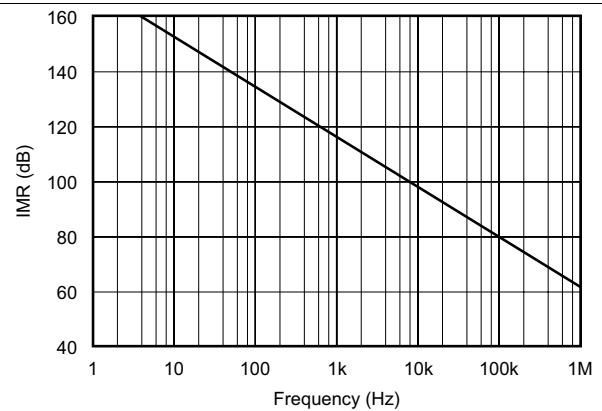
**Figure 3. Step Response**



**Figure 4. Step Response**



**Figure 5. Isolation Voltage vs Frequency**



**Figure 6. IMR vs Frequency**

## Typical Characteristics (continued)

At  $T_A = +25^\circ\text{C}$ , and  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

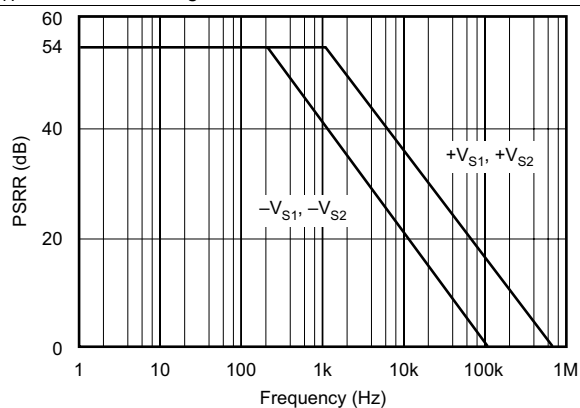


Figure 7. PSRR vs Frequency

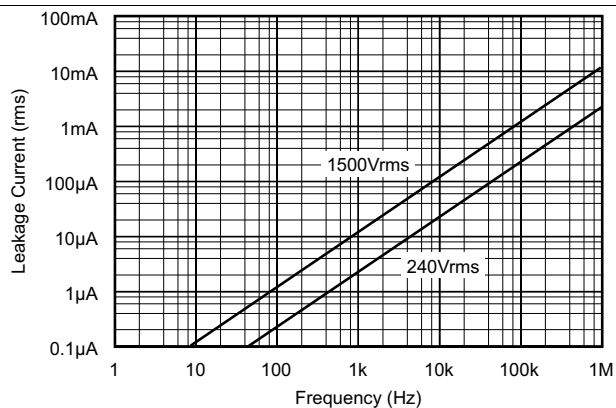
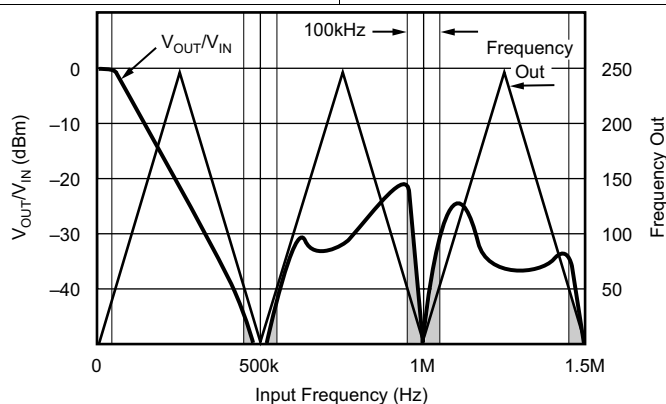


Figure 8. Isolation Leakage Current vs Frequency



NOTE: Shaded area shows aliasing frequencies that cannot be removed by a low-pass filter at the output.

Figure 9. Signal Response to Inputs Greater than 250 kHz





## **8.3 Feature Description**

### **8.3.1 Isolation Amplifier**

The ISO124 is a precision analog isolation amplifier. The input signal is transmitted digitally across a high-voltage differential capacitive barrier. With digital modulation the barrier characteristics do affect signal integrity, resulting in excellent reliability and high-frequency transient immunity.

## **8.4 Device Functional Modes**

The ISO124 does not have any additional functional modes.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Carrier Frequency Considerations

The ISO124 amplifier transmits the signal across the isolation barrier by a 500-kHz duty-cycle modulation technique. For input signals having frequencies below 250 kHz, this system works like any linear amplifier. But for frequencies above 250 kHz, the behavior is similar to that of a sampling amplifier. The typical characteristic "Signal Response to Inputs Greater Than 250 kHz" shows this behavior graphically; at input frequencies above 250 kHz, the device generates an output signal component of reduced magnitude at a frequency below 250 kHz. This is the aliasing effect of sampling at frequencies less than two times the signal frequency (the Nyquist frequency). At the carrier frequency and its harmonics, both the frequency and amplitude of the aliasing go to zero.

#### 9.1.2 Isolation Mode Voltage Induced Errors

IMV can induce errors at the output as indicated by the plots of IMV vs Frequency. It should be noted that if the IMV frequency exceeds 250 kHz, the output also will display spurious outputs (aliasing) in a manner similar to that for  $V_{IN} > 250$  kHz and the amplifier response will be identical to that shown in the "Signal Response to Inputs Greater Than 250 kHz" typical characteristic. This occurs because IMV-induced errors behave like input-referred error signals. To predict the total error, divide the isolation voltage by the IMR shown in the "IMR versus Frequency" typical performance curve and compute the amplifier response to this input-referred error signal from the data given in the "Signal Response to Inputs Greater Than 250 kHz" typical characteristic. For example, if a 800-kHz 1000-Vrms IMR is present, then a total of  $[(-60 \text{ dB}) + (-30 \text{ dB})] \times (1000 \text{ V}) = 32\text{-mV}$  error signal at 200 kHz plus a 1-V, 800-kHz error signal will be present at the output.

#### 9.1.3 High IMV dV/dt Errors

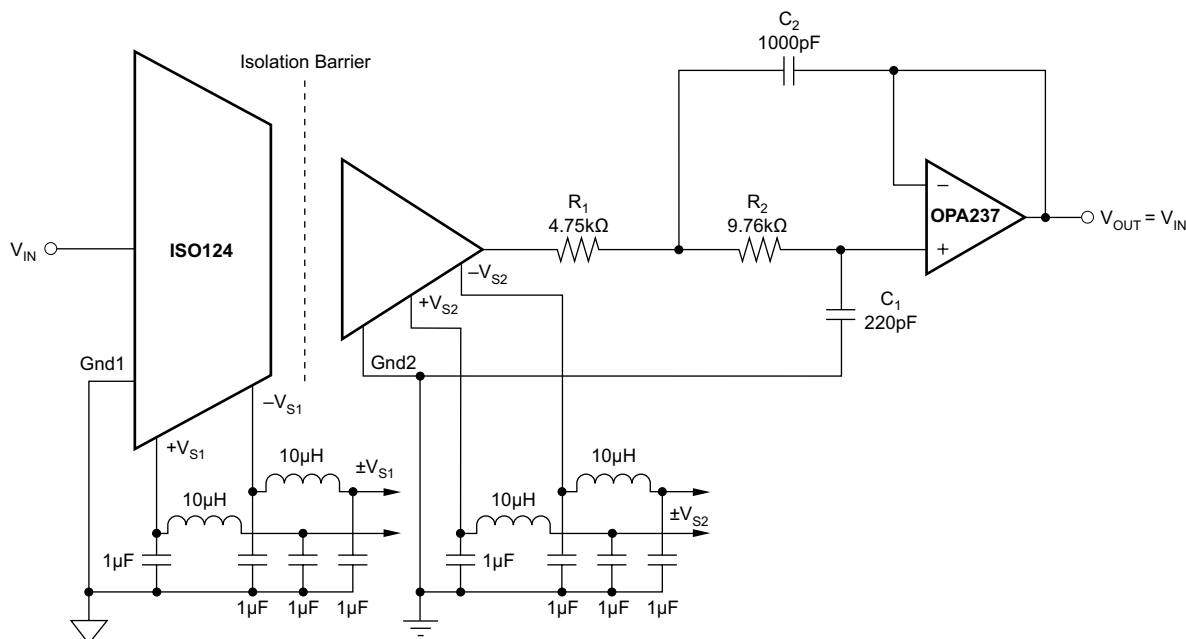
As the IMV frequency increases and the dV/dt exceeds 1000 V/ $\mu$ s, the sense amp may start to false trigger, and the output will display spurious errors. The common-mode current being sent across the barrier by the high slew rate is the cause of the false triggering of the sense amplifier. Lowering the power-supply voltages below  $\pm 15$  V may decrease the dV/dt to 500 V/Ms for typical performance.

#### 9.1.4 High Voltage Testing

TI has adopted a partial discharge test criterion that conforms to the German VDE0884 Optocoupler Standards. This method requires the measurement of minute current pulses ( $< 5$  pC) while applying 2400-Vrms, 60-Hz high-voltage stress across every ISO124 isolation barrier. No partial discharge may be initiated to pass this test. This criterion confirms transient overvoltage ( $1.6 \times 1500$  Vrms) protection without damage to the ISO124. Lifetest results verify the absence of failure under continuous rated voltage and maximum temperature.

This new test method represents the "state-of-the art" for nondestructive high-voltage reliability testing. It is based on the effects of nonuniform fields that exist in heterogeneous dielectric material during barrier degradation. In the case of void nonuniformities, electric field stress begins to ionize the void region before bridging the entire high-voltage barrier. The transient conduction of charge during and after the ionization can be detected externally as a burst of 0.01–0.1- $\mu$ s current pulses that repeat on each ac voltage cycle. The minimum ac barrier voltage that initiates partial discharge is defined as the "inception voltage." Decreasing the barrier voltage to a lower level is required before partial discharge ceases and is defined as the "extinction voltage." The package insulation processes have been characterized and developed to yield an inception voltage in excess of 2400 Vrms so that transient overvoltages below this level will not damage the ISO124. The extinction voltage is above 1500 Vrms so that even overvoltage induced partial discharge will cease once the barrier voltage is reduced to the 1500-Vrms (rated) level. Older high-voltage test methods relied on applying a large enough overvoltage (above rating) to break down marginal parts, but not so high as to damage good ones. Our new partial discharge testing gives us more confidence in barrier reliability than breakdown/no breakdown criteria.

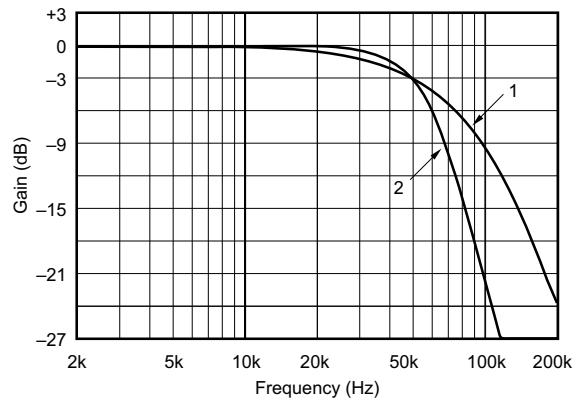
### 9.2.1 Output Filters



**Figure 10. ISO124 With Output Filter for Improved Ripple**

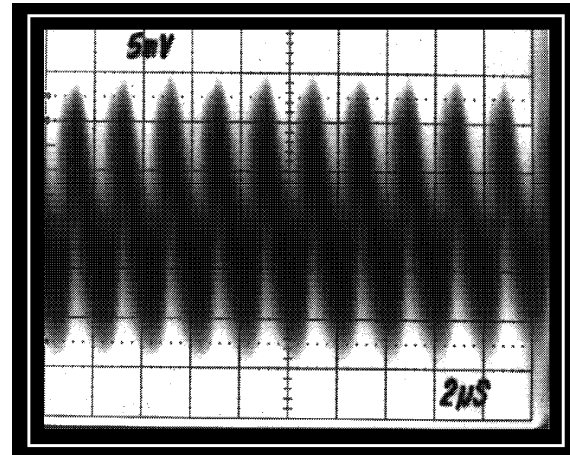
## Typical Applications (continued)

### 9.2.1.3 Application Curves

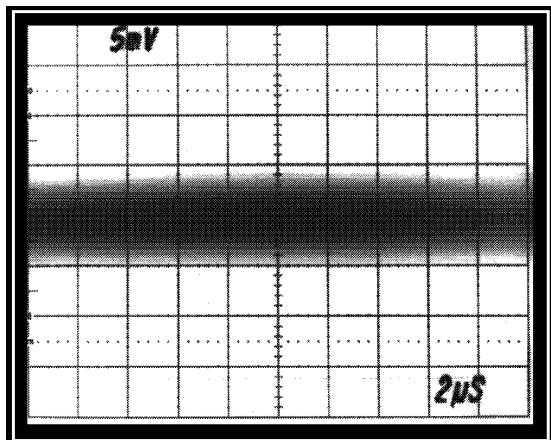


- 1) Standard ISO124 has 50kHz single-pole (Butterworth) response.
- 2) ISO124 with cascaded 50kHz,  $Q = 1$ , two-pole, low-pass filter has three-pole Butterworth response.

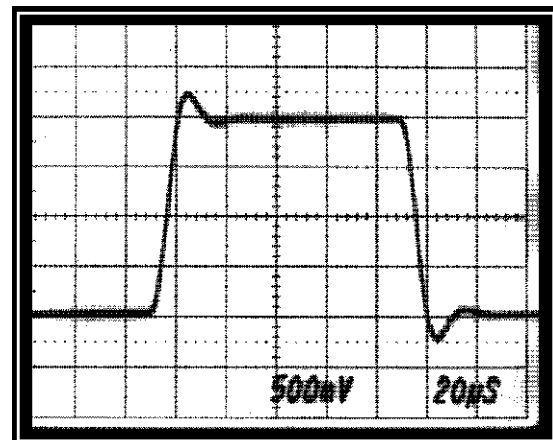
**Figure 11. Gain vs. Frequency**



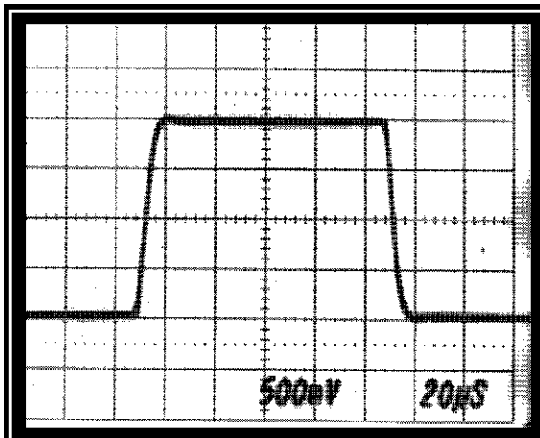
**Figure 12. Standard ISO124 (Approximately 20-mVp-p Output Ripple)**



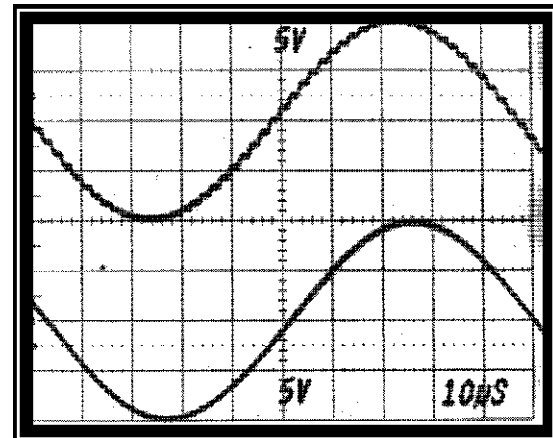
**Figure 13. Filtered ISO124 (No Visible Output Ripple)**



**Figure 14. Step Response of Standard ISO124**



**Figure 15. Step Response of ISO124 With Added Twopole Output Filter**

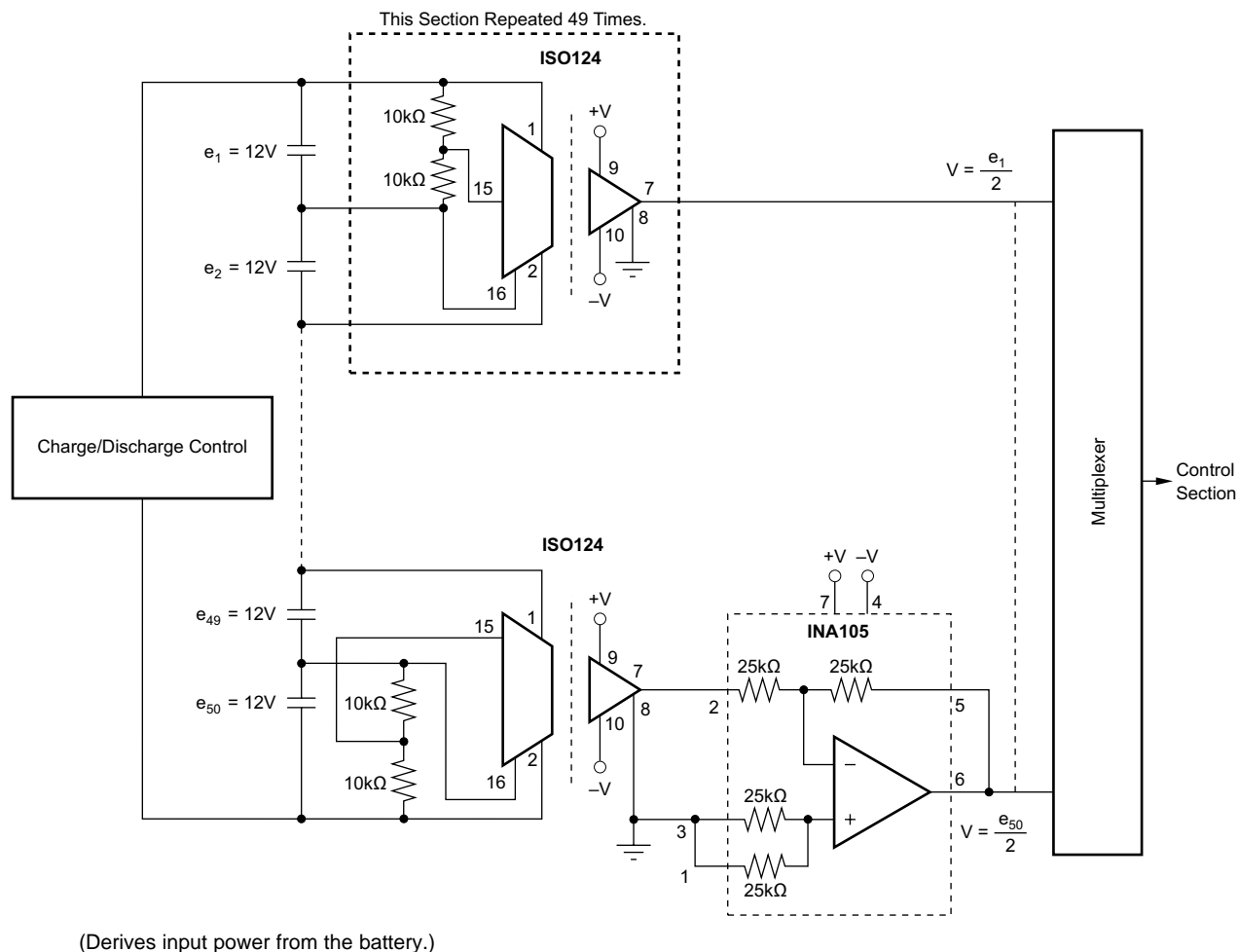


**Figure 16. Large-signal, 10-kHz Sine-wave Response of ISO124 With and Without Output Filter**

## Typical Applications (continued)

### 9.2.2 Battery Monitor

Figure 17 provides a means to monitor the cell voltage on a 600-V battery stack by using the battery as a power source for the isolated voltage.

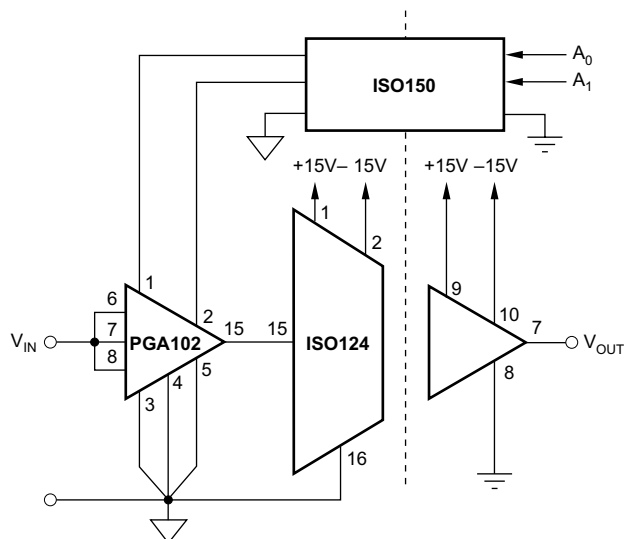


**Figure 17. Battery Monitor for a 600-V Battery Power System**

## Typical Applications (continued)

### 9.2.3 Programmable Gain Amplifier

In applications where variable gain configurations are required, a programmable gain amplifier like the PGA102 can be used with the ISO124. [Figure 18](#) uses an ISO150 to provide gain pin selection options to the PGA102.



**Figure 18. Programmable-Gain Isolation Channel With Gains of 1, 10, and 100**

## Typical Applications (continued)

### 9.2.4 Thermocouple Amplifier

For isolated temperature measurements, Figure 19 provides an application solution using the INA114 or INA128 feeding the input stage of the ISO124. The table provides suggested resistor values based on the type of thermistor used in the application.

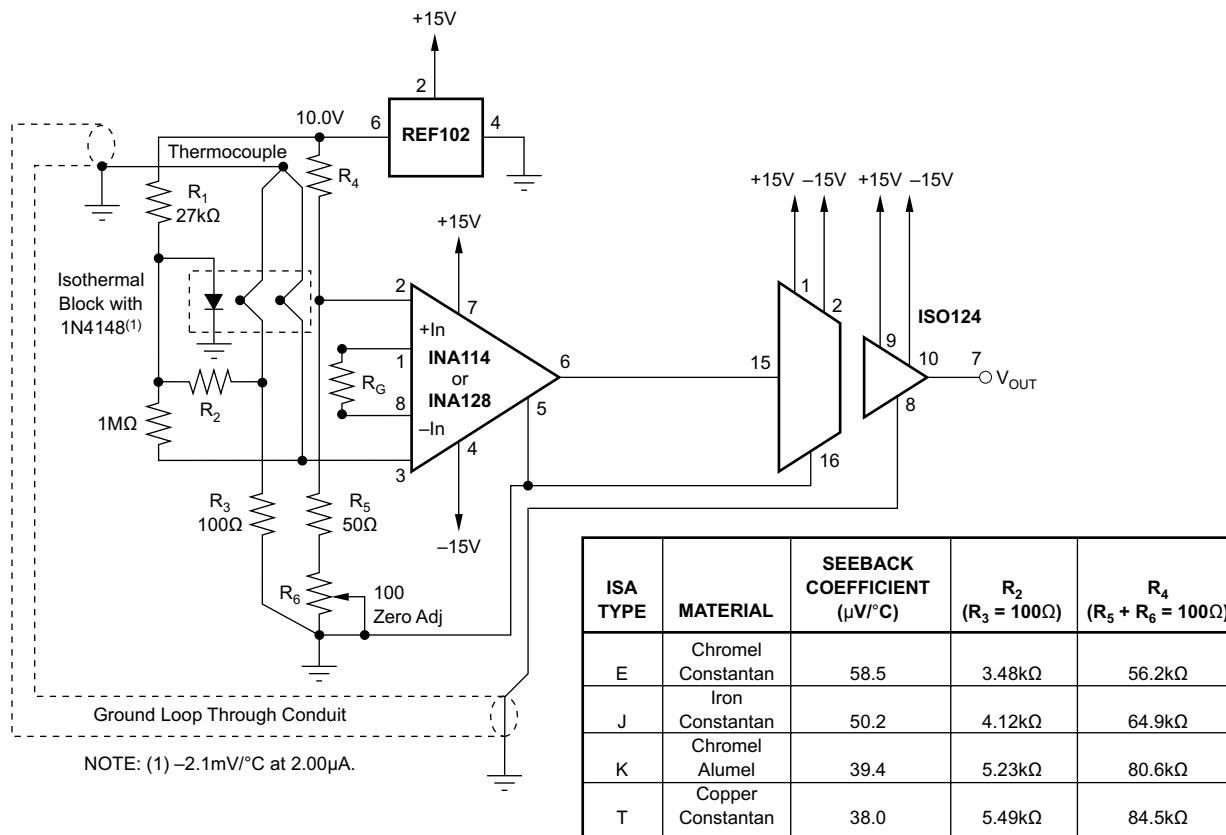
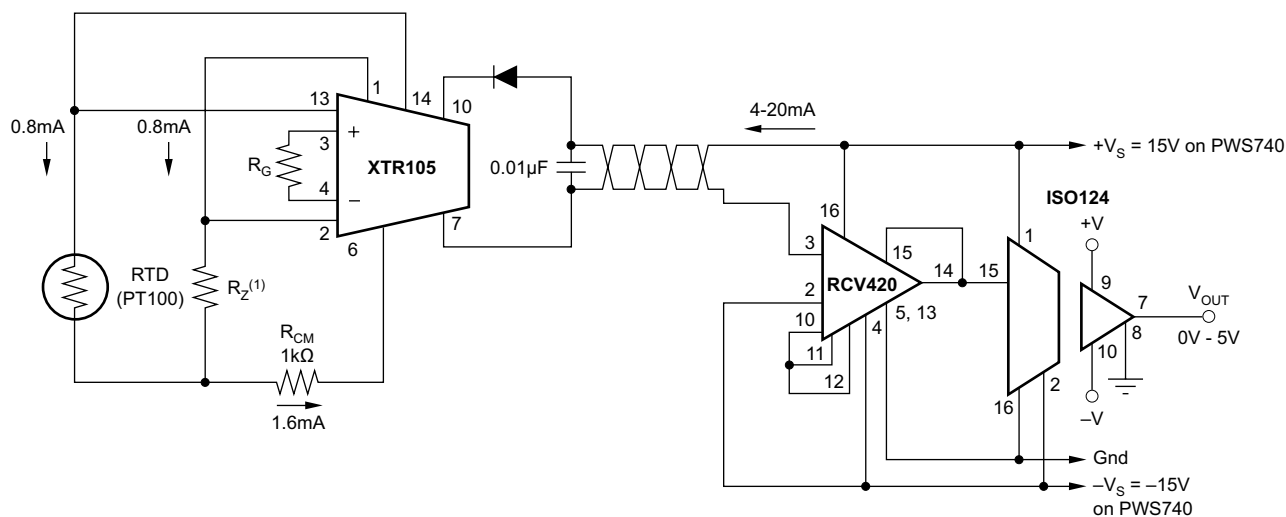


Figure 19. Thermocouple Amplifier With Ground Loop Elimination, Cold Junction Compensation, and Up-scale Burn-out

## Typical Applications (continued)

### 9.2.5 Isolated 4- to 20-mA Instrument Loop

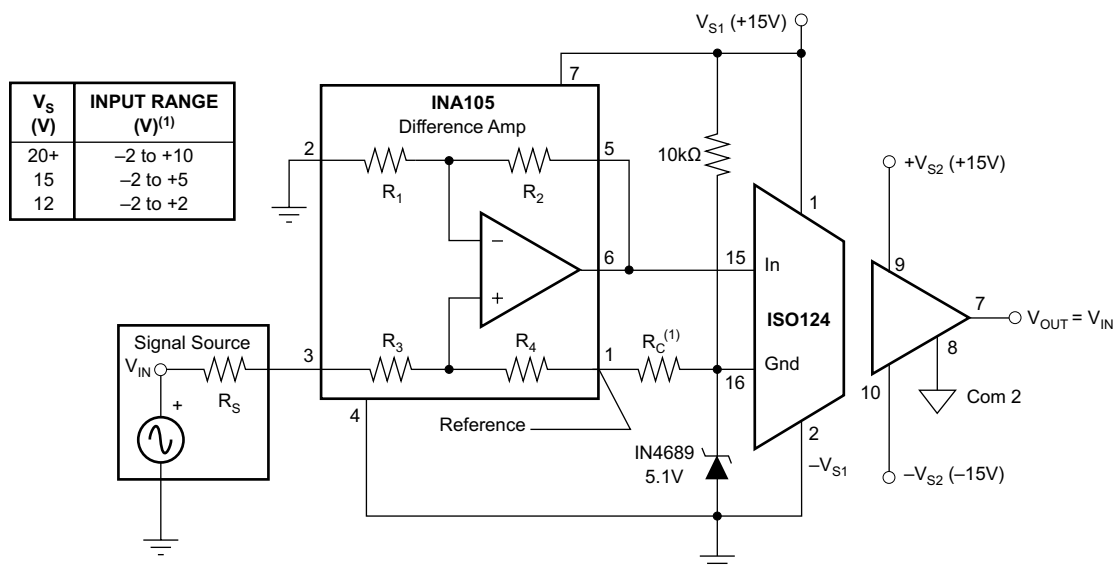
For isolated temperature measurements in a 4- to 20-mA loop, Figure 20 provides a solution using the XTR101 and RCV420. A high-performance PT100 resistance temperature detector (RTD) provides the user with an isolated 0- to 5-V representation of the isolated temperature measurement.



**Figure 20. Isolated 4- to 20-mA Instrument Loop (RTD Shown)**

### 9.2.6 Single-Supply Operation of the ISO124 Isolation Amplifier

The circuit shown in Figure 21 uses a 5.1-V Zener diode to generate the negative supply for an ISO12x from a single supply on the high-voltage side of the isolation amplifier. The input measuring range will be dependent on the applied voltage as noted in the accompanying table.



NOTE: Because the amplifier is unity gain, the input range is also the output range. The output can go to -2 V because the output section of the ISO amp operates from dual supplies.

For additional information refer to Application Note [SBOA004](#)

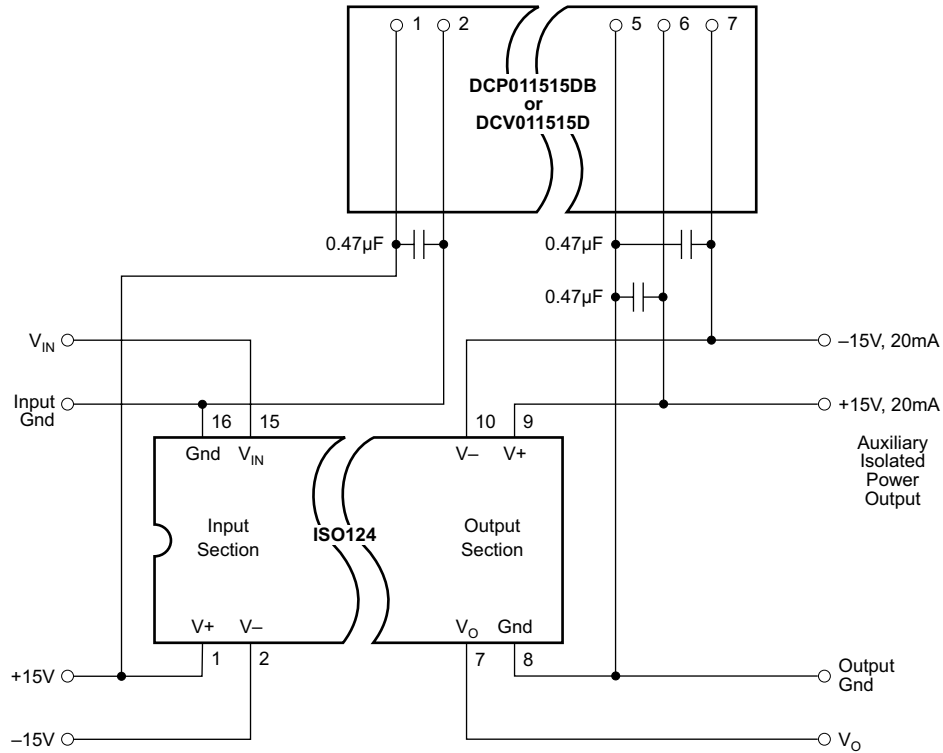
**Figure 21. Single-Supply Operation of the ISO124 Isolation Amplifier Schematic**



## Typical Applications (continued)

### 9.2.7 Input-Side Powered ISO Amplifier

The user side of the ISO124 can be powered from the high voltage side using an isolated DC-DC converter as shown in [Figure 22](#).

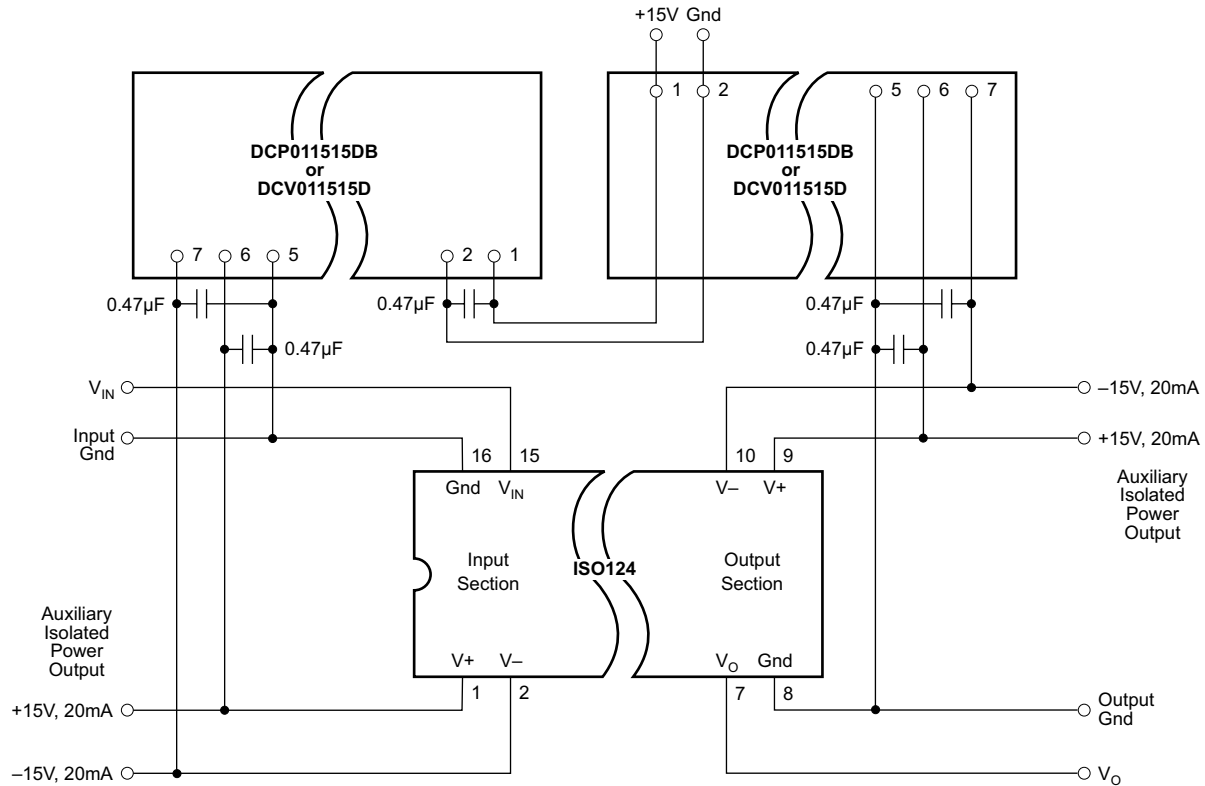


**Figure 22. Input-Side Powered ISO Amplifier Schematic**

## Typical Applications (continued)

### 9.2.8 Powered ISO Amplifier With Three-Port Isolation

Figure 23 illustrates an application solution that provides isolated power to both the user and high-voltage sides of the ISO124 amplifier.



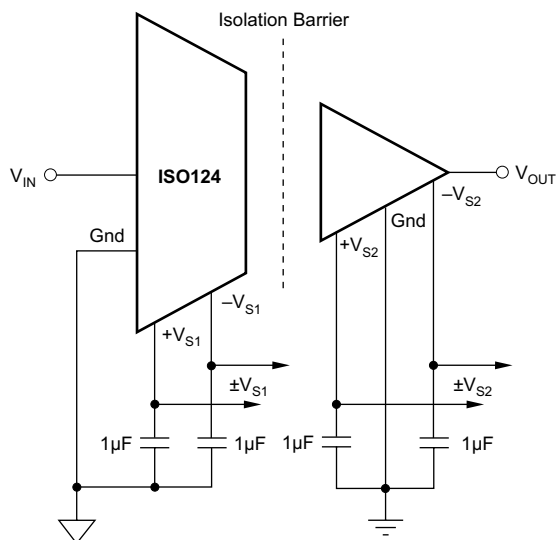
**Figure 23. Powered ISO Amplifier With Three-Port Isolation Schematic**

## 10 Power Supply Recommendations

### 10.1 Signal and Supply Connections

Each power-supply pin should be bypassed with 1- $\mu$ F tantalum capacitors located as close to the amplifier as possible. The internal frequency of the modulator/demodulator is set at 500 kHz by an internal oscillator. Therefore, if it is desired to minimize any feedthrough noise (beat frequencies) from a DC-DC converter, use a  $\pi$  filter on the supplies (see Figure 10). The ISO124 output has a 500-kHz ripple of 20 mV, which can be removed with a simple 2-pole low-pass filter with a 100-kHz cutoff using a low-cost op amp (see Figure 10).

The input to the modulator is a current (set by the 200-k $\Omega$  integrator input resistor) that makes it possible to have an input voltage greater than the input supplies, as long as the output supply is at least  $\pm 15$  V. It is therefore possible, when using an unregulated DC-DC converter, to minimize PSR related output errors with  $\pm 5$ -V voltage regulators on the isolated side and still get the full  $\pm 10$ -V input and output swing.



**Figure 24. Basic Signal and Power Connections**

## 11 Layout

### 11.1 Layout Guidelines

To maintain the isolation barrier of the device, the distance between the high-side ground (pin 16 or 28) and the low-side ground (pin 8 or 14) should be kept at maximum; that is, the entire area underneath the device should be kept free of any conducting materials.

### 11.2 Layout Example

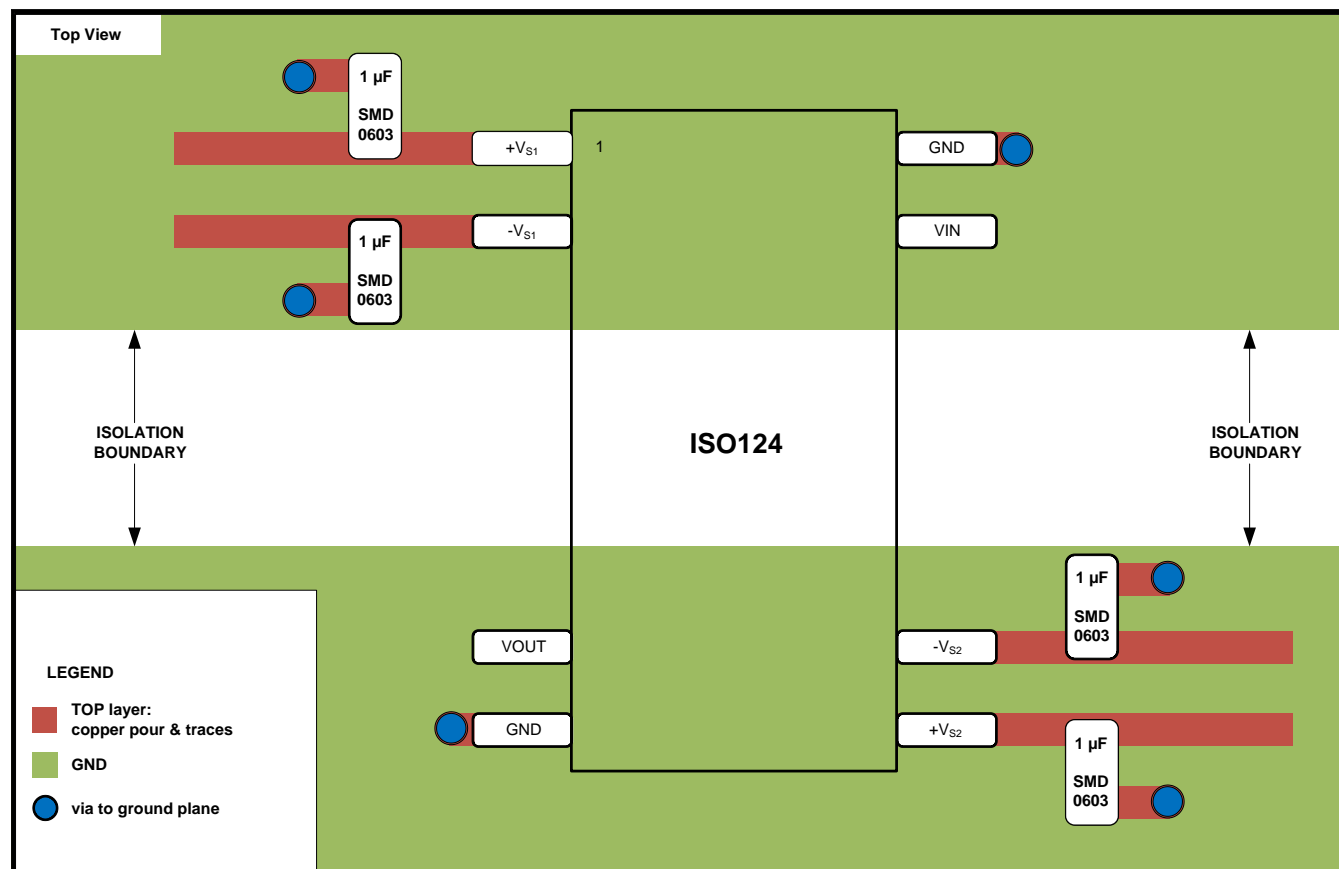


Figure 25. ISO124 Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

- *Single-Supply Operation of Isolation Amplifiers*, [SBOA004](#)
- *Simple Output Filter Eliminates ISO Amp Output Ripple and Keeps Full Bandwidth*, [SBOA012](#)
- *FilterPro™ User's Guide*, [SBFA001](#)

### 12.2 Trademarks

FilterPro is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO124P	ACTIVE	PDIP	NVF	8	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-25 to 85	ISO124P	<a href="#">Samples</a>
ISO124U	ACTIVE	SOIC	DVA	8	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	<a href="#">Samples</a>
ISO124U/1K	ACTIVE	SOIC	DVA	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	<a href="#">Samples</a>
ISO124U/1KE4	ACTIVE	SOIC	DVA	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	<a href="#">Samples</a>
ISO124UE4	ACTIVE	SOIC	DVA	8	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-25 to 85	ISO 124U	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

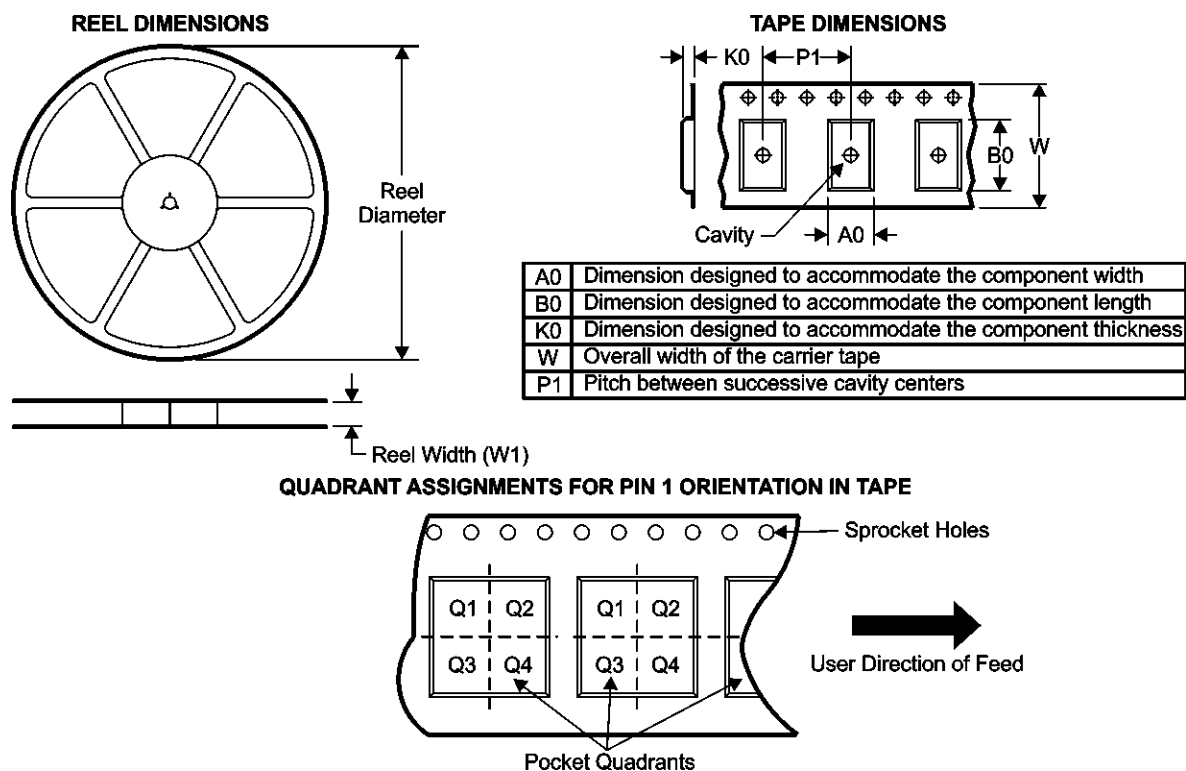
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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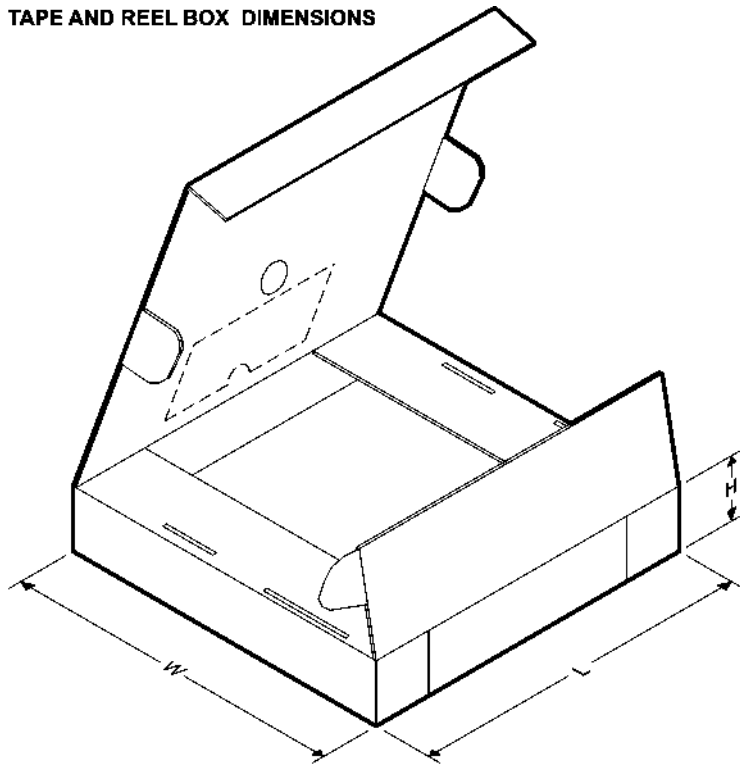
**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO124U/1K	SOIC	DVA	8	1000	330.0	24.4	10.9	18.3	3.2	12.0	24.0	Q1



## TAPE AND REEL BOX DIMENSIONS

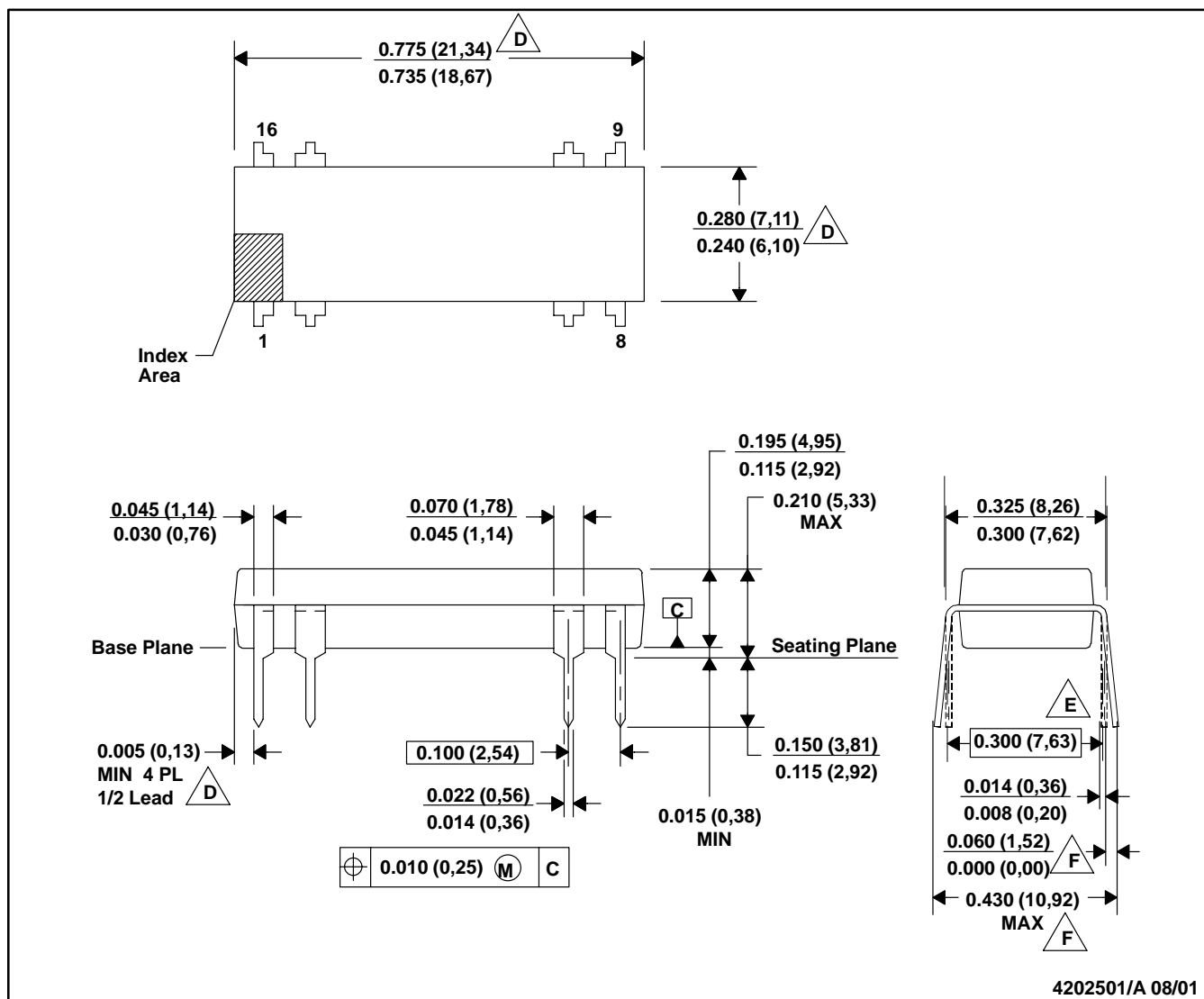


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO124U/1K	SOIC	DVA	8	1000	367.0	367.0	45.0

## NVF (R-PDIP-T8/16)

## PLASTIC DUAL-IN-LINE



- A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001-BB with the exception of lead count.

**D.** Dimensions do not include mold flash or protrusions.  
 Mold flash or protrusions shall not exceed 0.010 (0,25).

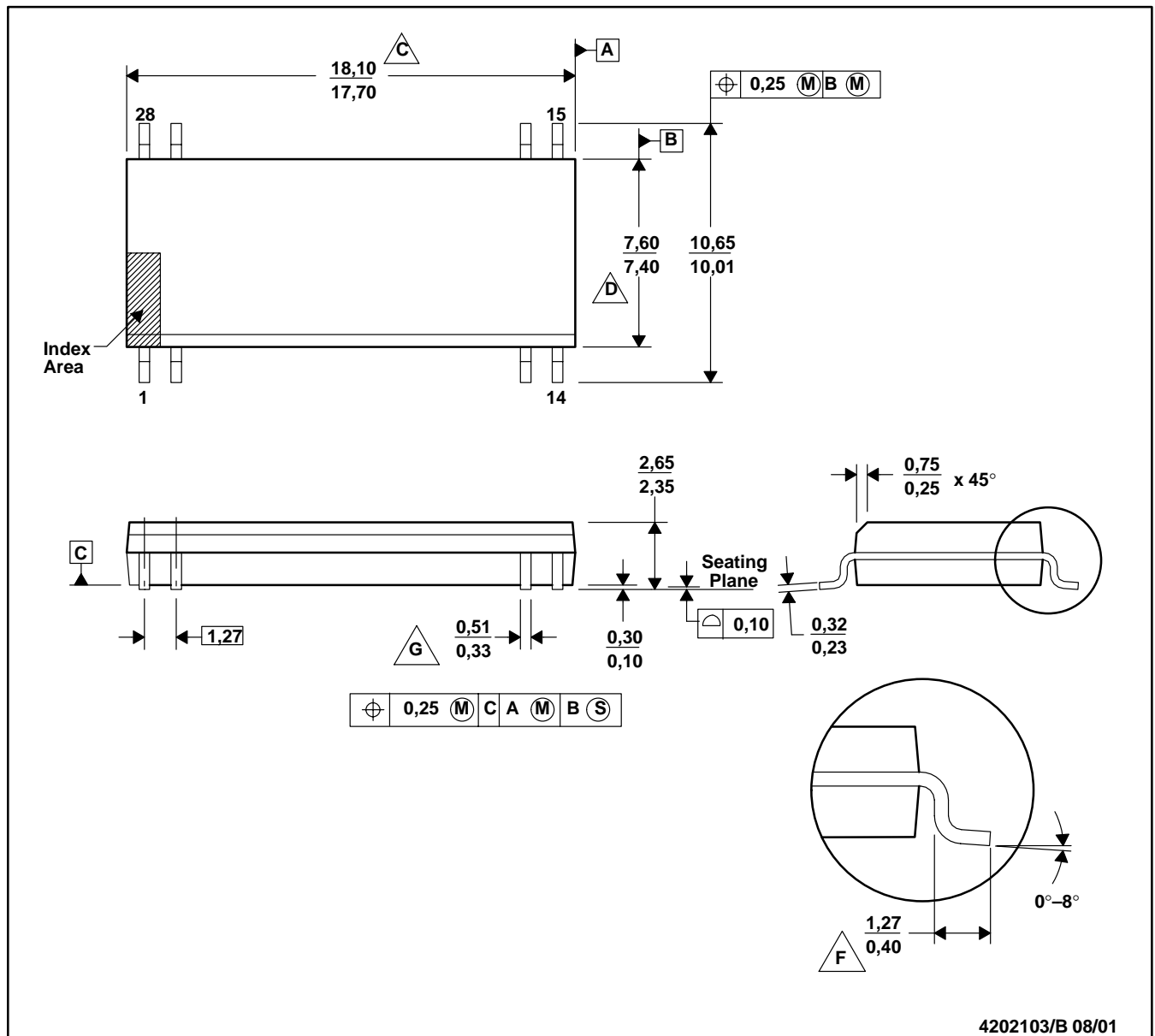
**E.** Dimensions measured with the leads constrained to be perpendicular to Datum C.

**F.** Dimensions are measured at the lead tips with the leads unconstrained.

- G. A visual index feature must be located within the cross-hatched area.

## DVA (R-PDSO-G8/28)

## PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body length dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0,15 mm per side.

D. Body width dimension does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0,25 mm per side.

E. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross-hatched area.

F. Lead dimension is the length of terminal for soldering to a substrate.

G. Lead width, as measured 0,36 mm or greater above the seating plane, shall not exceed a maximum value of 0,61 mm.

H. Lead-to-lead coplanarity shall be less than 0,10 mm from seating plane.

I. Falls within JEDEC MS-013-AE with the exception of the number of leads.

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Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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