



Product Change Notification / SYST-30UXEF314

Date:

04-Jun-2024

Product Category:

8-Bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ATtiny3224/3226/3227 Silicon Errata and Data Sheet Clarifications

Affected CPNs:

[SYST-30UXEF314_Affected_CPN_06042024.pdf](#)

[SYST-30UXEF314_Affected_CPN_06042024.csv](#)

Notification Text:

SYST-30UXEF314

Microchip has released a new Document for the ATtiny3224/3226/3227 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [ATtiny3224/3226/3227 Silicon Errata and Data Sheet Clarifications](#).

Notification Status: Final

Description of Change:

- Document:
 - Editorial updates
- Added new errata:
 - Device:
 - 2.2.1. IDD Power-Down Current Consumption
 - 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values
 - 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces
 - ADC: 2.3.3. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode
 - CRCSCAN: 2.5.1. Running CRC Scan on Part of The Flash is Non-Functional
 - NVMCTRL: 2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register
 - TCA: 2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode
 - USART: 2.9.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field

- Added new data sheet clarifications:
 - I/O Multiplexing and Considerations:
- 3.1.1. I/O Multiplexing
 - Electrical Characteristics:
- 3.2.1. I/O Pin Characteristics
- 3.2.2. SPI - Timing Characteristics
- 3.2.3. Programming Time

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 04 June 2024

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[ATtiny3224/3226/3227 Silicon Errata and Data Sheet Clarifications](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

ATTINY3224-SSF
ATTINY3224-SSFVAO
ATTINY3224-XF
ATTINY3226-XF
ATTINY3226-SF
ATTINY3226-MF
ATTINY3227-MF
ATTINY3224-SSU
ATTINY3224-XU
ATTINY3226-XU
ATTINY3226-SU
ATTINY3226-MU
ATTINY3227-MU
ATTINY3224-SSUR
ATTINY3224-XUR
ATTINY3226-XUR
ATTINY3226-SUR
ATTINY3226-MUR
ATTINY3227-MUR
ATTINY3224-SSFR
ATTINY3224-XFR
ATTINY3226-XFR
ATTINY3226-SFR
ATTINY3226-MFR
ATTINY3227-MFR

Silicon Errata and Data Sheet Clarifications

ATtiny3224/3226/3227



The ATtiny3224/3226/3227 devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002345), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATtiny3224/3226/3227 devices.

Notes:

- This document summarizes all the silicon errata issues from all the silicon revisions, previous and current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002345) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- Erratum is not applicable.
- X Erratum is applicable.

Peripheral	Short Description	Valid for Silicon Revision
		Rev. A
Device	2.2.1. IDD Power-Down Current Consumption	X
	2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
	2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces	X
ADC	2.3.1. Low Latency Mode Must Be Set Before Changing ADC Configuration	X
	2.3.2. The PGA Initialization Delay Does Not Work Outside Low Latency Mode	X
	2.3.3. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode	X
CCL	2.4.1. The CCL Must be Disabled to Change the Configuration of a Single LUT	X
CRCSCAN	2.5.1. Running CRC Scan on Part of The Flash is Non-Functional	X
NVMCTRL	2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register	X
TCA	2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.8.1. CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.9.1. Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X
	2.9.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field	X

2. Silicon Errata Issues

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 IDD Power-Down Current Consumption

For material with date code 2045 (manufactured in the year 2020, week 45) or older, the IDD power-down leakage can exceed the targeted maximum value of 1.5 μ A.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.2.2 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCKEN in CLKCTRL.MCLKLOCK to '1' when the OSC20M oscillator is used as the Main Clock source.

Affected Silicon Revisions

Rev. A
X

2.2.3 Write Operation Lost if Consecutive Writes to Specific Address Spaces

An ST/STD/STS instruction to address ≥ 64 followed by either an ST/STD instruction to address < 64 or a write to the SLPCTRL.CTRLA register will cause a loss of the last write.

Work Around

To avoid loss of write operation, use one of the following workarounds depending on address space:

- Insert an NOP instruction before writing to address < 64 , or use the OUT instruction instead of ST/STD
- Insert an NOP instruction before writing to SLPCTRL.CTRLA register

Affected Silicon Revisions

Rev. A
X

2.3 ADC - Analog-to-Digital Converter

2.3.1 Low Latency Mode Must Be Set Before Changing ADC Configuration

If using the low latency mode in the ADC, the initialization delay does not start for settings configured before the Low Latency (LOWLAT) bit in the Control A (ADCn.CTRLA) register. This may result in a conversion starting before the initialization time has ended and give a corrupt result.

Work Around

Enable the low latency bit (LOWLAT) in the Control A (ADCn.CTRLA) register at the start of ADC initialization before configuring any other register in the ADC.

Affected Silicon Revisions

Rev. A
X

2.3.2 The PGA Initialization Delay Does Not Work Outside Low Latency Mode

The initialization delay for the PGA does not start when the LOWLAT bit is '0'. This may cause a corrupt conversion when the PGA is the module with the slowest initialization time. When using the internal references, this is not an issue because of a slower initialization delay.

Work Around

Set the ADC in low latency mode by setting the Low Latency (LOWLAT) bit in the Control A (CTRLA) register to '1'.

Affected Silicon Revisions

Rev. A
X

2.3.3 ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode

If the Low Latency bit (LOWLAT in ADCn.CTRLA) is '1', the ADC stays active when the device enters Power-Down or Standby sleep modes. If the Free-Running bit (FREERUN in ADCn.CTRLF) is '1', the ADC continues to run in Standby sleep mode even if the Run in Standby bit (RUNSTDBY in ADCn.CTRLA) is '0'. In both cases, the interrupts will not trigger when the device enters Power-Down or Standby sleep mode.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.4 CCL - Configurable Custom Logic

2.4.1 The CCL Must be Disabled to Change the Configuration of a Single LUT

To reconfigure an LUT, the CCL peripheral must first be disabled (write ENABLE in CCL.CTRLA to '0'). Writing ENABLE to '0' will disable all the LUTs, and affects the LUTs not under reconfiguration.

Work Around

None

Affected Silicon Revisions

Rev. A
X

2.5 CRCSCAN - Cyclic Redundancy Check Memory Scan

2.5.1 Running CRC Scan on Part of The Flash is Non-Functional

- Running CRC scan on the boot section does not work if FUSE.BOOTSIZE is different from 0x00
- Running CRC scan on the boot and application section does not work if FUSE.CODESIZE is different from 0x00
- Running CRC scan on the entire Flash works

Work Around

None

Affected Silicon Revisions

Rev. A
X

2.6 NVMCTRL - Nonvolatile Memory Controller

2.6.1 Wrong Reset Value of NVMCTRL.CTRLA Register

In some cases, the reset value of NVMCTRL.CTRLA will not be '0'. Even reserved bits can be read as '1' after Reset.

Work Around

Ignore the initial value.

Affected Silicon Revisions

Rev. A
X

2.7 TCA - 16-Bit Timer/Counter Type A

2.7.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to a NORMAL or FRQ mode (WGMode in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset the count direction to default. The default is counting upwards.

Work Around

None.

Affected Silicon Revisions

Rev. A
X

2.8 TCB - 16-Bit Timer/Counter Type B

2.8.1 CCMP and CNT Registers Act as 16-Bit Registers in 8-Bit PWM Mode

When the TCB is operating in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CCMP and CNT registers act as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A
X

2.9 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

2.9.1 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception. The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This triggers the Start-of-Frame Detector and falsely detects the next falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data. Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around

Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Re-enable it by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. A
X

2.9.2 Receiver Non-Functional after Detection of Inconsistent Synchronization Field

The USART Receiver becomes non-functional when the Inconsistent Synchronization Field Interrupt Flag (ISFIF) in the Status (USARTn.STATUS) register is set. The ISFIF interrupt flag is set when the Receiver Mode (RXMODE) bit field in the Control B (USARTn.CTRLB) register is configured to Generic Auto-Baud (GENAUTO) or LIN Constrained Auto-Baud (LINAUTO) mode, and the received synchronization frame does not conform to the conditions described in the data sheet. Clearing the flag does not re-enable the USART Receiver.

Work Around

When the ISFIF interrupt flag is set, disable and re-enable the USART Receiver by first writing a '0' and then a '1' to the Receiver Enable (RXEN) bit in the Control B (USARTn.CTRLB) register.

Affected Silicon Revisions

Rev. A
X

3. Data Sheet Clarifications

Note the following typographic corrections and clarifications for the latest version of the device data sheet (www.microchip.com/DS40002345).

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 I/O Multiplexing and Considerations

3.1.1 I/O Multiplexing

A clarification is made in *Table 3-1. PORT Function Multiplexing*. The “footnote 4” is also valid for LUT0-OUT on pin PB4. Functional change is shown in **bold**.

Table 3-1. PORT Function Multiplexing

VQFN 24-pin	VQFN 20-pin	SSOP/SOIC 20-pin	SSOP/SOIC 14-pin	Pin Name (1,2)	Other/ Special	ADC0 ⁽³⁾	AC0	USART0	USART1	SPI0	TWI0	TCA0	TCBn	CCL
23	19	16	10	PA0	RESET UPDI									LUT0-IN0
24	20	17	11	PA1		AIN1		TXD ⁽⁴⁾	TXD	MOSI				LUT0-IN1
1	1	18	12	PA2	EVOUTA	AIN2		RxD ⁽⁴⁾	RXD	MISO				LUT0-IN2
2	2	19	13	PA3	EXTCLK	AIN3		XCK ⁽⁴⁾	XCK	SCK		WO3	1,WO	
3	3	20	14	GND										
4	4	1	1	VDD										
5	5	2	2	PA4		AIN4		XDIR ⁽⁴⁾	XDIR	SS		WO4		LUT0-OUT
6	6	3	3	PA5	VREFA	AIN5	OUT					WO5	0,WO	LUT3-OUT ⁽⁴⁾
7	7	4	4	PA6		AIN6	AINN0							
8	8	5	5	PA7	EVOUTA ⁽⁴⁾	AIN7	AINP0							LUT1-OUT
9				PB7	EVOUTB ⁽⁴⁾									
10				PB6			AINP3							LUT2-OUT ⁽⁴⁾
11	9	6		PB5	CLKOUT	AIN8	AINP1					WO2 ⁽⁴⁾		
12	10	7		PB4	RESET ⁽⁴⁾	AIN9	AINN1					WO1 ⁽⁴⁾		LUT0-OUT ⁽⁴⁾
13	11	8	6	PB3	TOSC1			RxD				WO0 ⁽⁴⁾		LUT2-OUT
14	12	9	7	PB2	TOSC2 EVOUTB			TxD				WO2		LUT2-IN2
15	13	10	8	PB1		AIN10	AINP2	XCK			SDA	WO1		LUT2-IN1
16	14	11	9	PB0		AIN11	AINN2	XDIR			SCL	WO0		LUT2-IN0
17	15	12		PC0		AIN12			XCK ⁽⁴⁾	SCK ⁽⁴⁾			0,WO ⁽⁴⁾	LUT3-IN0
18	16	13		PC1		AIN13			RxD ⁽⁴⁾	MISO ⁽⁴⁾				LUT1-OUT ⁽⁴⁾ LUT3-IN1
19	17	14		PC2	EVOUTC	AIN14			TxD ⁽⁴⁾	MOSI ⁽⁴⁾				LUT3-IN2
20	18	15		PC3		AIN15			XDIR ⁽⁴⁾	SS ⁽⁴⁾		WO3 ⁽⁴⁾		LUT1-IN0
21				PC4								WO4 ⁽⁴⁾	1,WO ⁽⁴⁾	LUT1-IN1 LUT3-OUT
22				PC5								WO5 ⁽⁴⁾		LUT1-IN2

Notes:

- Pin names are Pxn type, with x being the PORT instance (A, B) and n the pin number. Notation for signals is PORTx_PINn.
- All pins can be used for external interrupt where pins Px2 and Px6 of each port have full asynchronous detection. All pins can be used as event input.
- AIN[15:8] can not be used as negative ADC input for differential measurements.
- Alternative pin location. For selecting an alternative pin location, refer to the PORTMUX section.

3.2 Electrical Characteristics

3.2.1 I/O Pin Characteristics

A clarification of the maximum value of the pull-up resistor is made in *Table 33-16 in the Electrical Characteristics* section. Functional change is shown in **bold**.

Operating conditions:

- $T_A = [-40, 125]^{\circ}\text{C}$
- $V_{DD} = [1.8, 5.5]\text{V}$, unless otherwise specified

Table 33-16. I/O Pin Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input low-voltage, except RESET pin as I/O		-0.2	-	$0.3 \times V_{DD}$	V
V_{IH}	Input high-voltage, except RESET pin as I/O		$0.7 \times V_{DD}$	-	$V_{DD} + 0.2\text{V}$	V
I_{IH} / I_{IL}	I/O pin Input leakage current, except RESET pin as I/O	$V_{DD} = 5.5\text{V}$, Pin high	-	< 0.05	-	μA
		$V_{DD} = 5.5\text{V}$, Pin low	-	< 0.05	-	
V_{OL}	I/O pin drive strength	$V_{DD} = 1.8\text{V}$, $I_{OL} = 1.5\text{ mA}$	-	-	0.36	V
		$V_{DD} = 3.0\text{V}$, $I_{OL} = 7.5\text{ mA}$	-	-	0.6	
		$V_{DD} = 5.0\text{V}$, $I_{OL} = 15\text{ mA}$	-	-	1	
V_{OH}	I/O pin drive strength	$V_{DD} = 1.8\text{V}$, $I_{OH} = 1.5\text{ mA}$	1.44	-	-	V
		$V_{DD} = 3.0\text{V}$, $I_{OH} = 7.5\text{ mA}$	2.4	-	-	
		$V_{DD} = 5.0\text{V}$, $I_{OH} = 15\text{ mA}$	4	-	-	
I_{total}	Maximum combined I/O sink current per pin group ⁽¹⁾		-	-	100	mA
	Maximum combined I/O source current per pin group ⁽¹⁾		-	-	100	
V_{IL2}	Input low-voltage on RESET pin as I/O		-0.2	-	$0.3 \times V_{DD}$	V
V_{IH2}	Input high-voltage on RESET pin as I/O		$0.7 \times V_{DD}$	-	$V_{DD} + 0.2\text{V}$	V
V_{OL2}	I/O pin drive strength on RESET pin as I/O	$V_{DD} = 1.8\text{V}$, $I_{OL} = 0.1\text{ mA}$	-	-	0.36	V
		$V_{DD} = 3.0\text{V}$, $I_{OL} = 0.25\text{ mA}$	-	-	0.6	
		$V_{DD} = 5.0\text{V}$, $I_{OL} = 0.5\text{ mA}$	-	-	1	
V_{OH2}	I/O pin drive strength on RESET pin as I/O	$V_{DD} = 1.8\text{V}$, $I_{OH} = 0.1\text{ mA}$	1.44	-	-	V
		$V_{DD} = 3.0\text{V}$, $I_{OH} = 0.25\text{ mA}$	2.4	-	-	
		$V_{DD} = 5.0\text{V}$, $I_{OH} = 0.5\text{ mA}$	4	-	-	
t_{RISE}	Rise time	$V_{DD} = 3.0\text{V}$, load = 20 pF	-	2.5	-	ns
		$V_{DD} = 5.0\text{V}$, load = 20 pF	-	1.5	-	
t_{FALL}	Fall time	$V_{DD} = 3.0\text{V}$, load = 20 pF	-	2.0	-	ns
		$V_{DD} = 5.0\text{V}$, load = 20 pF	-	1.3	-	
C_{PIN}	I/O pin capacitance, unless otherwise specified		-	4	-	pF
C_{PIN_TWI}	I/O pin capacitance on TWI pins ⁽²⁾		-	12	-	pF
C_{PIN_AC}	I/O pin capacitance on AC pins ⁽²⁾	PB0 and PB1	-	12	-	pF
		other AC pins	-	4	-	
C_{PIN_VREFA}	I/O pin capacitance on ADC VREFA pin		-	14	-	pF
R_p	Pull-up resistor		20	35	60	k Ω

Notes:

1. Pin group x (Px[7:0]). The combined continuous sink/source current for all I/O ports should not exceed the limits.
2. This capacitance is valid for pins with this functionality, even when that functionality is unused.

3.2.2 SPI - Timing Characteristics

A clarification regarding the SPI clock is made in *Table 33-18. SPI - Timing Characteristics*. Functional changes are shown in **bold**.

Table 33-18. SPI - Timing Characteristics⁽¹⁾

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{SCK}	SCK clock frequency	Host	-	-	10	MHz
t_{SCK}	SCK period	Host	100	-	-	ns
t_{SCKW}	SCK high/low width	Host	-	$0.5 \times t_{SCK}$	-	ns
t_{SCKR}	SCK rise time	Host	-	2.7	-	ns
t_{SCKF}	SCK fall time	Host	-	2.7	-	ns
t_{MIS}	MISO setup to SCK	Host	-	10	-	ns
t_{MIH}	MISO hold after SCK	Host	-	10	-	ns
t_{MOS}	MOSI setup to SCK	Host	-	$0.5 \times t_{SCK}$	-	ns
t_{MOH}	MOSI hold after SCK	Host	-	1.0	-	ns
f_{SSCK}	Client SCK clock frequency	Client	-	-	5	MHz
t_{SSCK}	Client SCK Period	Client	$6 \times t_{CLK_PER}$	-	-	ns
t_{SSCKW}	SCK high/low width	Client	$3 \times t_{CLK_PER}$	-	-	ns
t_{SSCKR}	SCK rise time	Client	-	-	1600	ns
t_{SSCKF}	SCK fall time	Client	-	-	1600	ns
t_{SIS}	MOSI setup to SCK	Client	0.0	-	-	ns
t_{SIH}	MOSI hold after SCK	Client	$3 \times t_{CLK_PER}$	-	-	ns
t_{SSS}	SS setup to SCK	Client	-	t_{CLK_PER}	-	ns
t_{SSH}	SS hold after SCK	Client	-	t_{CLK_PER}	-	ns
t_{SOS}	MISO setup to SCK	Client	-	8.0	-	ns
t_{SOH}	MISO hold after SCK	Client	-	13	-	ns
t_{SOSS}	MISO setup after SS low	Client	-	11	-	ns
t_{SOSH}	MISO hold after SS low	Client	-	8.0	-	ns

Note:

1. These parameters are for design guidance only and are not production-tested.

3.2.3 Programming Time

A clarification of the *Programming Time* section is made. *Table 33-34* has been upgraded from *Programming Times* to *Memory Programming Specifications* in the *Electrical Characteristics*. Functional changes are shown in **bold**.

Table 33-34. Memory Programming Specifications

Symbol	Description	Min.	Typ. †	Max.	Unit	Conditions
Data EEPROM Memory Specifications						
E_{EE}* 	Data EEPROM byte endurance	100k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +105°C
t_{EE_RET}	Characteristic retention	—	40	—	Year	T_A = 55°C
t _{EE_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK _{CPU} cycles	
t _{EE_EEER}	Full EEPROM Erase (EEER)	—	4	—	ms	
t _{EE_WP}	Page Write (WP)	—	2	—	ms	
t _{EE_ER}	Page Erase (ER)	—	2	—	ms	
t _{EE_ERWP}	Page Erase-Write (ERWP)	—	4	—	ms	
Program Flash Memory Specifications						
E_{FL}* 	Flash memory cell endurance	10k	—	—	Erase/Write cycles	-40°C ≤ T_A ≤ +105°C
t_{FL_RET}	Characteristic retention	—	40	—	Year	T_A = 55°C
V_{FL_UPDI}	V_{DD} for Chip Erase operation	V_{BODLEVEL0}(1)	—	V_{DDMAX}	V	
t _{FL_PBC}	Page Buffer Clear (PBC)	—	7	—	CLK _{CPU} cycles	
t _{FL_CHER}	Chip Erase (CHER)	—	4	—	ms	
t _{FL_WP}	Page Write (WP)	—	2	—	ms	
t _{FL_ER}	Page Erase (ER)	—	2	—	ms	
t _{FL_ERWP}	Page Erase/Write (ERWP)	—	4	—	ms	
t _{FL_UPDI}	Chip Erase with UPDI	—	40	—	ms	32 KB Flash
† Data in the “Typ.” column is at T _A = 25°C and V _{DD} = 3.0V unless otherwise specified. These parameters are not tested and are for design guidance only.						
* These parameters are characterized but not tested in production.						
Note:						
1. The Brown-out Detector (BOD) configured with BODLEVEL0 is forced ON during Chip Erase. The erase attempt will fail if the supply voltage V _{DD} is below V _{BOD} for BODLEVEL0.						

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc. Rev.	Date	Comments
B	05/2024	- Document: - Editorial updates - Added new errata: - Device: 2.2.1. IDD Power-Down Current Consumption 2.2.2. Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values 2.2.3. Write Operation Lost if Consecutive Writes to Specific Address Spaces - ADC: 2.3.3. ADC Stays Active in Sleep Modes for Low Latency Mode and Free Running Mode - CRCSCAN: 2.5.1. Running CRC Scan on Part of The Flash is Non-Functional - NVMCTRL: 2.6.1. Wrong Reset Value of NVMCTRL.CTRLA Register - TCA: 2.7.1. Restart Will Reset Counter Direction in NORMAL and FRQ Mode - USART: 2.9.2. Receiver Non-Functional after Detection of Inconsistent Synchronization Field - Added new data sheet clarifications: - I/O Multiplexing and Considerations: 3.1.1. I/O Multiplexing - Electrical Characteristics: 3.2.1. I/O Pin Characteristics 3.2.2. SPI - Timing Characteristics 3.2.3. Programming Time
A	09/2021	Initial document release

Microchip Information

The Microchip Website

Microchip provides online support via our website at www.microchip.com/. This website is used to make files and information easily available to customers. Some of the content available includes:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip design partner program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Product Change Notification Service

Microchip's product change notification service helps keep customers current on Microchip products. Subscribers will receive email notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, go to www.microchip.com/pcn and follow the registration instructions.

Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Embedded Solutions Engineer (ESE)
- Technical Support

Customers should contact their distributor, representative or ESE for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in this document.

Technical support is available through the website at: www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure

that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, Adaptec, AVR, AVR logo, AVR Freaks, BesTime, BitCloud, CryptoMemory, CryptoRF, dsPIC, flexPWR, HELDO, IGLOO, JukeBlox, KeeLoq, Kleer, LANCheck, LinkMD, maXStylus, maXTouch, MediaLB, megaAVR, Microsemi, Microsemi logo, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, PolarFire, Prochip Designer, QTouch, SAM-BA, SenGenuity, SpyNIC, SST, SST Logo, SuperFlash, Symmetricom, SyncServer, Tachyon, TimeSource, tinyAVR, UNI/O, Vectron, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

AgileSwitch, ClockWorks, The Embedded Control Solutions Company, EtherSynch, Flashtec, Hyper Speed Control, HyperLight Load, Libero, motorBench, mTouch, Powermite 3, Precision Edge, ProASIC, ProASIC Plus, ProASIC Plus logo, Quiet-Wire, SmartFusion, SyncWorld, TimeCesium, TimeHub, TimePictra, TimeProvider, and ZL are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, Augmented Switching, BlueSky, BodyCom, Clockstudio, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, Espresso T1S, EtherGREEN, EyeOpen, GridTime, IdealBridge, IGaT, In-Circuit Serial Programming, ICSP, INICnet, Intelligent Paralleling, IntelliMOS, Inter-Chip Connectivity, JitterBlocker, Knob-on-Display, MarginLink, maxCrypto, maxView, memBrain, Mindi, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, mSiC, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, Power MOS IV, Power MOS 7, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, RTAX, RTG4, SAM-ICE, Serial Quad I/O, simpleMAP, SimpliPHY, SmartBuffer, SmartHLS, SMART-I.S., storClad, SQI, SuperSwitcher, SuperSwitcher II, Switchtec, SynchroPHY, Total Endurance, Trusted Time, TSHARC, Turing, USBCheck, VariSense, VectorBlox, VeriPHY, ViewSpan, WiperLock, XpressConnect, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

The Adaptec logo, Frequency on Demand, Silicon Storage Technology, and Symmcom are registered trademarks of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2024, Microchip Technology Incorporated and its subsidiaries. All Rights Reserved.

ISBN: 978-1-6683-4611-2

Quality Management System

For information regarding Microchip's Quality Management Systems, please visit www.microchip.com/quality.

Worldwide Sales and Service

AMERICAS	ASIA/PACIFIC	ASIA/PACIFIC	EUROPE
Corporate Office 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 480-792-7200 Fax: 480-792-7277 Technical Support: www.microchip.com/support Web Address: www.microchip.com	Australia - Sydney Tel: 61-2-9868-6733 China - Beijing Tel: 86-10-8569-7000 China - Chengdu Tel: 86-28-8665-5511 China - Chongqing Tel: 86-23-8980-9588 China - Dongguan Tel: 86-769-8702-9880 China - Guangzhou Tel: 86-20-8755-8029 China - Hangzhou Tel: 86-571-8792-8115 China - Hong Kong SAR Tel: 852-2943-5100 China - Nanjing Tel: 86-25-8473-2460 China - Qingdao Tel: 86-532-8502-7355 China - Shanghai Tel: 86-21-3326-8000 China - Shenyang Tel: 86-24-2334-2829 China - Shenzhen Tel: 86-755-8864-2200 China - Suzhou Tel: 86-186-6233-1526 China - Wuhan Tel: 86-27-5980-5300 China - Xian Tel: 86-29-8833-7252 China - Xiamen Tel: 86-592-2388138 China - Zhuhai Tel: 86-756-3210040	India - Bangalore Tel: 91-80-3090-4444 India - New Delhi Tel: 91-11-4160-8631 India - Pune Tel: 91-20-4121-0141 Japan - Osaka Tel: 81-6-6152-7160 Japan - Tokyo Tel: 81-3-6880-3770 Korea - Daegu Tel: 82-53-744-4301 Korea - Seoul Tel: 82-2-554-7200 Malaysia - Kuala Lumpur Tel: 60-3-7651-7906 Malaysia - Penang Tel: 60-4-227-8870 Philippines - Manila Tel: 63-2-634-9065 Singapore Tel: 65-6334-8870 Taiwan - Hsin Chu Tel: 886-3-577-8366 Taiwan - Kaohsiung Tel: 886-7-213-7830 Taiwan - Taipei Tel: 886-2-2508-8600 Thailand - Bangkok Tel: 66-2-694-1351 Vietnam - Ho Chi Minh Tel: 84-28-5448-2100	Austria - Wels Tel: 43-7242-2244-39 Fax: 43-7242-2244-393 Denmark - Copenhagen Tel: 45-4485-5910 Fax: 45-4485-2829 Finland - Espoo Tel: 358-9-4520-820 France - Paris Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79 Germany - Garching Tel: 49-8931-9700 Germany - Haan Tel: 49-2129-3766400 Germany - Heilbronn Tel: 49-7131-72400 Germany - Karlsruhe Tel: 49-721-625370 Germany - Munich Tel: 49-89-627-144-0 Fax: 49-89-627-144-44 Germany - Rosenheim Tel: 49-8031-354-560 Israel - Hod Hasharon Tel: 972-9-775-5100 Italy - Milan Tel: 39-0331-742611 Fax: 39-0331-466781 Italy - Padova Tel: 39-049-7625286 Netherlands - Drunen Tel: 31-416-690399 Fax: 31-416-690340 Norway - Trondheim Tel: 47-72884388 Poland - Warsaw Tel: 48-22-3325737 Romania - Bucharest Tel: 40-21-407-87-50 Spain - Madrid Tel: 34-91-708-08-90 Fax: 34-91-708-08-91 Sweden - Gothenberg Tel: 46-31-704-60-40 Sweden - Stockholm Tel: 46-8-5090-4654 UK - Wokingham Tel: 44-118-921-5800 Fax: 44-118-921-5820