PD69208M and PD69200

Datasheet

8-Port PSE PoE Manager and PSE PoE Controller

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Microsemi

a Microchip company

Contents

1 Revision History 1
1.1 Revision 6.0 1
1.2 Revision 5.0 1
1.3 Revision 4.0 1
1.4 Revision 3.0 2
1.5 Revision 2.0 2
1.6 Revision 1.2 2
1.7 Revision 1.1 2
1.8 Revision 1.0 2
2 Overview 3
2.1 Features 4
2.2 Applications 4
2.3 Typical PoE Application 5
3 Functional Descriptions 6
3.1 Digital Block Module 6
3.2 PD Detection Generator 6
3.3 Classification Generator 6
3.4 Current Limiter 7
3.5 Main Power MOSFET 7
3.6 Analog to Digital Converter 7
3.7 Power on Reset 7
3.8 Voltage Regulator 7
3.9 Clock 7
3.10 SPI Communication 8
3.11 PD69208M SPI Addressing 8
3.12 Broadcast 8
3.13 SPI Timing 9
3.14 PD69200 I2C Address Selection 10
4 Electrical Specifications 11
4.1 PD69200 Electrical Characteristics and Features 11
4.2 PD69208M Electrical Characteristics 12
4.2.1 Electrical Characteristics 12
4.2.2 Detection 13
4.2.3 Classification 13
4.2.4 Port Real Time Protection 14
4.2.5 Port Current Monitoring 15

4.2.6 Port Voltage Monitoring 15
4.2.7 Main Voltage Monitoring 15
4.2.8 Temperature Monitoring 16
4.2.9 Digital Interface 16
4.2.10 Immunity 16
4.3 Absolute Maximum Ratings 17

5 Pin Descriptions 18
5.1 Pin Configuration and Pinout 18
5.2 PD69200 and PD69208M Pin Descriptions 20
5.2.1 PD69200 Pin Descriptions 20
5.2.2 PD69208M Pin Descriptions 23
5.3 Recommended PCB Layouts 25
5.3.1 PD69200 Recommended PCB Layout for 32-Pin QFN 5 mm x 5 mm 25
5.3.2 PD69208M Recommended PCB Layout for 56-Pin QFN 8 mm x 8 mm 27

6 Package Specification 32
6.1 Thermal Specifications 34
6.2 Recommended Solder Reflow 35
6.3 Tape and Reel 36
6.3.1 PD69200 Tape and Reel Specification 36
6.3.2 PD69208M Tape and Reel Specification 37
6.4 Reference Documents 40

7 Application Information 41
7.1 PD Detection 41
7.2 Legacy (Reduced Capacitor) Detection 41
7.3 Classification 41
7.4 Port Start-Up 42
7.5 Over-Load Detection and Port Shut Down 42
7.6 Disconnect Detection 42
7.7 IC Thermal Monitoring 42
7.8 Over-Temperature Protection 43
7.9 V MAIN Out of Range Protection 43
7.10 2-Pair and 4-Pair Ports 43
7.11 Power Management 43
7.12 Port Power Limit 43
7.13 Reset Pin 43
7.14 System OK Indication 43
7.15 Interrupt Pin 44
7.16 Port Matrix Control 44
7.17 Power Good Interrupt 44
7.18 LED Stream 44

7.19 Power Sequencing 45

8 Ordering Information 46

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Revision 6.0 of this document was published in September 2019. The following is a summary of the changes.

- Features (see page 4) list was updated.
- Typical PoE Application (see page 5) figure and note were updated.
- Fast PoE and Perpetual PoE were added to PD69200 Features Description (see page 11) table.
- Max accuracy value was updated in PD69208M Main Voltage Monitoring (see page 15) table.
- PD69208M Pin Diagram (see page 19), PD69200 Top-Layer Copper PCB Layout (see page 25), and PD69200 Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array (see page 26) figures were updated.
- Typical Θ_{JB} value was updated in PD69208M Thermal Specifications (see page 34) table.
- Typical IEEE802.3bt Port PoE Voltage Diagram (see page 42) was updated.
- Ordering Information (see page 46) was updated.

1.2 Revision 5.0

Revision 5.0 of this document was published in November 2018. The following was a summary of the changes.

- Updated the Features and Applications details.
- Port real time protection details are updated for I_{PORT}, I_{LIM}, I_{CUT}, I_{UDL}, P_{PWR}, and T_{MPS}.
- Port current monitoring information is updated for accuracy.
- Main voltage information is updated for accuracy.
- The PD69200 pin diagram is updated.
- The Top-Layer Pin Geometry measurement is updated.
- The PD692000 Thermal Specifications table is added.
- The company name Freescale is replaced with NXP across the document.
- Updated Figures 8 - 12.
- Added table footnotes for D, VVVV, and SS.

1.3 Revision 4.0

Revision 4.0 of this document was published in February 2018. The following was a summary of the changes.

- Preliminary designation was removed.
- Thermal specifications were updated.
- The tape specification was updated.
- Tape mechanical data was added.
- Ordering part numbers were updated.

1.4 Revision 3.0

Revision 3.0 of this document was published in November 2017. The following was a summary of the changes.

- Maximum storage temperature value is no longer preliminary.
- The link to stencil and via plug recommendations was updated.
- Application information was updated.
- Maximum slew rate requirement of 100 mS was added.
- Manufacturing and ordering part number information was updated.
- Updated revision 2.0 history to include entry for the redefinition of quiescent current in terms of port threshold.

1.5 Revision 2.0

Revision 2.0 of this document was published in September 2017. The following was a summary of the changes.

- Updated the recommended PCB layout for better manufacturability.
- Redefined quiescent current in terms of port threshold.
- Added the PD69208M Manufacturing and Ordering Part Numbers table.
- Added a note about I^2C communication configuration.
- Added table footnotes for ESD (HBM and CDM).
- Updated the main voltage monitoring table for accuracy data.
- Updated the Peak Classification Temperature (TP).
- Updated the description for pin 24 for PD69200.
- Updated the description for pin 19 for PD69208M.
- Updated the thermal specifications table.
- Changed the notation from V_{PORT_NEGx} to V_{PORT}.
- Added a footnote for Absolute Storage Temperature in the table.
- Updated the accuracy values in the Port Current Monitoring table.
- Updated the R_{SIG_LOW} and R_{SIG_HIGH} values in the Detection table.
- Updated the LSB value in the Temperature Monitoring table.
- Updated the values for D11, D12, D15, D16, and D17 in the SPI Timing Diagram Description table.

1.6 Revision 1.2

Revision 1.2 of this document was published in August 2016. The following was a summary of the changes.

- According to PCN155881, qualification of UTAC Thailand assembly for PD6920X. Parts from UTAC will be identified by different marking that was added.
- Match 802.3af ILIM and I_{INRUSH} levels to IEEE standard levels.
- Match 802.3at ILIM low level to IEEE standard levels.

1.7 Revision 1.1

Revision 1.1 of this document was published in July 2016. The following was a summary of the changes.

- Updated the feature's list. Changed MSL1 of PD69208 to MSL3.
- Updated ordering information. Changed MSL1 of PD69208 to MSL3.

1.8 Revision 1.0

Revision 1.0 of this document was published in December 2015. This was the first publication.

2 Overview

Microsemi's PD69208M Power over Ethernet (PoE) manager IC integrates power, analog, and state-of-the-art logic into a single 56-pin, plastic QFN package. The device is used in Ethernet switches and Midspans to allow network devices to share power and data over the same cable. The PD69208M device is an 8-port, mixed-signal, and high-voltage PoE driver. Together with the PD69200 external MCU, it performs as a PSE system. Microsemi's PoE controller, PD69200, is a cost-effective, pre-programmed MCU designed to implement enhanced mode.

PD69208M/PD69200 chip-set supports PoE Powered Device (PD) detection, power-up, and protection according to IEEE standards, as well as legacy/pre-standard PD detection. It provides PD real-time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit, and enables operation in a standalone mode. It also executes all real-time functions as specified in IEEE802.3at and IEEE802.3bt Class 3.

PD69208M supports supply voltages between 32 V and 57 V without additional power supply sources. A system that powers over four pairs can be implemented by combining two ports of PD69208M, enabling an extra feature for a simple and low-cost, high-power PD device. Ongoing monitoring of system parameters for the host software is available via communication. Internal thermal protection is implemented in the chip. PD69208M is a low-power dissipation device that uses internal MOSFETs and internal 100 mΩ sense resistors.

PD69200 features an ESPI bus for all PD69208M. It is developed based on NXP Kinetis_L family, MKL15Z128VFM4, that is embedded with the ARM Cortex™-M0+ core. It also uses I^2C or UART interface to the host CPU, and is designed to support software field upgradable through the communication interface.

PD69208M is available in a 56-pin, 8 mm × 8 mm QFN package. PD69200 is available in 32-pin, 5 mm × 5 mm QFN package.

2.1 Features

- 8 independent channels
- Complies with IEEE802.3af-2003, IEEE802.3at-2009 (including two-event classification), and IEEE802.3bt
- Supports Fast PoE
- Supports Perpetual PoE
- Drives 2-pair power ports or 4-pair ports
- Supports pre-standard PD detection
- Single DC voltage input (32 V to 57 V)
- Built-in 3.3 V and 5 V regulators
- Input voltage out of range protection
- Wide ambient temperature range: –40 °C to 85 °C
- On-chip over-temperature thermal protection and monitoring
- Low-power dissipation (0.1 Ω sense resistor and 0.2 Ω MOSFET Rdson per channel)
- Includes Reset command pin
- 4× direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- Configurable PSE AT/AF/BT-Type3 modes
- Power soft start mechanism
- Voltage monitoring/protection
- Internal power on reset
- Emergency power management supporting four configurable power bank I/Os
- Advance System Power Management algorithm supports up to 96 physical ports
- Can be cascaded to up to 12 PoE devices (96 ports)
- Supports both UART and I^2C interfaces to host CPU
- Backwards compatible with Microsemi communication protocol used at prior generations
- LED stream support
- System OK indication
- Software download via I^2C or UART
- Detailed port status
- Programmable threshold temperature alarm limit
- Interrupt out pin for system and port events
- Forced port power ON function
- Port power limit setting
- Port matrix and priority
- Automatic PoE device type detection
- MSL3, RoHS compliant

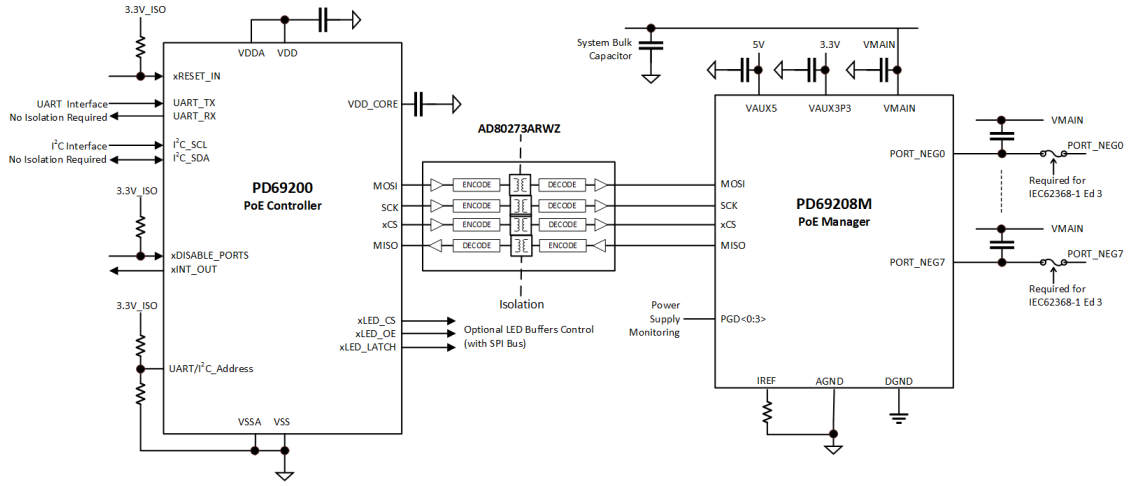
2.2 Applications

- Power over Ethernet (all IEEE compliant 2-pair modes)
- Supports 4-pair and IEEE802.3bt PSE Type 3
- Switches/Routers/Midspans
- Industrial automation
- PoE for LED lighting

2.3 Typical PoE Application

The following figure illustrates the typical PoE application of PD69208M and PD69200 devices.

Figure 1 • Typical PoE Application



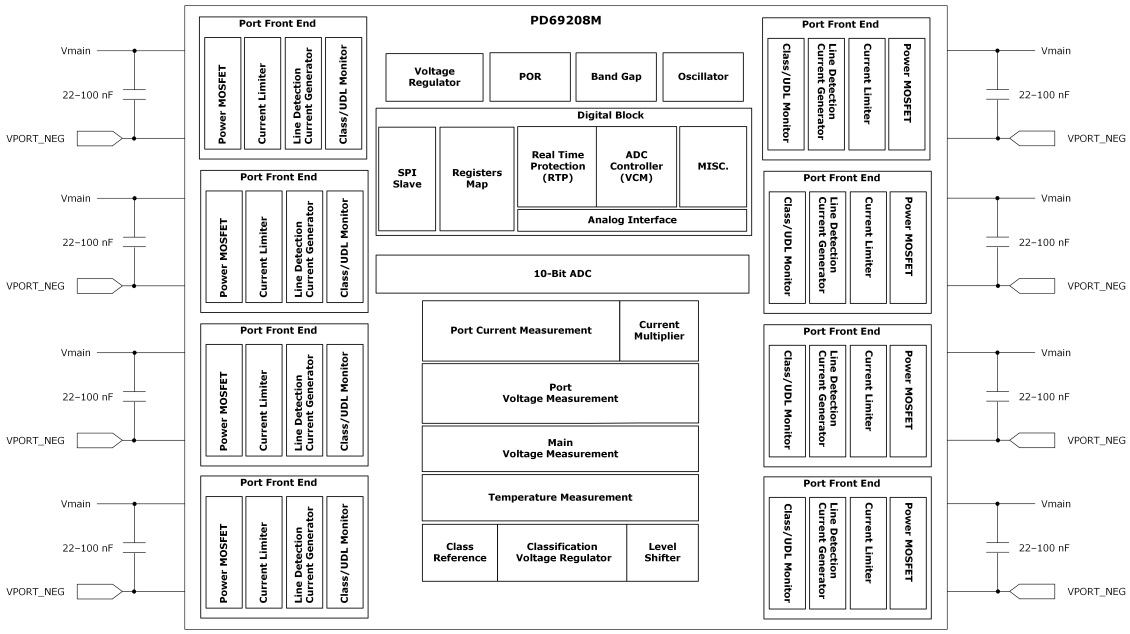
Note: For complete reference design, see Microsemi AN211 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System (Document Number: PD-000300282).

Fuses per port are not required for use in circuits with a total power level of up to 3 kW. This is because PD69208 is a UL 2367 (category QVRQ2) recognized component and fulfills limited power source (LPS) requirements of the latest editions of IEC60950-1 and EN60950-1. However, IEC62368-1 Ed 3 (released in October 2018 and becomes effective December 2020) requires per-port fuses for a system power supply greater than 250 W.

3 Functional Descriptions

The following illustration shows the functional blocks of PD69208M.

Figure 2 • PD69208M Block Diagram



The following sections describe the functional blocks of PD69208M.

3.1 Digital Block Module

The logic main control block includes digital timing mechanisms and state machines synchronizing and activating PoE functions according to PD69200 control commands, such as:

- Real Time Protection (RTP)
- Start Up Macro (DVDT)
- Load Signature Detection (RES DET)
- Classification Macro (CLASS)
- Voltage and Current Monitoring (VCM)
- ADC Interfacing
- Direct Digital Signals with Analog Block
- SPI Communication Block
- Registers

3.2 PD Detection Generator

Upon request from PD69200 to main control module, the PD detection generator generates four different voltage levels to ensure a robust AF/AT/BT PD detection functionality.

3.3 Classification Generator

Upon request from PD69200 to main control module, the state machine applies a regulated class event and mark event voltage to ports, as required by IEEE standards.

3.4 Current Limiter

This circuit continuously monitors the current of powered ports and limits the current to a pre-defined value set by AF/AT. When the current value exceeds this specific value, the system starts measuring the elapsed timing. If this interval is greater than a preset threshold, the port is disconnected.

3.5 Main Power MOSFET

Main power switching FET is used to control PoE current into the load.

3.6 Analog to Digital Converter

A 10-bit analog to digital converter (ADC) is used to convert analog signals into digital registers for the logic control module.

3.7 Power on Reset

Power on reset (PoR) monitors the internal 3.3 V and 5 V DC levels. If this voltage drops down below the specified threshold limit, a reset signal is generated and PD69208M is reset.

3.8 Voltage Regulator

The voltage regulator generates 3.3 V and 5 V for internal circuitry. These voltages are derived from V_{MAIN} supply. Connect the following to use the internal voltage regulator:

- V_{AUX5} to DRV_VAUX5
- V_{AUX3P3} to VAUX3P3_INT

The following three options reduce PD69208M power dissipation by regulating the voltage outside the chip:

- Use an external NPN transistor to regulate the 5 V. In this setup, the configuration of regulator pins should be as follows:
  - DRV_VAUX5 is connected to NPN BASE
  - V_{AUX5} is connected to NPN EMITTER (Connect Collector to V_{MAIN})
  - V_{AUX3P3} is connected to V_{AUX3P3_INT}
- Supply PD69208M with an external 5 V regulator. In this setup, regulator pins configuration should be as follows:
  - V_{AUX3P3} is connected to V_{AUX3P3_INT}
  - DRV_VAUX5 is not connected (left open)
  - V_{AUX5} is connected to external 5 V
- Supply PD69208M with an external 3.3 V regulator. In this setup, regulator pins configuration should be as follows:
  - V_{AUX5} is connected to DRV_VAUX5
  - V_{AUX3P3_INT} is not connected (left open)
  - V_{AUX3P3} is connected to external 3.3 V

These options can be implemented simultaneously to reduce PD69208M power dissipation.

3.9 Clock

PD69208M clock (CLK) is an internal 8 MHz clock oscillator.

3.10 SPI Communication

PD69208M uses SPI communication in SPI slave mode to communicate with the PD69200 MCU. Each PD69208M has an address determined by ADDR0-ADDR3 pins. The PD69200 can support up to 12 ICs. The actual frequency between PD69200 and PD69208M ICs is 1 MHz.

The following table lists the SPI communication packet structure.

Table 1 • SPI Communication: Packet Structure

Control Byte Selects PD69208M According to the Address	R/W Bit	Internal Register Address	Number of Words (Only in Read Access)	Data Written to IC (in Write Access) Read from IC (in Read Access)
8 bits	R(0)/W(1)	8 bits	8 bits	16 bits

3.11 PD69208M SPI Addressing

PD69208M operates in 8-bit address and 16-bit data. It responds to SPI transaction if the first SPI byte (IC address byte bits[7:1]) complies with the following:

Table 2 • SPI Addressing

3 Bits (Bit 7:5)	4 Bits (Bit 4:1)	1 Bit (Bit 0)
000	Address Input Pin	Read/Write

3.12 Broadcast

- A broadcast command is intended to instruct all connected PD69208M ICs to perform a specific operation.
- The broadcast command is a write command with the standard packet structure. In case of a broadcast read operation, the read data is not valid and the read operation has no impact.

Table 3 • Broadcast

3 Bits (Bit 7:5)	4 Bits (Bit 4:1)	1 Bit (Bit 0)
001	0000	Write

3.13 SPI Timing

Figure 3 • SPI Timing Diagram

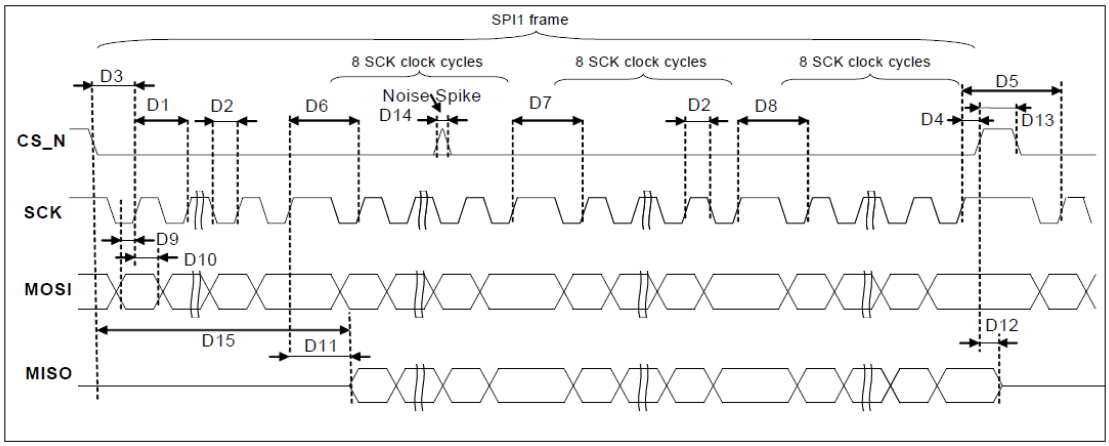


Table 4 • SPI Timing Diagram Description

Name	Min Delay	Max Delay	Description
D1	910 ns		SPI clock period
D2	45%	55%	SPI duty cycle
D3	340 ns		SPI_CS setup to SPI clock positive edge (delay after SPI_CS active signal)
D4	340 ns		SPI_CS hold to SPI clock positive edge (delay before SPI_CS inactive signal)
D5	2 SPI clock cycles		Delay between the last SCK in eSPI1 frame and first SCK at adjacent eSPI1 frame
D6	1 SPI clock cycles		Between byte 0 (IC address) and byte 1 (address)
D7	1 SPI clock cycles		Between byte 1 (address) and byte 2 (data)
D8	1 SPI clock cycles		Between byte 2 (MS data byte) and byte 3 (LS data byte)
D9	340 ns		MOSI setup time
D10	340 ns		MOSI hold time
D11		700 ns	MISO tri-state to valid data from clock positive edge
D12		700 ns	MISO valid data to tri-state from SPI_CS positive edge
D13	1 SPI clock cycles		SPI_CS width (Delay eSPI1 frame to adjacent eSPI1 frame)
D14		60 ns	Filtered glitch width
D15		D3 + D11 + 24 SPI clock cycles	MISO tri-state from SPI_CS negative edge to valid data
D16	200 ns		MISO setup to SCK positive edge
D17	200 ns		MISO hold to SCK positive edge

3.14 PD69200 I2C Address Selection

The I²C interface between the host CPU and a specific PD69200 requires setting the PD69200 address. This is done by applying a specific voltage level to pin #22 (I2C_ADDR_MEAS), as listed in the following table.

Table 5 • I2C Address Selection

I2C_ADDR Voltage Level	I²C Address (Hexadecimal)
0.00 to 0.21 VDC	UART
0.21 to 0.41 VDC	0x4
0.41 to 0.62 VDC	0x8
0.62 to 0.83 VDC	0xC
0.83 to 1.03 VDC	0x10
1.03 to 1.24 VDC	0x14
1.24 to 1.44 VDC	0x18
1.44 to 1.65 VDC	0x1C
1.65 to 1.86 VDC	0x20
1.86 to 2.06 VDC	0x24
2.06 to 2.27 VDC	0x28
2.27 to 2.48 VDC	0x2C
2.48 to 2.68 VDC	0x30
2.68 to 2.89 VDC	0x34
2.89 to 3.09 VDC	0x38
3.09 to 3.30 VDC	0x3C

UART communications configuration:

- Bits per second: 19,200 bps
- Data bits: 8
- Parity: None
- Stop bits: 1
- Flow control: None

I²C communication configuration:

- Address: 7 bits
- Host should support clock stretch
- Transaction: 15 bytes or 1 byte

4 Electrical Specifications

The following sections describe the electrical characteristics of PD69208M and PD69200 devices.

4.1 PD69200 Electrical Characteristics and Features

In this application, PD69200 consumption is ~20 mA.

- Manufacturer: NXP
- Manufacturer part number: MKL15Z128VFM4
- Maximum pull-ups consumption based on PD69200 application is 2 mA. See the hardware application note (Catalog Number: PD69208_AN_211).

Table 6 • PD69200 Features Description

Features	Description
Supports up to 12 PoE devices: 96 physical ports (48 logical)	Up to 12 PoE devices can be cascaded, fitting into a 96-physical-port PoE system that uses one PoE controller (PD69200). PD69200 can support up to 48 logical ports. A logical port can be built from 2× physical ports or 1× physical port.
Power management	The system supports three power management modes: Class (LLDP), Dynamic, and Static.
Threshold configuration	Over-voltage and under-voltage thresholds can be configured for disconnection purposes.
Fast PoE	Ability of a system to quickly boot and power-up ports without loading EEPROM firmware.
Perpetual PoE	Ability of a PoE system to maintain PoE power while switch host firmware is being loaded.
High-power ports, 2-pair or 4-pair	PoE devices can be configured (both hardware and software) to enable higher current through ports (up to ~627 mA) or double power at the RJ in case of 4 pairs.
Communication	Supports both I^2C and UART interfaces with host CPU.
Legacy (reduced capacitance) detection	Enables detection and powering of pre-standard devices (PDs) up to 30 uF.
LED stream	Provides a direct SPI interface to an external LED stream circuitry. Enables designers to implement a simple LED circuit that does not require a software code. LED stream clock frequency is 1 MHz.
System OK indication	Provides a digital output pin to host. System validity indication, when system OK pin state is low. This output behavior is controlled by software mask register settings (Mask 0×28). The mask default settings is 0, meaning that this pin indicates valid software and V_{MAIN} is in range. This pin is active low. For more information, see the Serial Communication Protocol User Guide document (Catalog Number: PD69200_UG_COMM_PROT).
System and port measurements	Measurements of the following parameters: Current (mA), Power Consumption (W), V_{MAIN} (V), Port Voltage (V), and PD Class (0–4).
Detailed port status	Port statuses are received from PoE managers. Statuses such as port on and port off due to disconnection or due to overload.
Interrupt pin	Interrupt out from PoE controller (PD69200) indicating events such as: port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events, see the Serial Communication Protocol User Guide document (Catalog Number: PD69200_UG_COMM_PROT).
Port power limit	Configurable port power limit; when a port exceeds the limit, it is automatically disconnected.
Port matrix control	Enables layout designers to connect all physical ports to logical ports as required.
"Power Good" interrupt from power supply directly to POE drivers	For systems comprising more than a single power supply, when one power supply fails, a fast port disconnection mechanism is executed to maintain operation and prevent collapse of other power supplies.

4.2 PD69208M Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated in the following table apply to the entire specified operating ratings of the device. Typ values stated are either by design or by production testing at 25 °C ambient.

4.2.1 Electrical Characteristics

Table 7 • Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{MAIN}	Main supply voltage	Supports Full IEEE802.3 AF and AT functionality	32		57	V
V_{PORT}	Port output	$V_{MAIN} – V_{PORT\_NEGx}$	0		57	V
V_{TH}	POR threshold	Internal or External 3.3 V supply		8		V
I_{MAIN}		Main power supply current at operating mode.V_{MAIN} = 55 V		14		mA
V_{AUX5}	5 V output voltage	V_{AUX5}–AGND	4.5	5	5.5	V
V_{AUX3P3}	3.3 V output voltage	V_{AUX3P3}–AGND	3	3.3	3.6	V
I_{AUX3P3}	3.3 V output current for application use	Without external NPN			5	mA
		With external NPN transistor on V_{AUX5}			30	mA
V_{AUX3P3_IN}	3.3 V input voltage	V_{AUX3P3}-AGND	3	3.3	3.6	V
DV_{DD}	Digital 3.3 V input voltage	DV_{DD}-DGND	3	3.3	3.6	V
POR_{TP}	Power-on reset DV_{DD} trip point	DV_{DD}-DGND	2.575	2.775	2.975	V
POR_{HYS}	Power-on reset DV_{DD} hysteresis	POR_{TP}-DGND	0.2	0.25	0.3	V
R_{CH_ON}	Total channel resistance	$R_{ds\_on} + R_{sense} + R_{bonding}$		0.34		Ω

4.2.2 Detection

Table 8 • PD69208M Detection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OC}	Pre-detection voltage, open circuit voltage	$V_{MAIN} – V_{PORT\_NEGx}$, open port			7.8	V
V_{VALID}	Detection voltage	$V_{MAIN} – V_{PORT\_NEGx}$, for IEEE802.3 compliant signature resistance (R_{SIG} < 33 K)			9.3	V
I_{SC}	Short circuit current	$V_{MAIN} – V_{PORT\_NEGx}$ = 0 V		388	408	µA
R_{SIG_LOW}	Minimum valid detection resistance		15		19	KΩ
R_{SIG_HIGH}	Maximum valid detection resistance		26.5		33	KΩ

4.2.3 Classification

Table 9 • PD69208M Classification

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{CLASS}	Class event output voltage	$V_{MAIN} – V_{PORT\_NEGx}$; 0 mA ≤ I_{PORT} ≤ 50 mA	15.5	18	20.5	V
V_{MARK}	Mark event output voltage	$V_{MAIN} – V_{PORT\_NEGx}$; 0.1 mA ≤ I_{PORT} ≤ 5 mA	7	8.5	10	V
I_{CLASS_LIM}	Class event current limitation	$V_{MAIN} – V_{PORT\_NEGx}$ = 0 V	51	70	100	mA
I_{MARK_LIM}	Mark event current limitation	$V_{MAIN} – V_{PORT\_NEGx}$ = 0 V	51	70	100	mA
	Classification current thresholds	Class 0	0		5	mA
		Class 1	8		13	mA
		Class 2	16		21	mA
		Class 3	25		31	mA
		Class 4	35		45	mA
		Class error	51		100	mA

4.2.4 Port Real Time Protection

Table 10 • PD69208M Port Real Time Protection

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{RISE}	Turn on rise time	From 10% to 90% of the voltage difference at the V_{PORT_NEGx} in POWER_ON state from the beginning of POWER_UP	15			µs
I_{INRUSH}	Output current in POWER_UP state	C_{LOAD} ≤ 180 µF[1]	400	425	450	mA
T_{INRUSH}	Inrush time				65	ms
I_{PORT}	Output operating current	802.3af	10		360	mA
		802.3at	10		620	mA
		802.3bt class 5	10		560	mA
		802.3bt class 6	10		692	mA
I_{CUT}	Overload current	802.3af		375		mA
		802.3at		645		mA
		802.3bt class 5		589		mA
		802.3bt class 6		709		mA
T_{CUT}	Overload time limit		62	64	66	ms
I_{LIM}	Port current limit	802.3af	400	425	450	mA
		802.3bt class 1–3	670	720	770	mA
		802.3at, 802.3bt class 4–6	790	850	892	mA
T_{LIM}	Port current limit time	$V_{MAIN} - V_{PORT\_NEGx}$ < 30 V	1	2	3	ms
P_{PWR}	Port power accuracy	> 90 W			2	%
I_{UDL}	DC disconnect	2 Pairs	6	7.5	9	mA
	Under-load current	4 Pairs (for each pair-set)	2	2.5	3	mA
T_{MPDO}	PD maintain power signature dropout time limit		322	324	326	ms
T_{MPS}	PD maintain power	802.3bt PSE type 1, 2	46	48	50	ms
	Signature time for validity	802.3bt PSE type 3, 4	3	4	5	ms
T_{OFF}	Turn off time	From V_{MAIN} to 2.8 V			500	ms

1. Can be overridden by communication command.

4.2.5 Port Current Monitoring

Table 11 • PD69208M Port Current Monitoring

Symbol	Conditions	Typ	Max	Units
Resolution	Reported as 14 bits	10		Bits
LSB		122.07		µA
Measurement period		16		ms
Accuracy	50 mA < I_{PORT} < 150 mA		9	%
	150 mA < I_{PORT} < 350 mA		4.5	%
	350 mA < I_{PORT} < 600 mA		3.5	%
	I_{PORT} > 600 mA		3.0	%

4.2.6 Port Voltage Monitoring

Table 12 • Port Voltage Monitoring

Symbol	Typ	Max	Units
Resolution	10		Bits
LSB	58.6		mV
Measurement period	3		ms
Accuracy		3.3	%

4.2.7 Main Voltage Monitoring

Table 13 • PD69208M Main Voltage Monitoring

Symbol	Conditions	Typ	Max	Units
Resolution		10		Bits
LSB		58.6		mV
Measurement period		3		ms
Accuracy	42 V < V_{MAIN} < 50 V		2.1	%
	50 V < V_{MAIN} < 57 V		1.5	%
	50 V < V_{MAIN} < 57 V[1]		0.6	%

1. 0–70 °C

4.2.8 Temperature Monitoring

Table 14 • PD69208M Temperature Monitoring

Symbol	Conditions	Min	Typ	Max	Units
Resolution			8		Bits
LSB	Temperature = (DATA x 1.9384) – 273		1.9384		°C
Measurement period			3		ms
Accuracy		-3		3	°C

4.2.9 Digital Interface

Table 15 • PD69208M Digital Interface

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	Input logic high voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	2.2			V
V_{IL}	Input logic low voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]			0.8	V
Hyst	Input logic hysteresis voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	0.4	0.6	0.8	V
I_{IH}	Input logic high current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	–10		10	µA
I_{IL}	Input logic low current	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3]	–10		10	µA
V_{OH}	Output logic high voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = –1 mA	2.4			V
V_{OL}	Output logic low voltage	RESET_N, MOSI, MISO, SCK, CS_N, PGD[0..3], ADDR[0..3] I_{OH} = 1 mA			0.4	V

4.2.10 Immunity

Table 16 • PD69208M Immunity

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ESD	ESD rating	HBM[1]				
		CDM[2]				
Surge	Lightning surge[3]	EN61000 4-5	–1		1	KV

1. ESD HBM complies with JESD22 Class 2 standard.
2. ESD CDM complies with JESD22 Class 1 standard.
3. System-level common mode 10/700 µS according to IEC61000-4-5.

4.3 Absolute Maximum Ratings

PoE performance is not guaranteed when exceeding the recommended rating. Exposure to any stress in the range between the recommended rating, as listed in the following table, and the absolute maximum rating should be limited to a short time. Exceeding these ratings may impact long-term operating reliability.

Table 17 • Absolute Maximum Ratings

Parameters	Min	Max	Units
Supply input voltage (V_{MAIN})[1, 2]	–0.3	72	V
PORT_NEG[0.7] pins	–0.3	V_{MAIN} + 0.5	V
V_{AUX5}	–0.3	6	V
V_{AUX3P3}, D_{VDD}	–0.3	4	V
Digital pins: MISO, MOSI, SCK, CS_N, ADDR[3:0], PGD[3:0], RESET_N, TRIM	–0.3	D_{VDD} + 0.3 and <4.0	V
Junction temperature		150	°C
Lead soldering temperature (40 s, reflow)		260	°C
Storage temperature	–65	150	°C

1. Power Sequence Requirement: $V_{MAIN} > V_{AUX5} > V_{AUX3P3} = T_{RIM}, D_{VDD}$.
2. PD69208M EPAD is connected by copper plane on PCB to AGND. AGND is ground for IC.

Note: DRV_VAUX5 and IREF are output pins and should not apply voltage or current. DRV_VAUX5 can be left open when not used.

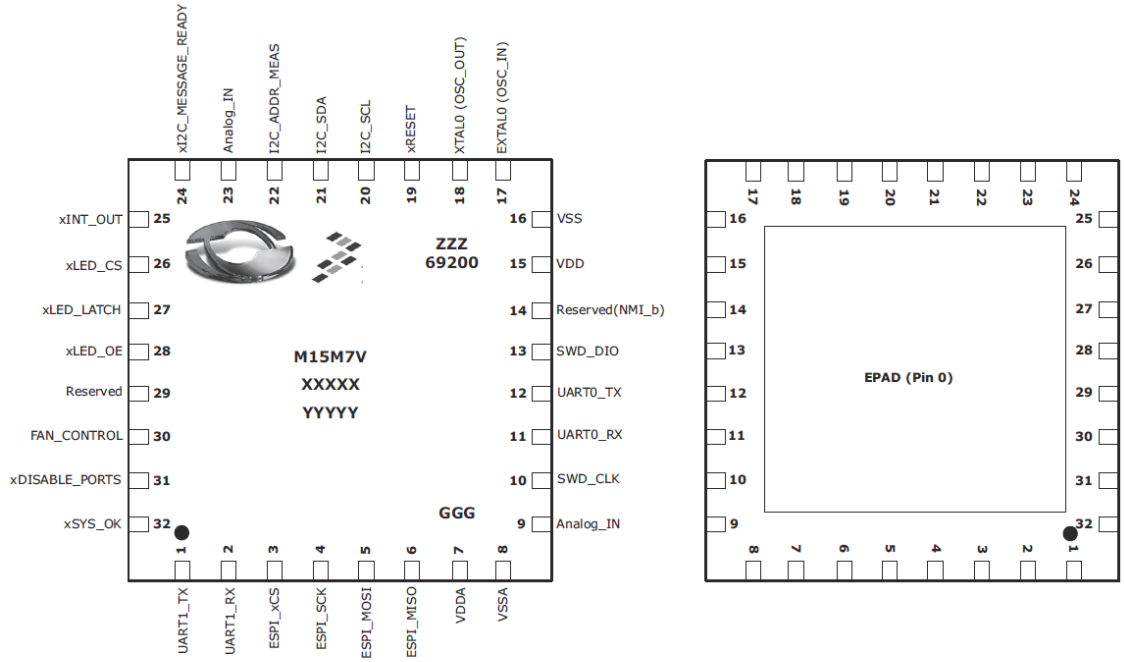
5 Pin Descriptions

The PD69200 device has 32 pins and PD69208M device has 56 pins, which are described in this section.

5.1 Pin Configuration and Pinout

The following figures represent the top and bottom view of PD69200 and PD69208M devices.

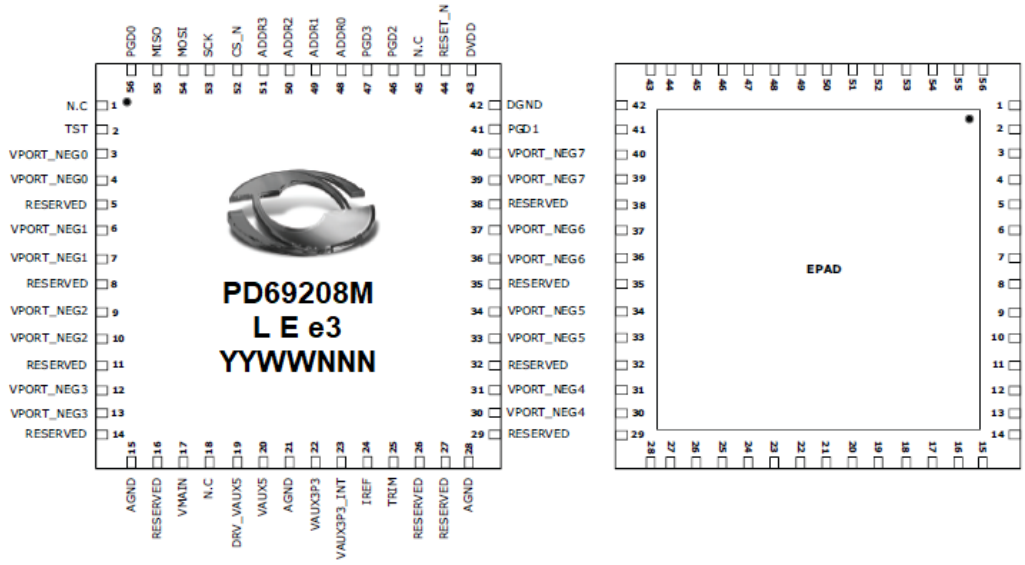
Figure 4 • PD69200 Pin Diagram



Note: The marking position of PD69200 may change subject to NXP practice.

Note: For definitions about markings in the PD69200 pinout diagram, see the Ordering Information (see page 46) table.

Figure 5 • PD69208M Pin Diagram



Note: For definitions about markings in the PD69208M pinout diagram, see the Ordering Information (see page 46) table.

5.2 PD69200 and PD69208M Pin Descriptions

The following sections describe the functional pin descriptions of PD69200 and PD69208M devices.

5.2.1 PD69200 Pin Descriptions

The following table lists the functional pin descriptions of the PD69200 device.

Table 18 • PD69200 Pin Description

Number	Designation	Type	Description
	EPAD	Thermal	Isolated Thermal PAD, recommended to tie to GND.
1	UART1_TX[1]	OUT	Reserved UART.
2	UART1_RX[1]	IN	Reserved UART.
3	ESPI_xCS	OUT	ESPI Bus to PoE Manager. SPI chip select (Active Low). CS is asserted during all SPI frame.
4	ESPI_SCK	OUT	ESPI Bus to PoE Manager. SPI clock output to PD6920x, and LED stream clock output, set to 1 MHz.
5	ESPI_MOSI	OUT	SPI packets are transmitted on this line.
6	ESPI_MISO	IN	ESPI Bus to PoE Manager. SPI Master In Slave Out. SPI packets are received on this line.
7	VDDA	Supply	Main Supply 3.3 V.
8	VSSA	GND	Analog ground.
9	Analog_IN	Analog_IN	Analog input. Should be connected to 3.3 V.
10	SWD_CLK	DEBUG	Serial Debug Data Bus Clock.
11	UART0_RX[1]	IN	UART receive from host. 15-byte protocol commands are received on this line. The baud rate is set to 19,200 bps. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69200_UG_COMM_PROT).
12	UART0_TX[1]	OUT	UART transmit to host. 15-byte protocol reply/telemetry are transmitted on this line. The baud rate is set to 19,200 bps. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69200_UG_COMM_PROT).
13	SWD_DIO	DEBUG	Serial Debug Data Bus.
14	Reserved (NMI_b)	IRQ_Input	Spare, an external pull-up must be connected.
15	VDD	Supply	Main Supply 3.3 V.
16	VSS	GND	Digital ground.
17	EXTAL0 (OSC_IN)[2]	Oscillator	Oscillator input - Reserved.
18	XTAL0 (OSC_OUT)[2]	Oscillator	Oscillator output - Reserved.

Number	Designation	Type	Description
19	xRESET[3,4]	IN/OUT	Host Reset input (Active Low). The shortest reset pulse from the host that is required for the PD69200 application is 150 µs. PD69200 can generate self-reset. In this case, the xRESET pin is driven low by the PD69200 for about 100 µs. It is recommended to connect this pin to a host open drain output with 10 KΩ pull-up. An 47 nF filter capacitor should be connected between this pin to GND, close to the PD69200 device. If this pin is connected to a push/pull driver, a serial resistor of 1.5 KΩ must be connected instead of the pull-up. The required shortest reset pulse in this case is 300 µs. For more information about this pin connectivity, see the Hardware Application Note (Catalog Number: PD69208_AN_211).
20	I2C0_SCL[4]	IN/OUT	I²C clock from the host master. Speed is limited to 400 KHz and clock stretching functionality must be implemented in the host master. If PD69200 is busy, it holds the clock line.
21	I2C0_SDA[4]	IN/OUT	I²C bidirectional data. 15-byte protocol messages are transmitted on this line. For more information, see the Serial Communication Protocol User Guide document (Catalog Number: PD69200_UG_COMM_PROT).
22	I2C_ADDR_MEAS	Analog_IN	I²C address of PD69200. Analog input to determine I²C address or UART operation. See I²C address selection in table I2C Address Selection (see page 10).
23	Analog_IN	Analog_IN	Reserved analog input. connect to GND.
24	xI2C_MESSAGE_READY[3]	OUT	I²C message ready for read by the host. PD69200 asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I2C read cycle only when the message is ready. This pin is active low. After the host reads the data from PD69200, this pin is asserted to high.
25	xINT_OUT[3, 4]	OUT	Interrupt output indication. This line is asserted low when a pre-configured event is in progress. The host configures the event that should generate an interrupt through 15 bytes protocol. When this event occurs, the xINT_OUT pin is asserted. This pin is active low.
26	xLED_CS[3]	OUT	Chip select signal for LED stream. This pin is active low.
27	xLED_LATCH[3]	OUT	Latch signal for LED stream. This pin is active low.
28	xLED_OE[3]	OUT	Output enable signal for LED stream. This pin is active low.
29	Reserved	IN	Reserved for MPRPD counter for future support. If not used, connect to VDD.
30	FAN_CONTROL	OUT	Optional. Fan control operates a fan, when the PD69208M device temperature is above the temperature alarm threshold. This pin is active high.
31	xDISABLE_PORTS[3]	IN	Disable all PoE ports. When this input is asserted low, the PD69200 device shuts down all of the PoE ports in the system. This pin contains software filter of 480 ms to reject noise and false disable scenarios.

Number	Designation	Type	Description
32	xSys_OK/LED System OK[3]	OUT	System validity indication. When the system is in OK state, the pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0x28). The mask default settings is 0, meaning that this pin indicates valid software, and V_{MAIN} is in range. This pin is active low. For more information, see the Serial Communication Protocol User Guide (Catalog Number: PD69200_UG_COMM_PROT).

1. A weak pull-up is recommended. See Hardware Application Note: PD69208_AN_240.
2. The oscillator pins are reserved and unused. The MCU uses internal clock source set to 47.972 MHz ±1.5% (max).
3. The initial x indicates that the pin is active low.
4. Open drain output requires an external pull-up. See Hardware Application Note: PD69208_AN_211.

Note: All I/Os in this application can sink or source 3 mA maximum.

5.2.2 PD69208M Pin Descriptions

The following sections describe the functional pin descriptions of PD69208M devices.

Table 19 • PD69208M Pin Description

Number	Designator	Type	Description
	EPAD		Exposed PAD: Connect to analog ground. A decent ground plane should be deployed around this pin as required. See the PD69208 Layout Design Guidelines in the hardware application note (Catalog Number: PD69208_AN_211).
1	N.C	N/A	Not connected. Do not connect externally (leave floating).
2	TST	Digital Input	Test pin for production use only. Keep connected to DGND.
3	VPORT_NEG0	Analog I/O	Negative port 0 output.
4	VPORT_NEG0	Analog I/O	Negative port 0 output.
5	RESERVED	N/A	Reserved pin. Do not connect externally.
6	VPORT_NEG1	Analog I/O	Negative port 1 output.
7	VPORT_NEG1	Analog I/O	Negative port 1 output.
8	RESERVED	N/A	Reserved pin. Do not connect externally.
9	VPORT_NEG2	Analog I/O	Negative port 2 output.
10	VPORT_NEG2	Analog I/O	Negative port 2 output.
11	RESERVED	N/A	Reserved pin. Do not connect externally.
12	VPORT_NEG3	Analog I/O	Negative port 3 output.
13	VPORT_NEG3	Analog I/O	Negative port 3 output.
14	RESERVED	N/A	Reserved pin. Do not connect externally.
15	AGND	Power	Analog ground.
16	RESERVED	N/A	Reserved pin. Do not connect externally.
17	V_{MAIN}	Power	Main high-voltage supply voltage. A low ESR 1 µF (or higher) bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low-resistance traces.
18	N.C	N/A	Not connected. Do not connect externally.
19	DRV_VAUX5	Power	Driven outputs for 5 V external regulation; if internal regulation is used, connect to pin 20. If an external NPN is used to regulate the voltage, connect this pin to Base. If an NPN is used, a 4.7 µF capacitor should be connected between this pin and AGND.
20	VAUX5	Power	Regulated 5 V output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. If an external NPN is used to regulate the voltage, connect this pin to the emitter. The collector should be connected to V_{MAIN}.
21	AGND	Power	Analog ground.
22	V_{AUX3P3}	Power	Regulated 3.3 V output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V regulator is used, connect it to this pin to supply the chip.
23	V_{AUX3P3_INT}	Power	Connected to V_{AUX3P3} (pin 22) if internal 3.3 V regulator is used. Leave unconnected (Floating) if external 3.3 V regulator is used.
24	I_{REF}	Analog Input	Reference resistor pin. Connect a 28.7 kΩ 1% resistor to AGND.

Number	Designator	Type	Description
25	TRIM	Test Input	Test Input pin; Keep connected to V_{AUX3P3}.
26	RESERVED	N/A	Reserved pin. Do not connect externally.
27	RESERVED	N/A	Reserved pin. Do not connect externally.
28	AGND	Power	Analog ground.
29	RESERVED	N/A	Reserved pin. Do not connect externally.
30	VPORT_NEG4	Analog I/O	Negative port 4 output.
31	VPORT_NEG4	Analog I/O	Negative port 4 output.
32	RESERVED	N/A	Reserved pin. Do not connect externally.
33	VPORT_NEG5	Analog I/O	Negative port 5 output.
34	VPORT_NEG5	Analog I/O	Negative port 5 output.
35	RESERVED	N/A	Reserved pin. Do not connect externally.
36	VPORT_NEG6	Analog I/O	Negative port 6 output.
37	VPORT_NEG6	Analog I/O	Negative port 6 output.
38	RESERVED	N/A	Reserved pin. Do not connect externally.
39	VPORT_NEG7	Analog I/O	Negative port 7 output.
40	VPORT_NEG7	Analog I/O	Negative port 7 output.
41	PGD1	Digital I/O	Power good input from the system power supply.
42	DGND	Power	Digital ground.
43	DV_{DD}	Power In	Regulated 3.3 V for digital circuitry. Connect voltage from pin V_{AUX3P3} or from external power supply source if used. A 1 µF or higher filtering capacitor should be connected between this pin and DGND.
44	RESET_N	Digital Input	Reset input—active low (0 = reset). An external 10 K pull-up resistor should be connected between this pin and DV_{DD}.
45	N.C.	N/A	Not connected. Do not connect externally.
46	PGD2	Digital Input	Power good input from the system power supply.
47	PGD3	Digital Input	Power good input from the system power supply.
48	ADDR0	Digital Input	SPI address bit 0 to set chip address.
49	ADDR1	Digital Input	SPI address bit 1 to set chip address.
50	ADDR2	Digital Input	SPI address bit 2 to set chip address.
51	ADDR3	Digital Input	SPI address bit 3 to set chip address.
52	CS_N	Digital Input	SPI bus and chip select.
53	SCK	Digital Input	SPI bus and serial clock Input.
54	MOSI	Digital Input	SPI bus and Master Data out/slave in.
55	MISO	Digital Output	SPI bus and Master Data in/slave out.
56	PGD0	Digital Input	Power good input from the system power supply.

5.3 Recommended PCB Layouts

This section describes the recommended PCB layouts for the PD69200 and PD69208M devices.

5.3.1 PD69200 Recommended PCB Layout for 32-Pin QFN 5 mm x 5 mm

The following figures illustrate the PCB layout pattern for PD69200. Units are in mm.

Figure 6 • PD69200 Top-Layer Copper PCB Layout

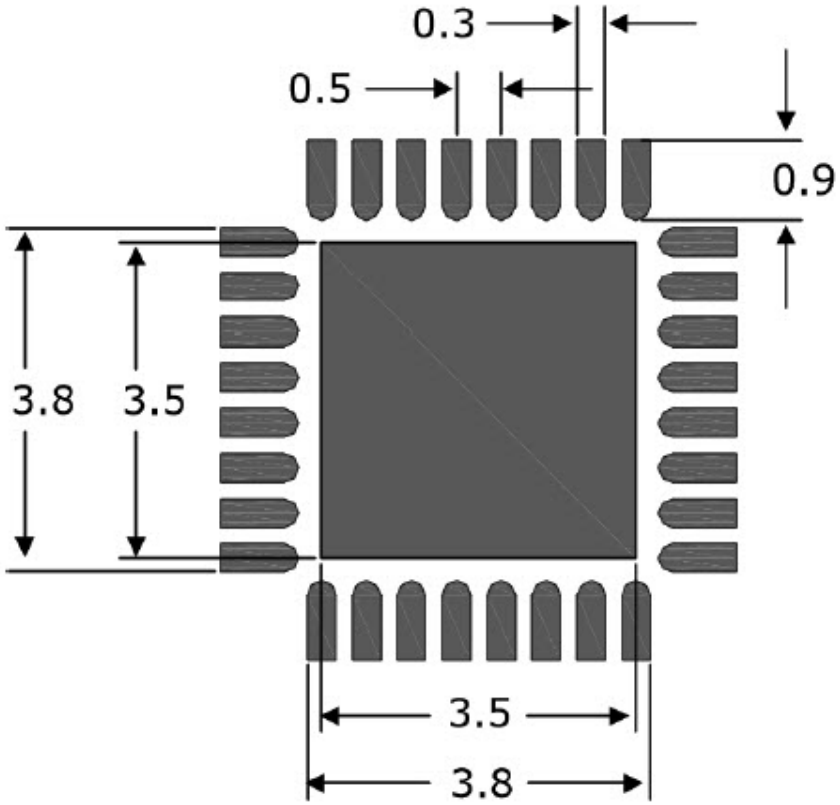
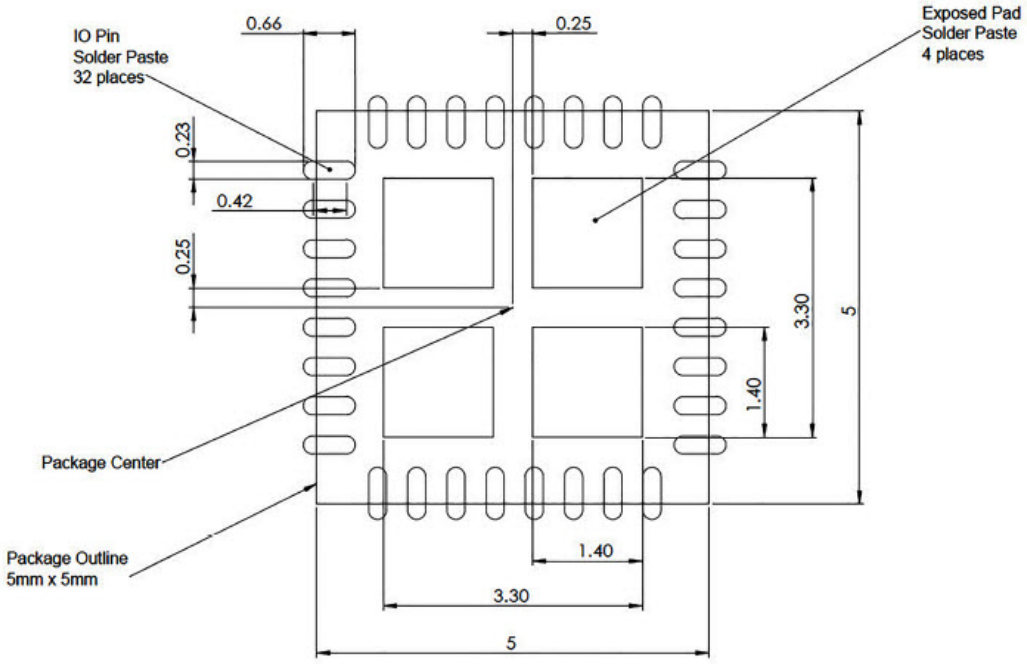


Figure 7 • PD69200 Top-Layer Solder Paste and Vias PCB Layout for Thermal Pad Array



5.3.2 PD69208M Recommended PCB Layout for 56-Pin QFN 8 mm x 8 mm

The following figures illustrate the PCB layout pattern for PD69208M. Units are in mm.

Figure 8 • Top Copper Layer

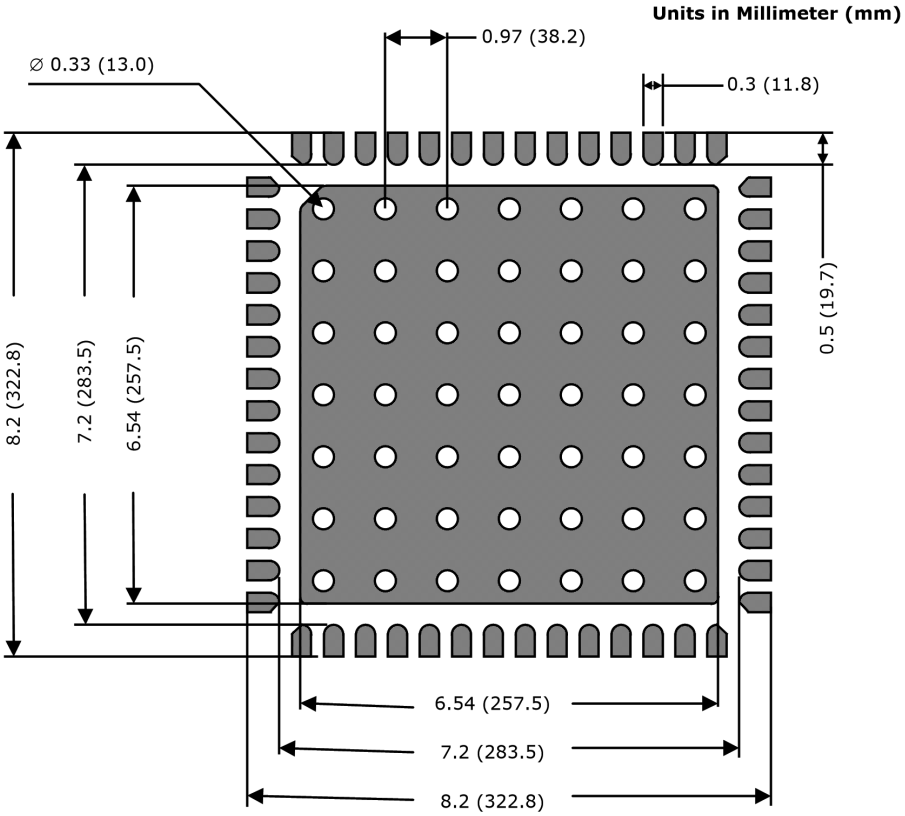


Figure 9 • Top Solder Paste Layer

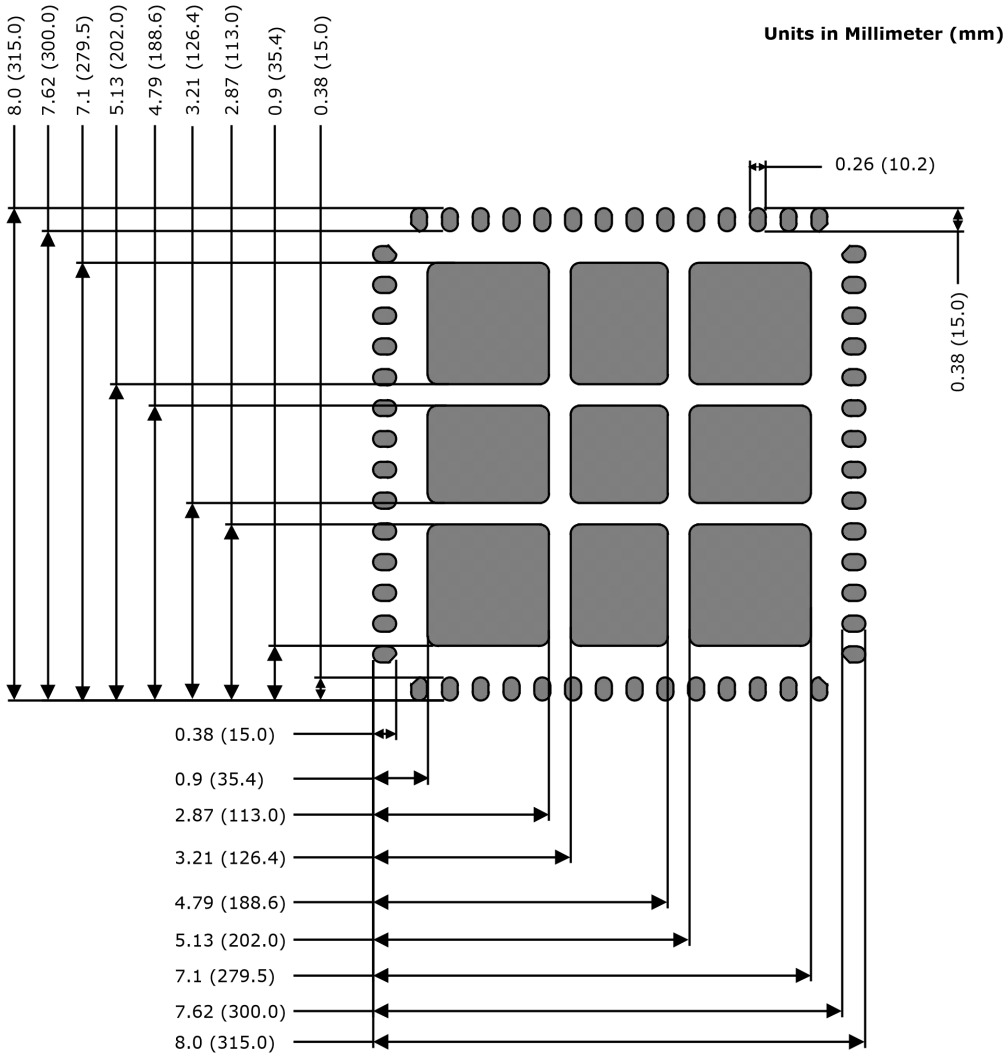


Figure 10 • Top Layer Mask

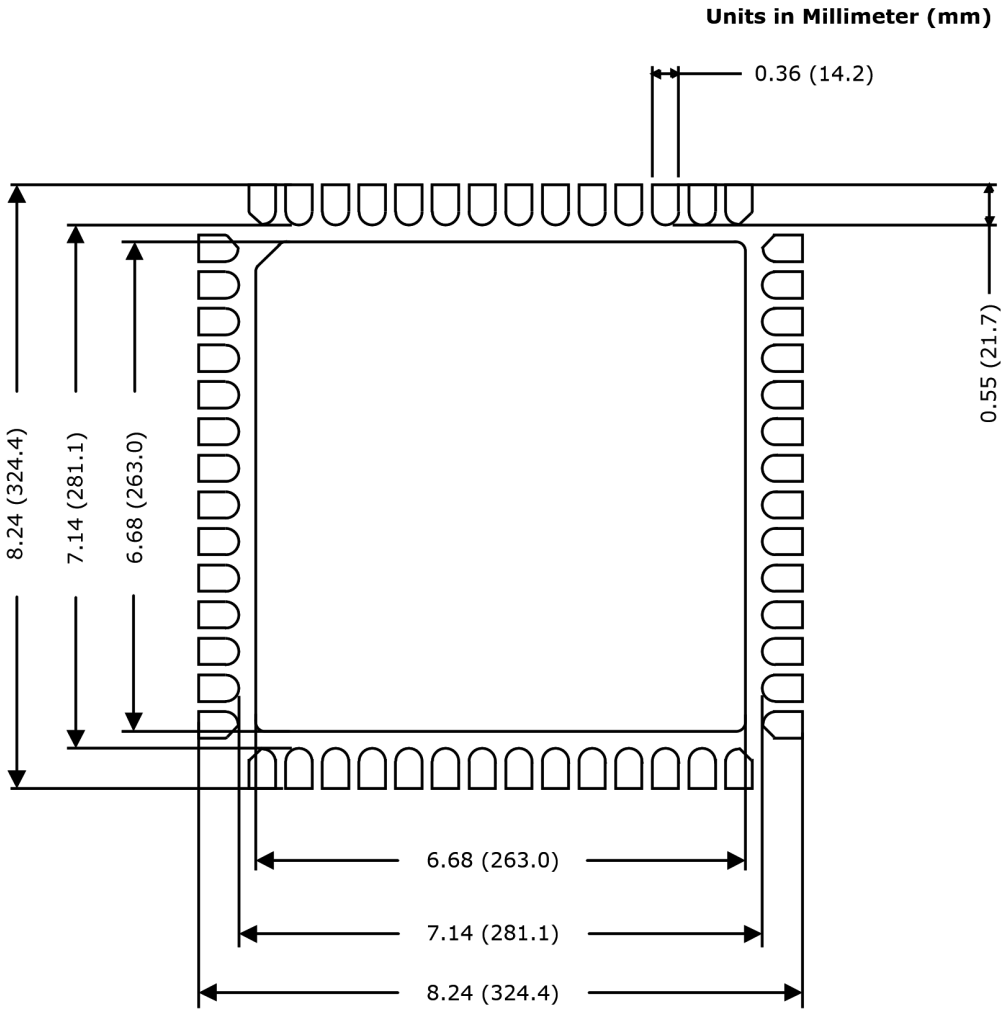


Figure 11 • BOT and Internal Layers Copper Plane

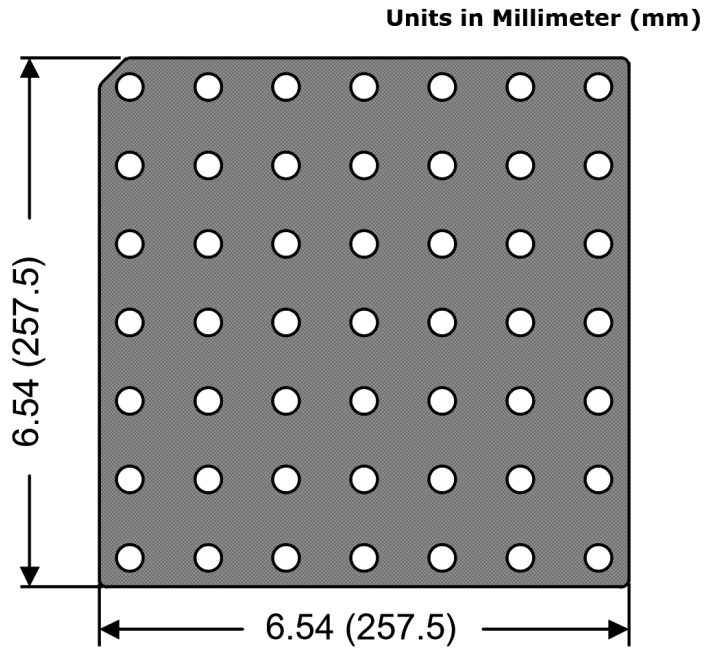
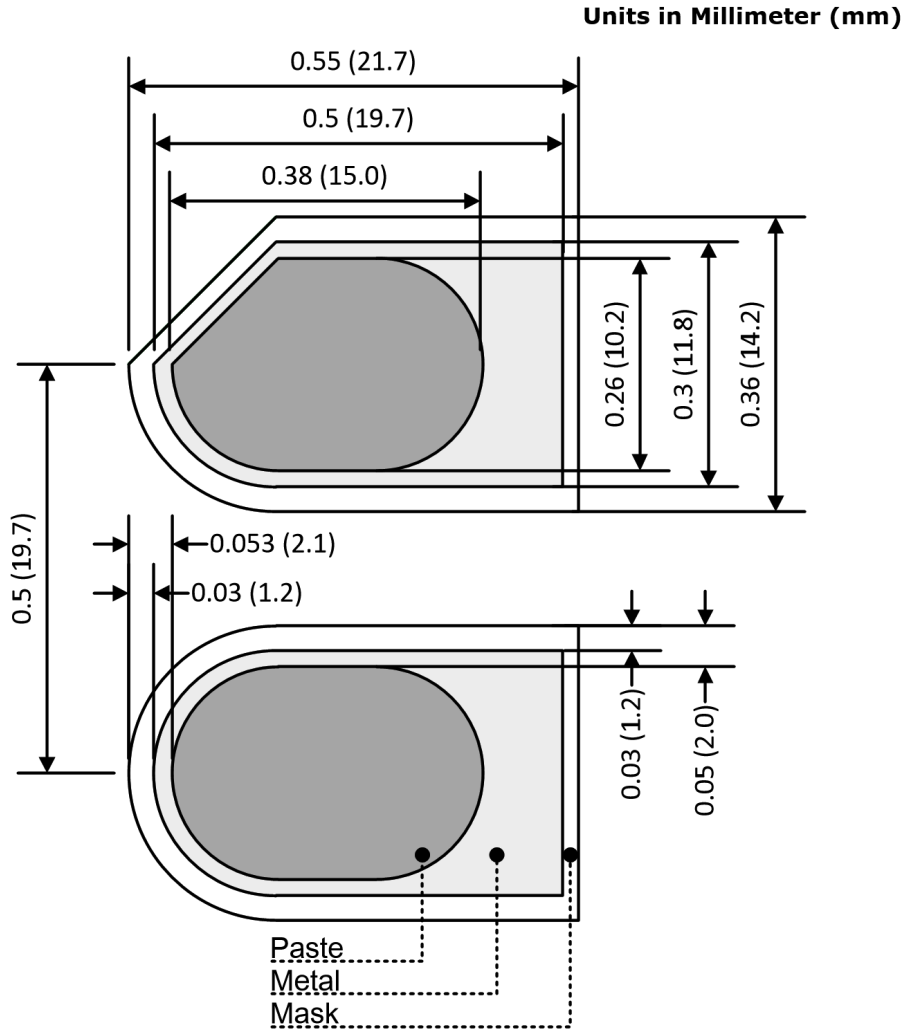


Figure 12 • Top Layer Pin Geometry

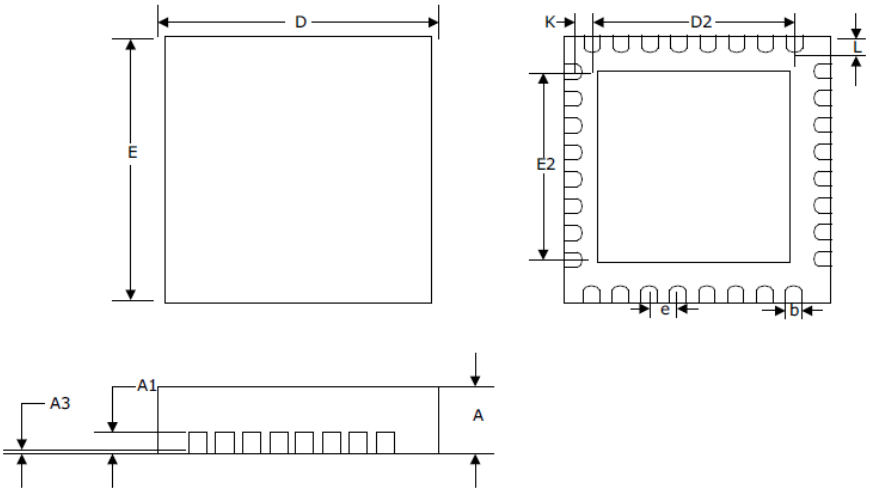


Note: The CM has latitude to modify the solder paste stencil for manufacturability reasons. The solder paste stencil shall cover 65% to 80% of the thermal pad and must not allow solder to be applied to the thermal vias under the QFN package using any method deemed appropriate. Any design should be subject to system validation and qualification prior to commitment to mass production of field deployment. Use a 5 mil stencil.

6 Package Specification

This section describes the package of PD69200 and PD69208M devices.

Figure 13 • PD69200 Package Outline Drawing (32-Pin QFN 5 mm x 5 mm)



The following table lists the dimensions and measurements of the PD69200 package.

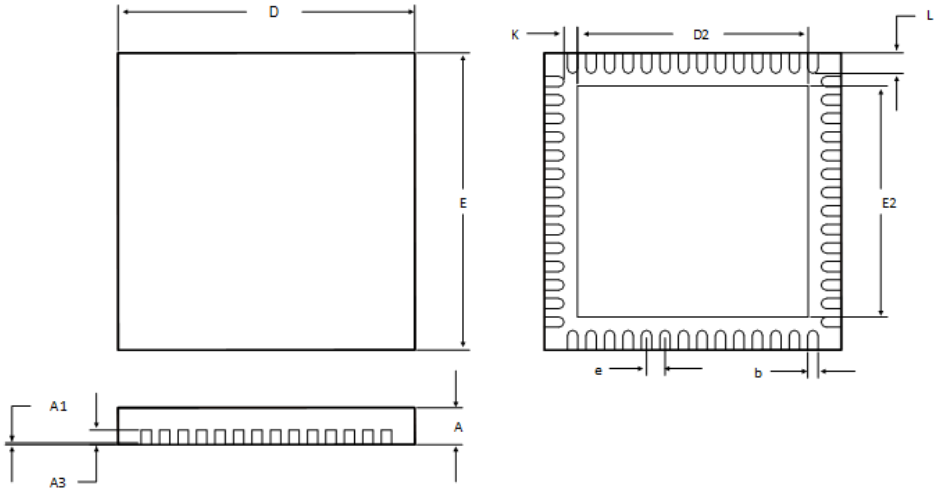
Table 20 • PD69200 Package Outline Dimensions and Measurements

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	3.50	3.70	0.138	0.147
E2	3.50	3.70	0.138	0.147
D	5.00 BSC		0.197 BSC	
E	5.00 BSC		0.197 BSC	

Note: Dimensions do not include protrusions; they should not exceed 0.155 mm (.006") on any side. Lead dimension should not include solder coverage. Dimensions are in millimeters and inches for reference.

The following figure illustrates the package drawing of the PD69208M package.

Figure 14 • PD69208M Package Drawing (56-Pin QFN 8 mm x 8 mm)



The following table lists the dimensions and measurements of the PD69208M package.

Table 21 • PD69208M Package Outline Dimensions and Measurements

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 REF		0.008 REF	
K	0.20 MIN		0.008 MIN	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.50	6.75	0.256	0.267
E2	6.50	6.75	0.256	0.267
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note: Dimensions do not include protrusions; they should not exceed 0.155 mm (0.006") on any side. Lead dimension should not include solder coverage. Dimensions are in millimeters and inches for reference.

6.1 Thermal Specifications

The following tables list the thermal specifications of PD69208M and PD69200.

Table 22 • PD69208M Thermal Specifications

Thermal Resistance	Typ	Units	Notes
θ_{JA}	19.0	°C/W	Junction-to-ambient thermal resistance.
ψ_{JT}	0.05	°C/W	Junction-to-top thermal characterization parameter. A thermal metric derived from the difference in junction temperature (TJ) and package top temperature (TT) divided by total heating power (PH).
$\theta_{JC\ (top)}$	4.9	°C/W	Junction-to-case thermal resistance with heat flow through package top.
θ_{JB}	15.2	°C/W	Junction-to-board thermal resistance.

Note: All parameters are as per JEDEC JESD-51.

Table 23 • PD69200 Thermal Specifications

Thermal Resistance	Typ	Units	Notes
θ_{JA}	33	°C/W	Junction-to-ambient thermal resistance.
Ψ_{JT}	8	°C/W	Junction-to-top thermal characterization parameter. A thermal metric derived from the difference in junction temperature (TJ) and package top temperature (TT) divided by total heating power (PH).
$\theta_{JC\ (top)}$	1.8	°C/W	Junction-to-case thermal resistance with heat flow through package top.
θ_{JB}	12	°C/W	Junction-to-board thermal resistance.

6.2 Recommended Solder Reflow

- RoHS 6/6
- Pb-free 100% Matte Tin Finish
- Package Peak Temperature for Solder Reflow (40 seconds maximum exposure)—260 °C (+0 °C, –5 °C)

Table 24 • Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/second max	3 °C/second max
Preheat		
Temperature min (TS_{min})	100 °C	150 °C
Temperature max (TS_{max})	150 °C	200 °C
Time (ts_{min} to ts_{max})	60–120 seconds	60–180 seconds
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60–150 seconds	60–150 seconds
Peak classification temperature (T_P)	210 °C to 235 °C	240 °C to 255 °C
Time within 5 °C of actual peak temperature (tp)	10–30 seconds	20–40 seconds
Ramp-down rate	6 °C/second max	6 °C/second max
Time 25 °C to peak temperature	6 minutes max	8 minutes max

Figure 15 • Classification Reflow Profiles

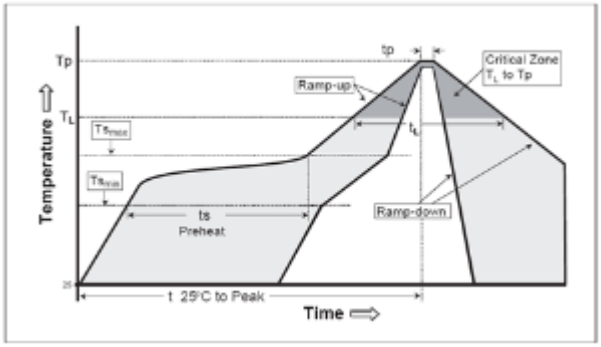


Table 25 • Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350—2000	Volume mm^3 >2000
<1.6 mm[1]	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm–2.5 mm[1]	260 + 0 °C	250 + 0 °C	245 + 0 °C
≥2.5 mm[1]	250 + 0 °C	245 + 0 °C	245 + 0 °C

1. Tolerance: The device manufacturer or supplier should assure process compatibility up to and including the stated classification temperature, meaning that the Peak reflow temperature is +0 °C. For example, 260 °C to 0 °C, at the rated MSL.

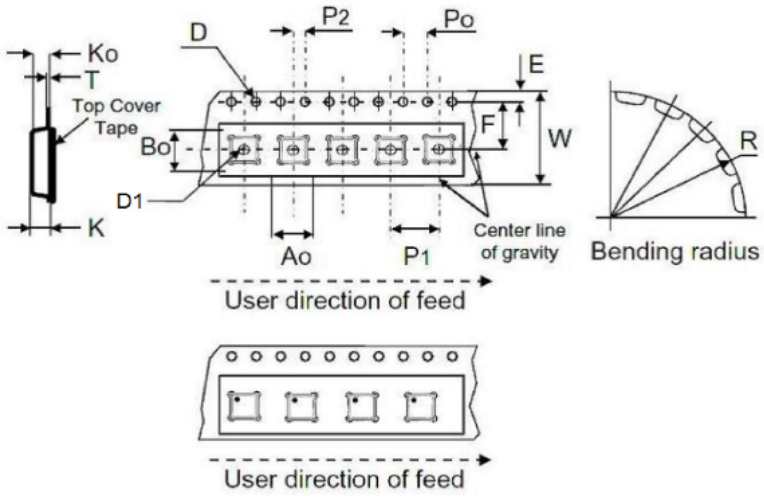
Note: Exceeding the ratings listed in the preceding table may damage the device.

6.3 Tape and Reel

This section describes the tape and reel.

6.3.1 PD69200 Tape and Reel Specification

Figure 16 • PD69200 Tape Specification

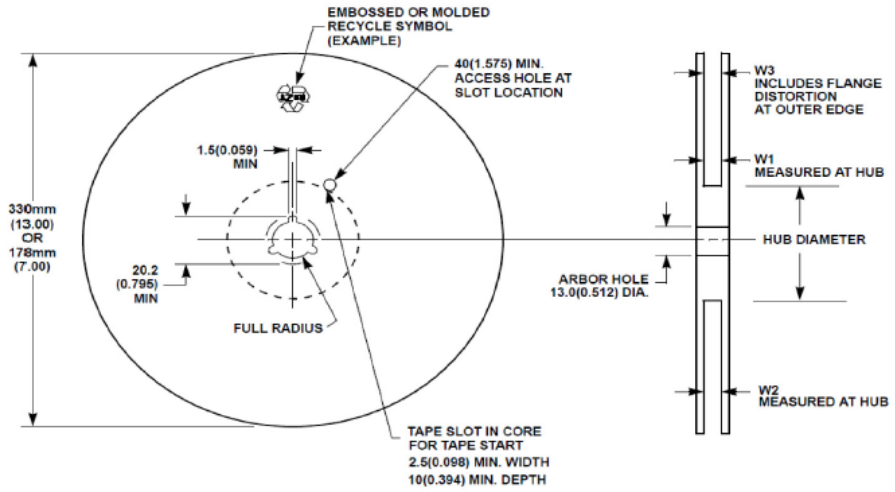


The following table lists the PD69200 tape mechanical data.

Table 26 • PD69200 Tape Mechanical Data

Dimensions	Value (mm)	Value (inches)
D	1.50 + 0.1/0	0.059 + 0.004/0
E	1.75 ±0.1	0.069 ±0.004
P0	4.00 ±0.1	0.157 ±0.004
T (max)	0.3 ±0.05	0.0118 ±0.003
D1	1.5	0.059
F	5.5 ±0.1	0.216 ±0.003
K (max)	1.6 ±0.1	0.0.63 ±0.004
P2	2.00 ±0.1	0.079 ±0.004
R	30	1.181
W	12.00 ±0.3	0.472 ±0.012
P1	8.00 ±0.1	0.31 ±0.004
K0	1.1	0.043
A0	5.30	0.208
B0	5.30	0.208

Figure 17 • PD69200 Reel Specification



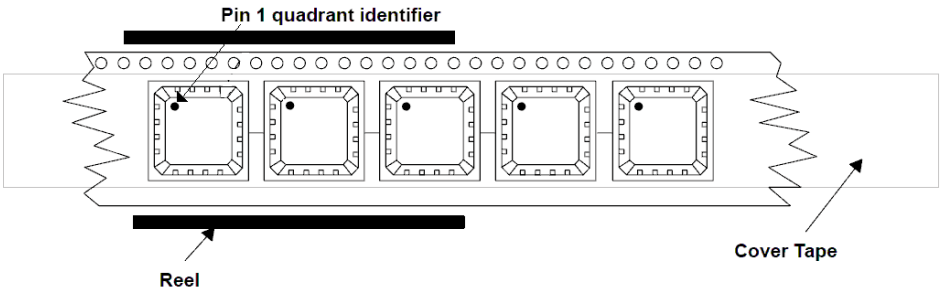
The following table lists the PD69200 reel mechanical data.

Table 27 • PD69200 Reel Mechanical Data

Dimensions	Value (mm)	Value (inches)
Tape size	12 +0.3	0.472 +0.012
W1	12.4	0.488
W2	18.4	0.724
W3	15.4	0.606

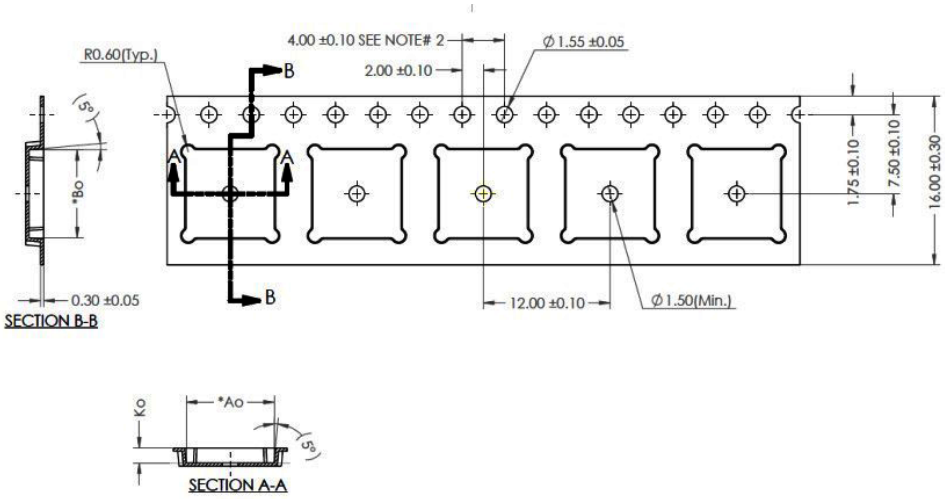
6.3.2 PD69208M Tape and Reel Specification

Figure 18 • PD69208M Tape and Reel Pin-1 Orientation



Pin-1 Orientation of QFN Packages

Figure 19 • PD69208M Tape Specifications



The following table lists the PD69208M tape mechanical data.

Table 28 • PD69208M Tape Mechanical Data

Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10
Width	16.00 ±0.30

Figure 20 • PD69208M Reel Specifications

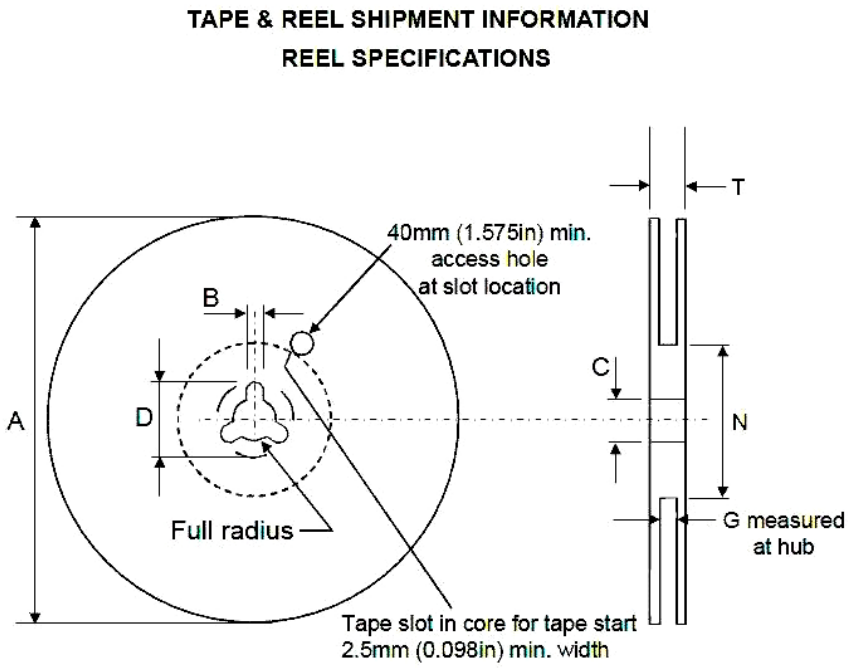


Table 29 • PD69208M Reel Mechanical Data

Dimensions	Value (mm)	Value (inch)
Tape size	16.00 ±0.3	0.630 ±0.012
A max	330	13
B max	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min	20.2	0.795
N min	50	1.968
G	16.4+2.0/–0.0	0.645+0.079/–0.0
T max	29	1.142
Base quantity	2000 pieces	

6.4 Reference Documents

- IEEE Std 802.3-2018 Clause 33 Power over Ethernet over 2-Pair and Clause 145 Power over Ethernet
- Microsemi, Serial communication protocol user guide (Catalog Number: PD69200_UG_COMM_PROT)
- Microsemi, Designing 48-port Enhanced PoE System (802.3af/802.3at Compliant) application note (Catalog Number: PD69208_AN_211)
- Microsemi, Software Download Algorithm technical note (TN-140 (Catalog Number: 06-0024-081)
- Microsemi, PoE LED stream technical note (Catalog Number: PD69100_TN_201)
- NXP, Kinetis_L MKL15Z128VFM4 datasheet
- NXP package drawings 98ASA00473D

7 Application Information

The PD69208M/PD69200 PSE chipset performs IEEE802.3af (Type 1), IEEE802.3at (Type 2), and IEEE802.3bt (Type 3) PSE functionalities in addition to the pre-standard and legacy (capacitor) detection. Moreover, it includes additional protections such as short circuit and dV/dT protection upon startup.

Note: IEEE802.3bt functionality will be enabled by a firmware upgrade.

7.1 PD Detection

The PD detection feature detects a valid IEEE802.3af, IEEE802.3at, or IEEE802.3bt. The PD detection is done based on four different voltage levels generated over PD (the load) as illustrated in the Typical IEEE802.3bt Port PoE Voltage Diagram (see page 42).

7.2 Legacy (Reduced Capacitor) Detection

When legacy detection is enabled, the PD detection mechanism detects and powers up the legacy and pre-standard PDs as well as IEEE802.3af, IEEE802.3at, and IEEE802.3bt standard compliant PDs (Classes 0–6).

7.3 Classification

The classification process takes place immediately after PD detection is successfully completed. The goal of the classification process is to detect PD class as specified in IEEE802.3 standards.

In IEEE802.3af mode, the classification mechanism is based on a single voltage level (single event). In IEEE802.3at and IEEE802.3bt modes, the classification mechanism is based on two voltage levels (multiple events) as defined in IEEE802.3-2015 Clause 33 and IEEE802.3bt.

Figure 21 • 4-Pair PoE System Diagram

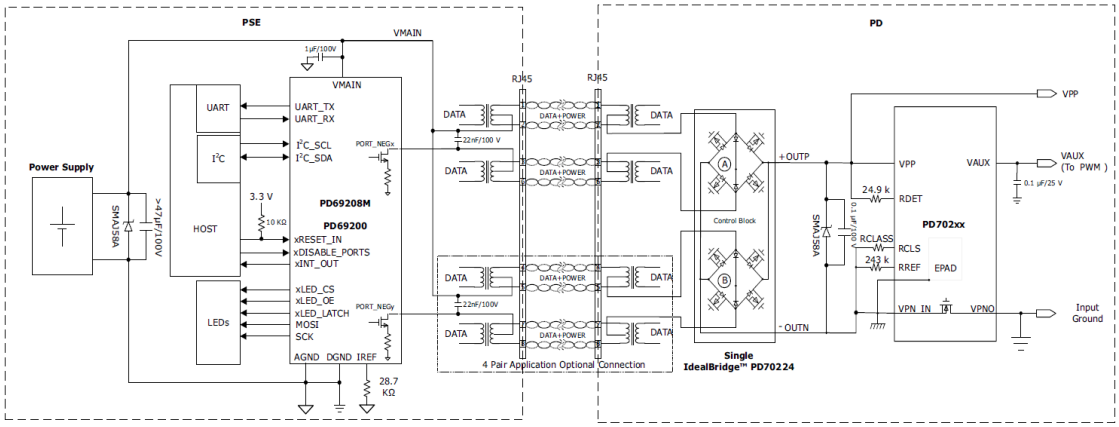
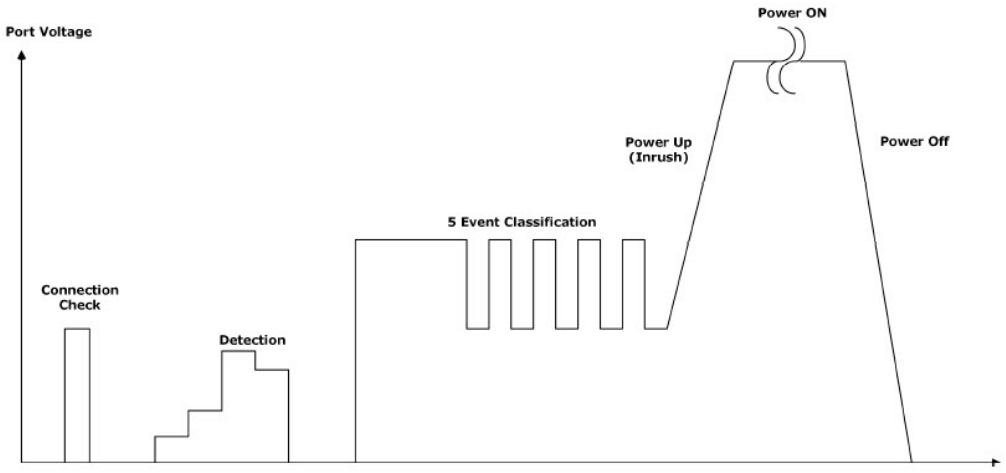


Figure 22 • Typical IEEE802.3bt Port PoE Voltage Diagram



7.4 Port Start-Up

Upon a successful detection and classification process, power is applied to the load via a controlled start-up mechanism.

During this period, inrush current is limited to 425 mA for a typical duration of 65 mS, which allows PD load to charge and allows a steady state of power condition.

7.5 Over-Load Detection and Port Shut Down

After power-up, PD69208M automatically initializes its internal protection mechanisms. These mechanisms are used to monitor and disconnect power from the PD when extreme conditions occur, as specified in the IEEE802.3 standards. These conditions include over-current or short ports terminals scenarios.

7.6 Disconnect Detection

PD69208M supports the DC disconnect function as per IEEE802.3 standards. This mechanism continuously monitors load current and disconnects power according to I_{UDL}, T_{MPDO}, and T_{MPS} parameters as specified in PD69208M Port Real Time Protection.

7.7 IC Thermal Monitoring

PD69208M contain a thermal sensor that is sampled by the PD69200 for every 20 mS so that the PD69208M die temperature is monitored at all times. If the die exceeds the temperature limit (150 °C), the system ports are disconnected to protect the PD69208M ICs.

A temperature alarm threshold can be set by PD69200 controller to send interrupt indication by the xINT_OUT pin before ports are disconnected. The temperature can be read and monitored by the host as well, if required.

7.8 Over-Temperature Protection

In addition to the die thermal sensor, there are thermal sensors on each MOSFET that continuously monitors each port main MOSFETs junction temperature, and shuts down the port load power when the temperature exceeds 200 °C.

7.9 V MAIN Out of Range Protection

The system automatically disconnects ports power when V_{MAIN} exceeds the pre-configured over-voltage and under-voltage thresholds.

7.10 2-Pair and 4-Pair Ports

Operation modes include the following:

- POE Type 1/2 class 0-4 (up to 30 W)
- POE Type 3 class 0-4 2-pair and class 5-6 4-pair (up to 60 W)

Note: For more information about 4-pair operation modes and power configuration, see Microsemi PoE 4-Pair Behavior PD6920x PSE Application Note 160159.

7.11 Power Management

The system supports three power management modes:

- Class (LLDP and CDP)
- Dynamic
- Static

7.12 Port Power Limit

Port power limit (PPL) is used to configure port power limit. When a port exceeds the power limit, it gets disconnected automatically.

7.13 Reset Pin

The xRESET pin is PD69200 digital host reset input (Active Low). The shortest pulse that is guaranteed to be recognized is 100 ns. PD69200 can generate self-reset. The xRESET pin is driven low by PD69200for at least 128 bus clock cycles until the flash initialization has completed. It is recommended to connect this pin to a host open drain output with a pull-up in a range of 4.7 KΩ to 10 KΩ. If this pin is connected to a push/pull driver, a serial resistor of 4.7 KΩ must be connected instead of a pull-up. Avoid resetting the PD69208M IC directly by the RESET_N pin. PD69200 controls the PD69208M ICs when the system reset is needed.

For more information about this pin connectivity, see the hardware application note (Catalog Number: PD69208_AN_211).

7.14 System OK Indication

Digital output pin to host is used as a system validity indication. When system is OK, pin state is low. The behavior of this output is controlled by software mask register settings (Mask 0×28). The mask default settings is 0, meaning that this pin indicates valid software and V_{MAIN} is in range. This pin is active low.

For more information, see the Serial Communication Protocol User Guide document (Catalog Number: PD69200_UG_COMM_PROT).

7.15 Interrupt Pin

Interrupt out from PoE controller, indicating events such as port on, port off, port fault, PoE device fault, voltage out of range, and more. For a full list of interrupt events, see the Serial Communication Protocol User Guide (Catalog Number: PD69200_UG_COMM_PROT). This pin is active low.

7.16 Port Matrix Control

Port matrix control enables layout designers to ascribe each physical port in the system to a logical port if required.

7.17 Power Good Interrupt

Interrupt from power supply directly to PD69208M manager. For systems comprising more than a single power supply, in case one power supply fails, a port shutdown mechanism is executed to maintain operation and prevent the collapse of other power supplies.

When a function is used, PGD0, PGD1, PGD2, and PGD3 should be connected to the main power supply status indication pin. Any change of at least 1 µs on these lines triggers a pre-defined disconnection matrix. This matrix is defined by PD69200 system power parameters. The port shutdown function reacts within 2 µs to any power good event.

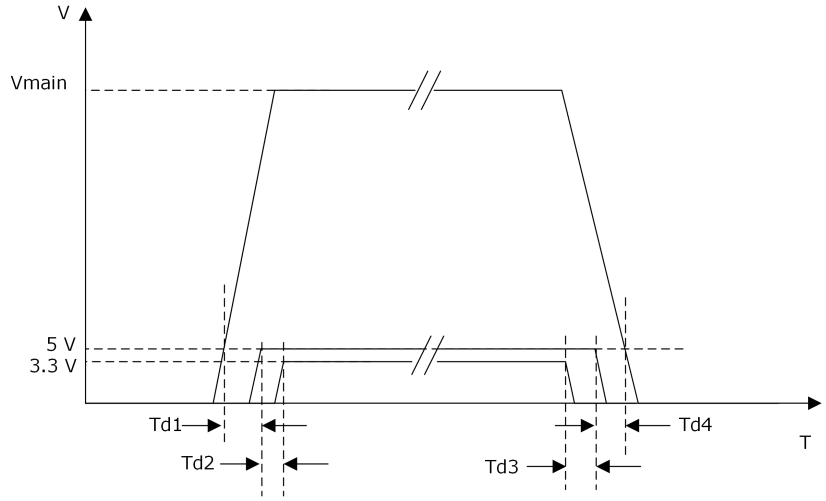
7.18 LED Stream

The direct SPI interface to an external LED stream circuitry that can drive LEDs directly without the host intervention. It enables designers to implement a simple LED circuit that does not require a software code. The LED stream clock frequency is 1 MHz.

For more information, see the TN-218 (Catalog Number: PD69200_TN_218).

7.19 Power Sequencing

Figure 23 • Power Sequencing



When using external V_{aux5} or V_{aux3p3}:

- Td1: V_{MAIN} at 5 V to V_{aux5} > 0 µs
- Td2: V_{aux5} to V_{aux3p3} > 0 µs
- Td3: V_{aux3p3} to V_{aux5} > 0 µs
- Td4: V_{aux5} to V_{MAIN} at 5 V > 0 µs
- $DV_{DD} = V_{aux3p3}$

Note: See the Application Note AN211 Designing a PD69208 48-port PoE System 802.3af/802.3at compliant.

For proper operations, you need to ensure that V_{MAIN} is always in the highest voltage connected to the IC. With an external DC-DC converter, the maximum 3.3 V slew rate is 100 ms.

8 Ordering Information

The following table lists the part ordering information for PD69200 and PD69208M devices.

Table 30 • Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking	Tray Marking
PD69200D[1]-VVVV[2]SS[3]	Plastic QFN 5 mm × 5 mm (32 lead)	Tray	–40 °C to 85 °C	Microsemi Logo NXP Logo 69200 M15M7V[4] XXXXX[5] YYYYY[6]	PD69200D- VVVVSS PD-OOOOG3bb[7] YYWW
PD69200D-VVVVSS-TR	Plastic QFN 5 mm × 5 mm (32 lead)	Tape and reel	–40 °C to 85 °C	Microsemi Logo NXP Logo 69200 M15M7V[4] XXXXX[5] YYYYY[6]	PD69200D- VVVVSS-TR PD-OOOOT3bb[7] YYWW
PD69208MILQ-TR-LE	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and reel	–40 °C to 85 °C	Microsemi Logo PD69208M L E e4[8] YYWWNNN[9]	

1. D stands for the detection method set as: C: Detection Method = IEEE802.3 and pre-standard; R: Detection Method = IEEE802.3.
2. VVVV is firmware revision.
3. SS stands for firmware parameters options.
4. Short part number
5. Mask set
6. Date code
7. MKTG Product Type (Detection = R: Resistor/D = C: Resistor/Legacy)/Version/SW Parameters /Operation P/N.
8. L = FAB Code, E for V2R4, and e4 = Second level interconnect.
9. YY = Year, WW = Week, and NNN = Trace code.

The Firmware Release Note has all the required information about how to specify the choice of VVVV and SS. You can find the Firmware Release Notes in the Microchip Software Libraries, and register yourself to a My Microchip account to have access to the release notes.

Note: The package meets RoHS, Pb-free, and MSL3 of the European Council to minimize the environmental impact of electrical equipment.

Note: Initial burning of controller's firmware is performed in the factory. Firmware upgrades can be performed by users using the communication interface. For more information, see TN-140 (Catalog Number: 06-0024-081).

The following table lists the manufacturing and ordering part numbers of PD69208M devices.

Table 31 • PD69208M Manufacturing and Ordering Part Numbers

Ordering Part Number	Die Revision	Product Revision Code	Manufacturing Part Number
PD69208MILQ-TR-LE	V2R4	E	PD69208MILQ-TR-LE

Note: Customers can order the PD69208M device using either the ordering part number or the manufacturing part number. See Ordering Information (see page 46) for a package, packing type, temperature, and part marking information.

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