Product Change Notification / SYST-05UHZG210

Date:

08-Oct-2020

Product Category:

Wireless Modules

PCN Type:

Document Change

Notification Subject:

ERRATA - PIC32MZ-W1 MCU and WFI32E01 Module Errata

Affected CPNs:

SYST-05UHZG210_Affected_CPN_10082020.pdf
SYST-05UHZG210_Affected_CPN_10082020.csv

Notification Text:

SYST-05UHZG210

Microchip has released a new Product Documents for the PIC32MZ-W1 MCU and WFI32E01 Module Errata of devices. If you are using one of these devices please read the document located at PIC32MZ-W1 MCU and WFI32E01 Module Errata.

Notification Status: Final

Description of Change: Initial release.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 08 Oct 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

PIC32MZ-W1 MCU and WFI32E01 Module Errata

Please contact your local Microchip sales office with questions or concerns regarding this notification.

Terms and Conditions:

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Affected Catalog Part Numbers (CPN)

PIC32MZ1025W104132-I/NX
WFI32E01PC-I
WFI32E01PCI
WFI32E01PE-I

PIC32MZ1025W104 MCU and WFI32E01 Module with Wi-Fi® and Hardware-based Security Accelerator Errata

The PIC32MZ W1 Family of devices that you have received conform functionally to the current Device Data Sheet (DS70005425), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select *Window* > *Dashboard*, then click the **Refresh Debug Tool Status** icon ( ).
5. The part number and the Device and Revision ID values appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, visit support.microchip.com or contact your local Microchip sales office.

The Device and Revision ID values for the PIC32MZ1025W104 silicon are shown in Table 1.

TABLE 1: SILICON DEVICE AND REVISION DETAILS

Part Number	Device ID	Revision ID for Silicon Revision
		A1
PIC32MZ1025W104	0x80C03053	X

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Issue	Issue Summary	Affected Revisions
				A1
ADC	Level Trigger	1.	The ADC level trigger does not perform burst conversions in Debug mode.	X
ADC	Scan	2.	Scan list conversion restarts without finishing the current scan list if a new trigger occurs before the scan completion with ADC2 (shared ADC).	X
CAN	Interrupt	3.	The CAN Wake Interrupt Flag bit, WAKIF, is set even when the CAN module is disabled.	X
CAN	CAN	4.	The CAN FIFO abort operation during transmission does not set the TXABAT bit in FIFOCON register.	X
Crypto	Partial Packet	5.	The cryptographic DMA module does not support partial packet processing.	X
Crypto	Zero Length Packet	6.	Using the crypto DMA on an empty hash string will cause the peripheral to time out and not return a valid hash.	X
I^2C	I^2C Slave	7.	The 7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.	X
I^2C	Speed	8.	The I^2C module does not meet the low period of the SCL clock (t_{LOW}) parameter from the I^2C specification for clock frequency >= 400 kHz.	X
ICSP	TDO	9.	The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.	X
Oscillators	Clock Switching	10.	Some clock switching combinations result in PLL locking failure.	X
Oscillators	RODIV Failure	11.	Failures at random voltage and temperature when the RODIV are set to a higher value.	X
Ports	Pin Remapping	12.	All remappable output configuration registers (RPA, RPB, RPC, and RPK) are always read 0.	X
SPI	Block Transmission	13.	The SRMT bit incorrectly indicates the end of transmission for the last PBCLK.	X
SQI	Special Function Registers	14.	The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled after a Reset.	X
SQI	SQI	15.	Reading the SQI registers with the default value causes a debug port failure/target Reset.	X
Timer1	Asynchronous Counter	16.	Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CLK input.	X
Timer1	TMR1 Register	17.	The TMR1 register of Timer1 in Asynchronous mode remains at the initial set value for five external clock pulses after wake-up from Sleep mode.	X
Timer1	Asynchronous Mode	18.	Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.	X
Timer1	TMR1 Register Write	19.	Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.	X

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Issue	Issue Summary	Affected Revisions
				A1
Timer1	Sleep Async	20.	The TMR1 register of Timer1 in Asynchronous mode remains at the initial set value of five external clock pulses after wake-up from Sleep mode.	X
UART	TX/RX Interrupt	21.	A UART Transmit Interrupt (UTXISEL[1:0] bits (UxSTA[15:14]) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL[1:0] bits (UxSTA[7:6]) = ‘0b00) is asserted while the receive buffer is not empty and non-functional.	X
UART	TX Interrupt	22.	A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b01) is generated, but does not remain asserted when all of the characters have been transmitted.	X
UART	TX Interrupt	23.	A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b10) is generated but does not remain asserted while the transmit buffer is empty.	X
UART	RX Interrupt	24.	The UART Receive Interrupt flag (URXI-SEL[1:0] bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.	X
UART	RX Interrupt	25.	The UART Receive Interrupt Flag bit (URXI-SEL[1:0] bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.	X
UART	Data Transmission	26.	The UART operation using PPS pins may fail with higher baud rates.	X
Watchdog Timer (WDT)	WDT	27.	WDT does not reset the device if WDT writes are performed outside of the WDT window.	X
Watchdog Timer (WDT)	WDT	28.	WDT does not reset the CPU within the expected time period across the voltage and temperature ranges.	X

Silicon Errata Issues

1. Module: ADC

The ADC level trigger does not perform burst conversions in Debug mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

2. Module: ADC

The scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and do not generate an EOSRDY bit (ADCCON2[29]) end of scan interrupt status if a new trigger event from the STRGSRC[4:0] bits (ADCCON1[20:16]) trigger source occurs before the scan list completion on the shared ADC2 core.

Work around

Ensure that the STRGSRC[4:0] bits trigger source repetition rate > (sample + conversion) times of the sum of all ANx inputs defined in the ADCCSS1/ADCCSS2 registers.

Affected Silicon Revisions

A1							
X							

3. Module: CAN

Clear the WAKIF (CxINT[14]) bit prior to enabling the CAN peripheral.

Work around

During the CAN initialization and before enabling the CAN peripheral, clear the WAKIF bit in the user code and this work around is implemented in Harmony.

Affected Silicon Revisions

A1							
X							

4. Module: CAN

The CAN FIFO aborts the operation during transmission without setting the TXABAT bit in the FIFOCON register.

Work around

None.

Affected Silicon Revisions

A1							
X							

5. Module: Crypto

Attempting to run part of a cryptographic packet through the peripheral may not result in a usable initial vector for continuing the cryptographic operation.

Work around

Do not interrupt a cryptographic operation with another, instead, always process a hash completely.

Affected Silicon Revisions

A1							
X							

6. Module: Crypto

Using the crypto DMA on an empty hash string will cause the peripheral to time out and not return a valid hash.

Work around

Use the fixed known hash of the empty string.

Affected Silicon Revisions

A1							
X							

7. Module: I^2C

The 7-bit address that matches the 10-bit upper address value (111_10xx_xxx) is not accepted regardless of the STRICT bit setting.

Work around

None.

Affected Silicon Revisions

A1							
X							

8. Module: I²C

The I²C module does not meet the low period of the SCL clock (t_{LOW}) parameter from the I²C specification for clock frequency >= 400 kHz.

Work around

None.

Affected Silicon Revisions

A1							
X							

9. Module: ICSP

The TDO pin becomes an output and toggles while programming on any ICSP™ PGECx/PGEDx pair.

Work around

None.

Affected Silicon Revisions

A1							
X							

10. Module: Oscillators

A failure in switching from any PLL clock source to UPLL leads to device Reset.

Note: All the switching is to their respective maximum clock frequency.

Work around

If there is a requirement to switch any PLL clock source to UPLL, switch to the FRC clock first, and, then, to the UPLL.

Affected Silicon Revisions

A1							
X							

11. Module: Oscillators

Failures seen at random voltage and temperature when the RODIV[14:0] are set to higher value (i.e., 0x7FFF and 0x3FFE) and when SYSPLL is
200 MHz to achieve 3 kHz and 6 kHz, respectively.

Work around

The reference clock of 3 kHz can be achieved when:

1. The SYSCLK is 100 MHz with POSC as the source.

2. The SYSCLK is 200 MHz with FRC as the source.

Affected Silicon Revisions

A1							
X							

12. Module: Ports

All remappable output configuration registers (RPA, RPB, RPC, and RPK) always read 0.

Work around

None.

Affected Silicon Revisions

A1							
X							

13. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL = 0).

Work around

Use the interrupt indication bit to determine the end of transmission.

Affected Silicon Revisions

A1							
X							

14. Module: SQI

After a Reset, the first access to the SQI SFRs must be a write. A read access can stall the CPU, requiring a Reset to clear. The typical initialization code may include a write to the SQIEN bit. The SQI1CFGbits.SQIEN=0 instruction is a read, modify and write sequence. After a Reset, this sequence will stall the CPU. Similarly, only reading the SQI SFRs will stall the CPU if that read is the first access after a Reset.

Work around

Enable the REFCLKO2 before reading the registers from the SQI peripheral. Do not use the "SQI1CFGbits.SQIEN=0" instruction to enable the SQI, instead use the "SQI1CFGCLR= _SQICFG_SQIEN_MASK" instruction.

Affected Silicon Revisions

A1							
X							

15. Module: SQI

Reading the SQI registers with the default value causes a debug port failure/target reset.

Work around

If the SQI is used, then program the SQI1CFG register to 2'b01(CPU mode) in the boot code.

Affected Silicon Revisions

A1							
X							

16. Module: Timer1

In Asynchronous External Counter mode, (i.e., TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0) and TECS[1:0] (T1CON[9:8] = '0b01)), the Timer1 register (TMR1) does not reflect the first count from an external T1CLK input.

Work around

Always add 1 to the Timer1 count value to reflect the first count from an external T1CLK input.

Affected Silicon Revisions

A1							
X							

17. Module: Timer1

In Asynchronous External Counter mode, (i.e., TCS bit (T1CON[1] = 1), TSYNC bit (T1CON[2] = 0), and TECS[1:0] (T1CON[9:8] = '0b01)), the Timer1 register (TMR1) remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

18. Module: Timer1

Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around

Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

A1							
X							

19. Module: Timer1

Back-to-back CPU writes to the TMR1 register are not allowed within four PBCLK cycles.

Work around

None.

Affected Silicon Revisions

A1							
X							

20. Module: Timer1

The TMR1 register of Timer1 in Asynchronous mode (i.e., TCS bit (T1CON[1] = 1, TSYNC bit (T1CON[2] = 0, and TECS[1:0] bits (T1CON[9:8]) are greater than '0b01), remains at the initial set value for 5 external clock pulses after the wake-up from Sleep mode.

Work around

None.

Affected Silicon Revisions

A1							
X							

21. Module: UART

A UART Transmit Interrupt (UTXISEL[1:0] bits (UxSTA[15:14]) = ‘0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL[1:0] bits (UxSTA[7:6]) = ‘0b00) is asserted while the receive buffer is not empty and non-functional.

Work around

None.

Affected Silicon Revisions

A1							
X							

22. Module: UART

A UART Transmit Interrupt (UTXISEL[1:0] bits = ‘0b01) is generated but does not remain asserted even when all of the characters have been transmitted. Once the IFSx bit is cleared by the user, it does not remain asserted even while all characters have been transmitted. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFSx flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1							
X							

23. Module: UART

The UART Transmit UTXISEL[1:0] bits = ‘0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty. Once the IFS bit is cleared by the user, it does not remain asserted even while the transmit buffer is empty. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

Work around

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

Affected Silicon Revisions

A1							
X							

24. Module: UART

The UART Receive Interrupt Flag (URXISEL[1:0] bits = ‘0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.

Work around

Before exiting the UART RX ISR, ensure all the contents of the RX Buffer have been read, by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA[0]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A1							
X							

25. Module: UART

The UART Receive Interrupt Flag bit (URXISEL[1:0] bits = ‘0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

Work around

Before exiting the UART RX ISR, ensure the entire contents of the RX Buffer have been read by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA[10]) is cleared and this work around is implemented in Harmony.

Affected Silicon Revisions

A1							
X							

26. Module: UART

When the UART channel is selected using the PPS feature for the TX pins, the transmitted string may fail to send the correct characters in high baud rates. The issue occurs randomly on any Voltage and Temperature, and is rare. The issue appears only on UART2 and UART3.

Work around

Use the FRC clock as the baud clock source to use the UART in high baud rate with the PPS feature.

Affected Silicon Revisions

A1							
X							

27. Module: Watchdog Timer (WDT)

The WDT does not reset the device if the WDT writes are performed outside of the WDT window.

Work around

None.

Affected Silicon Revisions

A1							
X							

28. Module: Watchdog Timer (WDT)

When LPRC is used as a WDT source prescalar, the WDT does not cause a CPU Reset within the time period expected by the WDTPS configurations. The following table shows the WDT and prescaler values, with their corresponding expected reset period and mean values.

TABLE 3: WDTPS CONFIGURATION

PS Value	Input Clock	Expected Time Period	Mean Value
0xA	LRPC	1s	1.026s
0xB	LPRC	2s	2.025s
0xA	LRPC	1s	1.439s
0xB	LPRC	2s	2.357s

Work around

None.

Affected Silicon Revisions

A1							
X							

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A (September 2020)

Initial release.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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