

Table 1–2. Cyclone II Package Options & Maximum User I/O Pins *Notes (1) (2)*

Device	144-Pin TQFP (3)	208-Pin PQFP (4)	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 (6) (8)	89	142	—	158 (5)	—	—	—	—
EP2C8 (6)	85	138	—	182	—	—	—	—
EP2C8A (6), (7)	—	—	—	182	—	—	—	—
EP2C15A (6), (7)	—	—	—	152	315	—	—	—
EP2C20 (6)	—	—	142	152	315	—	—	—
EP2C20A (6), (7)	—	—	—	152	315	—	—	—
EP2C35 (6)	—	—	—	—	322	322	475	—
EP2C50 (6)	—	—	—	—	294	294	450	—
EP2C70 (6)	—	—	—	—	—	—	422	622

Notes to Table 1–2:

- (1) Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C20 device in the 484-pin FineLine BGA package and the EP2C35 and EP2C50 devices in the same package).
- (2) The Quartus® II software I/O pin counts include four additional pins, TDI, TDO, TMS, and TCK, which are not available as general purpose I/O pins.
- (3) TQFP: thin quad flat pack.
- (4) PQFP: plastic quad flat pack.
- (5) Vertical migration is supported between the EP2C5F256 and the EP2C8F256 devices. However, not all of the DQ and DQS groups are supported. Vertical migration between the EP2C5 and the EP2C15 in the F256 package is not supported.
- (6) The I/O pin counts for the EP2C5, EP2C8, and EP2C15A devices include 8 dedicated clock pins that can be used for data inputs. The I/O counts for the EP2C20, EP2C35, EP2C50, and EP2C70 devices include 16 dedicated clock pins that can be used for data inputs.
- (7) EP2C8A, EP2C15A, and EP2C20A have a Fast On feature that has a faster POR time. The EP2C15A is only available with the Fast On option.
- (8) The EP2C5 optionally support the Fast On feature, which is designated with an “A” in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook*.

Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C35, EP2C50, and EP2C70 devices in the 672-pin FineLine BGA package). The exception to vertical migration support within the Cyclone II family is noted in [Table 1–3](#).

Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

Table 1–3. Total Number of Non-Migratable I/O Pins for Cyclone II Vertical Migration Paths

Vertical Migration Path	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA (1)	484-Pin FineLine BGA (2)	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA (3)
EP2C5 to EP2C8	4	4	1 (4)	—	—	—
EP2C8 to EP2C15	—	—	30	—	—	—
EP2C15 to EP2C20	—	—	0	0	—	—
EP2C20 to EP2C35	—	—	—	16	—	—
EP2C35 to EP2C50	—	—	—	28	28 (5)	28
EP2C50 to EP2C70	—	—	—	—	28	28

Notes to Table 1–3:

- (1) Vertical migration between the EP2C5F256 to the EP2C15AF256 and the EP2C5F256 to the EP2C20F256 devices is not supported.
- (2) When migrating from the EP2C20F484 device to the EP2C50F484 device, a total of 39 I/O pins are non-migratable.
- (3) When migrating from the EP2C35F672 device to the EP2C70F672 device, a total of 56 I/O pins are non-migratable.
- (4) In addition to the one non-migratable I/O pin, there are 34 DQ pins that are non-migratable.
- (5) The pinouts of 484 FBGA and 484 UBGA are the same.



When moving from one density to a larger density, I/O pins are often lost because of the greater number of power and ground pins required to support the additional logic within the larger device. For I/O pin migration across densities, you must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

To ensure that your board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (go to Assignments menu, then Device, then click the **Migration Devices** button). After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path. Table 1–3 lists the Cyclone II device package offerings and shows the total number of non-migratable I/O pins when migrating from one density device to a larger density device.