



Three-Wire Hall-Effect Latch with Advanced Diagnostics

FEATURES AND BENEFITS

- Functional safety
 - Developed in accordance with ISO 26262:2011 (pending assessment)
 - Designed to meet ASIL B requirements
 - Integrated background diagnostics for:
 - Signal path
 - Regulator
 - Hall plate and bias
 - Overtemperature detection
 - Nonvolatile memory
 - Defined fault state
- Multiple product options
 - Magnetic polarity, switchpoints, and hysteresis
 - Temperature coefficient
 - Output polarity
- Reduces module bill-of-materials (BOM) and assembly cost
 - ASIL B sensor can replace redundant sensors
 - Integrated overvoltage clamp and reverse-battery diode

Continued on the next page...

PACKAGES

3-pin SOT23-W (LH)

3-pin ultramini SIP (UA)



Not to scale

DESCRIPTION

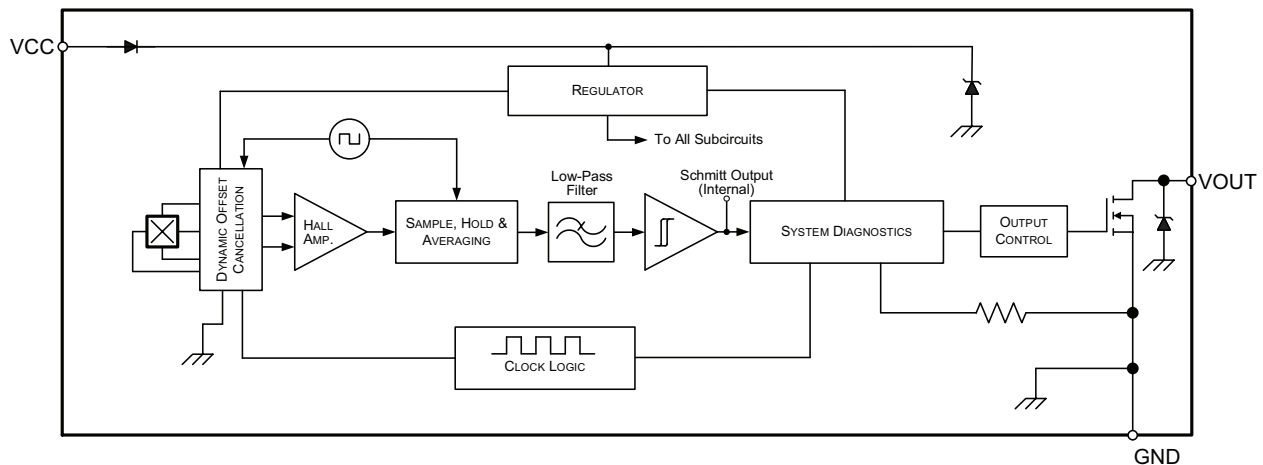
The APS12450 is a three-wire planar Hall-effect sensor integrated circuit (IC) developed in accordance with ISO 26262:2011. It includes internal diagnostics and a fault state that support a functional safety level of ASIL B when integrated and used in conjunction with the appropriate system-level control. The enhanced three-wire interface provides interconnect open/short diagnostics and a fault state to communicate diagnostic information while maintaining compatibility with legacy three-wire systems. The continuous background diagnostics are transparent to the host system and results in a reduced fault tolerant time.

The APS12450 product options include magnetic switchpoints, temperature coefficient, and output polarity. The response can be matched to SmCo, NdFeB, or low-cost ferrite magnets. For situations where a functionally equivalent three-wire switch device is preferred, refer to the APS11450.

Continued on the next page...

TYPICAL APPLICATIONS

- Automotive and industrial safety systems
- Seat/window motors
- Sun roof/convertible top/tailgate/liftgate actuation
- Brake and clutch by wire actuators
- Engine management actuators
- Electric power steering (EPS)
- Transmission shift actuator



Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Automotive-grade ruggedness and fault tolerance
 - Extended AEC-Q100 Grade 0 qualification
 - Operation to 175°C junction temperature
 - 3 to 30 V operating voltage range
 - ±8 kV HBM ESD
 - Overtemperature indication

DESCRIPTION (continued)

APS12450 sensors are engineered to operate in the harshest environments with minimal external components. They are qualified beyond the requirements of AEC-Q100 Grade 0 and will survive extended operation at 175°C junction temperature.

These monolithic ICs include on-chip reverse-battery protection, overvoltage protection (e.g., 40 V load dump), ESD protection, overtemperature detection, and an internal voltage regulator for operation directly from an automotive battery bus. These integrated features reduce the end-product bill-of-materials (BOM) and assembly cost.

Package options include industry-standard surface-mount SOT (LH) and through-hole SIP (UA) packages. Both packages are RoHS-compliant and lead (Pb) free with 100% matte-tin-plated leadframes.

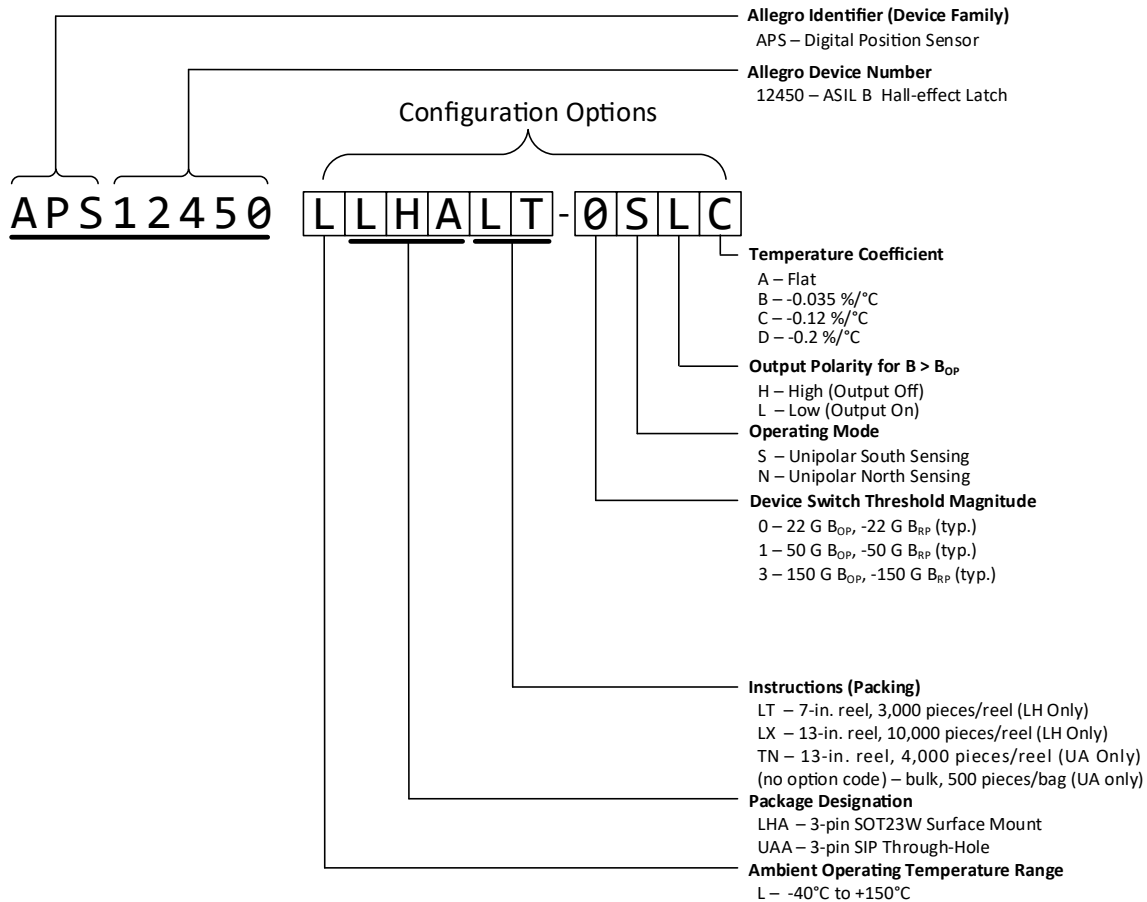
SELECTION GUIDE [1]

Part Number	Package	Packing	Output Polarity (B > B _{OP})	Temperature Coefficient	Magnetic Operate Point, B _{OP} (typ)
APS12450LLHALX-0SLA	3-pin SOT23W surface mount	13-in. reel, 10,000 pieces/reel	Low	0%/°C	22 G
APS12450LLHALT-0SLA	3-pin SOT23W surface mount	7-in. reel, 3000 pieces/reel			
APS12450LUAA-0SLA	3-pin SIP through-hole	bulk, 500 pieces/bag			
APS12450LLHALX-1SLA	3-pin SOT23W surface mount	13-in. reel, 10,000 pieces/reel	Low	0%/°C	50 G
APS12450LLHALT-1SLA	3-pin SOT23W surface mount	7-in. reel, 3000 pieces/reel			
APS12450LUAA-1SLA	3-pin SIP through-hole	bulk, 500 pieces/bag			
APS12450LLHALX-3SLA	3-pin SOT23W surface mount	13-in. reel, 10,000 pieces/reel	Low	0%/°C	150 G
APS12450LLHALT-3SLA	3-pin SOT23W surface mount	7-in. reel, 3000 pieces/reel			
APS12450LUAA-3SLA	3-pin SIP through-hole	bulk, 500 pieces/bag			

[1] Contact Allegro MicroSystems for options not listed in the selection guide.



Complete Part Number Format

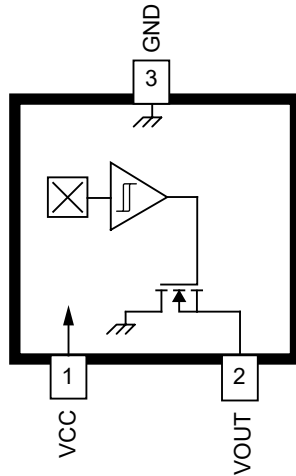


ABSOLUTE MAXIMUM RATINGS

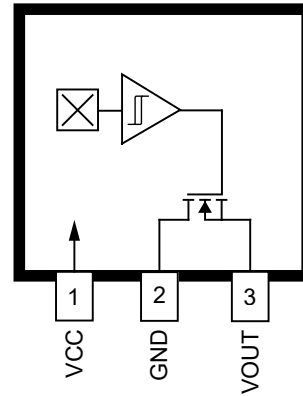
Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage ^[2]	V _{CC}		35	V
Reverse Supply Voltage	V _{RCC}		-30	V
Forward Output Voltage	V _{OUT}		30	V
Reverse Output Voltage	V _{ROUT}		-0.3	V
Output Current Sink	I _{OUT(SINK)}	V _{CC} to V _{OUT}	12	mA
Maximum Junction Temperature	T _{J(MAX)}		165	°C
		For 500 hours	175	°C
Storage Temperature	T _{stg}		-65 to 170	°C

^[2] This rating does not apply to extremely short voltage transients such as load dump and/or ESD. Those events have individual ratings specific to the respective transient voltage event. Contact your local field applications engineer for information on EMC test results.

PINOUT DIAGRAMS AND TERMINAL LIST



LH Package, 3-Pin SOT23W Pinout



UA Package, 3-Pin SIP Pinout

Terminal List Table

Name	Pin Number		Function
	LH	UA	
VCC	1	1	Supply voltage
VOUT	2	3	Output
GND	3	2	Ground

OPERATING CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
SUPPLY AND STARTUP						
Supply Voltage [2]	V_{CC}	Operating, $T_J < 165^\circ\text{C}$	3.0	–	30	V
Supply Current	I_{CC}		–	–	4.5	mA
Power-On Time [3]	t_{on}	$V_{CC} > V_{CC(min)}$, $B < B_{RP(min)} - 10\text{ G}$, $B > B_{OP(max)} + 10\text{ G}$	–	–	150	μs
Power-On State	POS	$t < t_{on(max)}$	$V_{OUT(FAULT)}$			–
Output Rise Time	t_{RISE}	See Applications Circuit, Figure 9; $V_{PU} = V_{CC}$, $R_{PU} = 3\text{ k}\Omega$, $C_{OUT} = 1\text{ nF}$, $I_{OUT} < 12\text{ mA}$	2	4	15	μs
Output Fall Time	t_{FALL}		2	4	15	μs
Output On Voltage	$V_{OUT(LOW)}$	Output ratiometric to V_{PU} ; $V_{PU} = V_{CC}$, $\tau < 3\text{ }\mu\text{s}$ [5], $I_{OUT} < 12\text{ mA}$	10	20	30	%
Output Off Voltage	$V_{OUT(HIGH)}$		70	80	90	%
Output Off Voltage Overshoot [4]	$V_{OUT(HIGH)OVER}$	Overshoot percentage relative to V_{PU} (see Figure 8); $V_{PU} = V_{CC}$, $\tau < 3\text{ }\mu\text{s}$ [5], $I_{OUT} < 12\text{ mA}$	–	2	–	%
	$t_{VOUT(H)OVER}$		Duration of output voltage overshoot ($V_{OUT(HIGH)OVER}$)	–	–	5
ON-BOARD PROTECTION						
Fault Reaction Time	t_{DIAG}		–	25	60	μs
Diagnostics Fault Retry Time [6]	t_{DIAGF}		–	2	–	ms
Fault Mode Output Voltage (Fault State)	$V_{OUT(FAULT)}$	$V_{PU} = V_{CC}$, $\tau < 3\text{ }\mu\text{s}$, $I_{OUT} < 12\text{ mA}$	$> V_{OUT(HIGH)MAX}$	V_{PU}	–	V
Overtemperature Shutdown	T_{SD}	Temperature increasing	–	205	–	$^\circ\text{C}$
Overtemperature Hysteresis	T_{JHYS}		–	25	–	$^\circ\text{C}$

[1] Typical data is at $T_A = 25^\circ\text{C}$ and $V_{CC} = 12\text{ V}$ and is for design information only.

[2] V_{CC} represents the voltage between the VCC pin and the GND pin.

[3] Power-On Time (t_{ON}) is measured from $V_{CC} = V_{CC(min)}$ to 50% of the output transition from V_{PU} to final value. Adding a bypass capacitor will increase Power-On Time.

[4] The overshoot specification pertains only to conditions where the overshoot is greater than the $V_{OUT(HIGH)MAX}$ specification.

[5] τ is the time constant of the RC circuit; $\tau = R_{PU} \times C_{OUT}$.

[6] The diagnostics fault retry repeats continuously until a fault condition is no longer observed. See Diagnostics Mode Operation section for details.

TRANSIENT PROTECTION CHARACTERISTICS: Valid for $T_A = 25^\circ\text{C}$ and $C_{BYP} = 0.1\text{ }\mu\text{F}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
Forward Supply Zener Clamp Voltage	V_Z	$I_{CC(max)} + 3\text{ mA}$	35	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RCC}	$I_{CC} = -1\text{ mA}$	–	–	–30	V
Reverse Supply Current	I_{RCC}	$V_{RCC} = -30\text{ V}$	–	–	–5	mA

MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_{J(max)}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
Sensitivity Temperature Coefficient	$T_{C_{SENS}}$	(A) Flat	–	0	–	%/°C
		(B) SmCo	–	–0.035	–	%/°C
		(C) NdFeB	–	–0.12	–	%/°C
		(D) Ferrite	–	–0.2	–	%/°C
Analog Signal Bandwidth	$f_{(-3dB)}$		–	10	–	kHz
Operate Point	B_{OP}	APS12450–0SxA	5	22	40	G
		APS12450–1SxA	15	50	90	G
		APS12450–3SxA	100	150	180	G
Release Point	B_{RP}	APS12450–0SxA	–40	–22	–5	G
		APS12450–1SxA	–90	–50	–15	G
		APS12450–3SxA	–180	–150	–100	G
Hysteresis	B_{HYS}	APS12450–0SxA	10	45	80	G
		APS12450–1SxA	30	100	180	G
		APS12450–3SxA	200	300	360	G
Symmetry	B_{SYM}	$B_{OP} + B_{RP}$	–30	–	30	G
Jitter [3]	–	$B_{OP} = 22 \text{ G}, B = 100 \text{ G}_{PK-PK}, 1000 \text{ Hz}$	–	0.25	–	%

[1] Typical data is at $T_A = 25^\circ\text{C}$ and $V_{CC} = 12 \text{ V}$, unless otherwise noted; for design information only.

[2] 1 G (gauss) = 0.1 mT (millitesla).

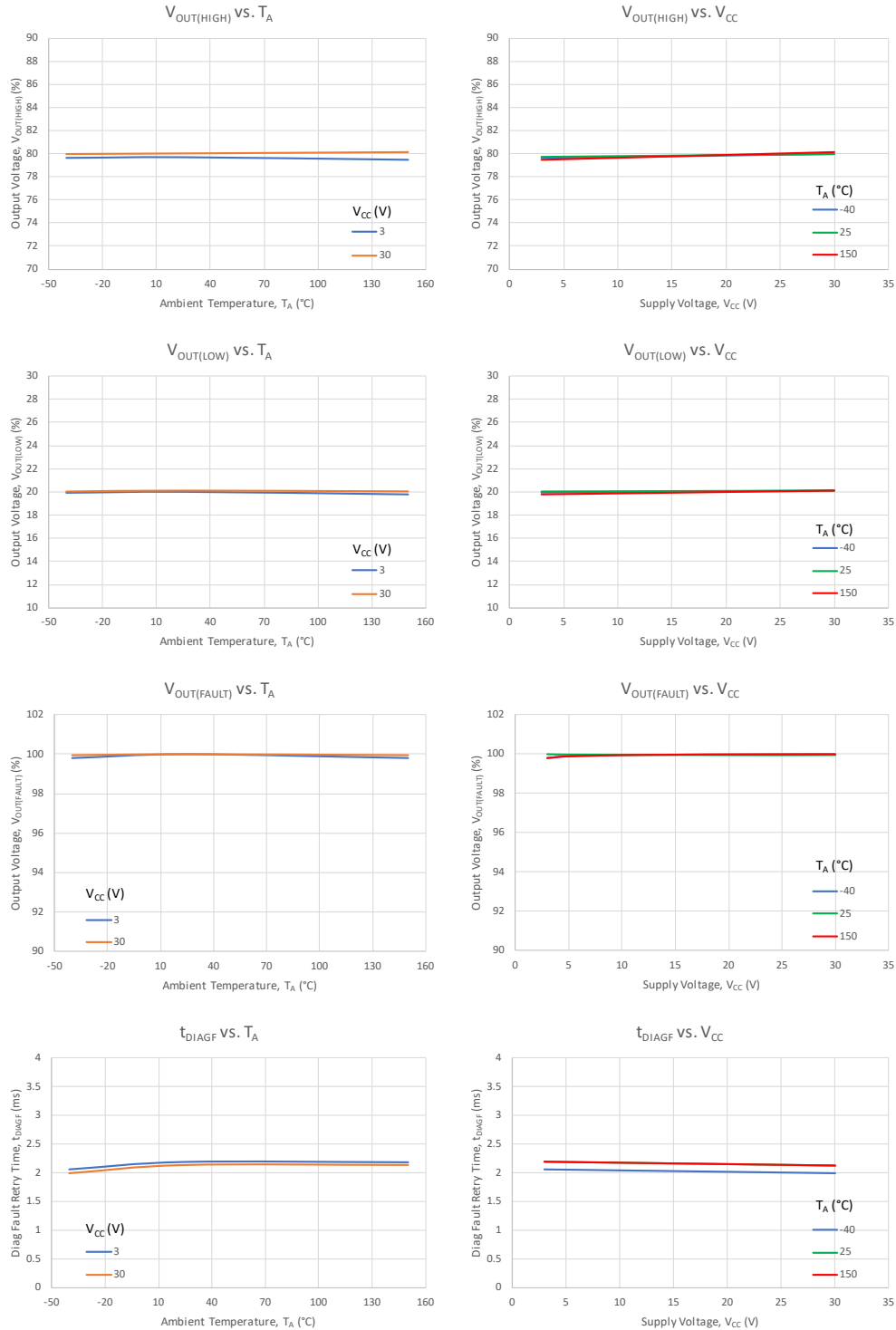
[3] Output edge repeatability as a percentage of the period.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

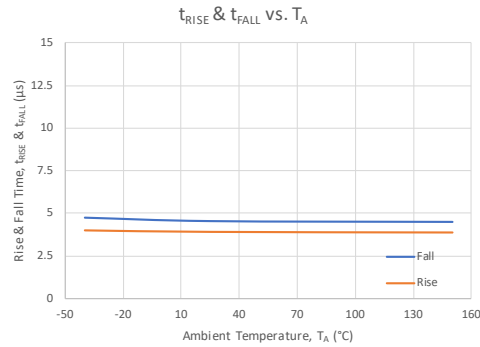
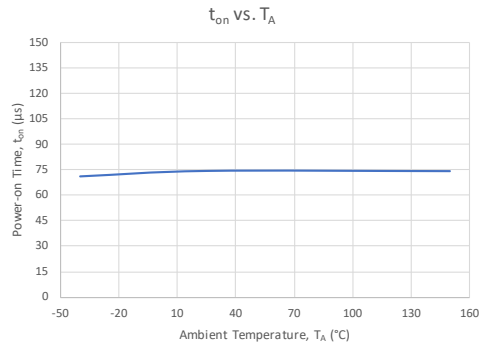
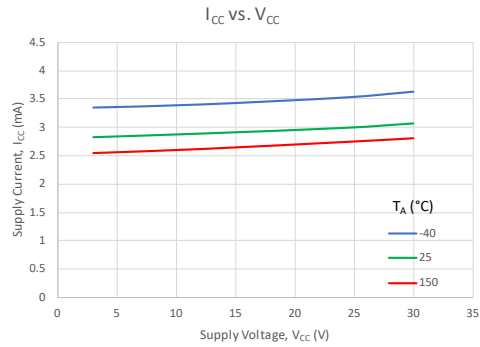
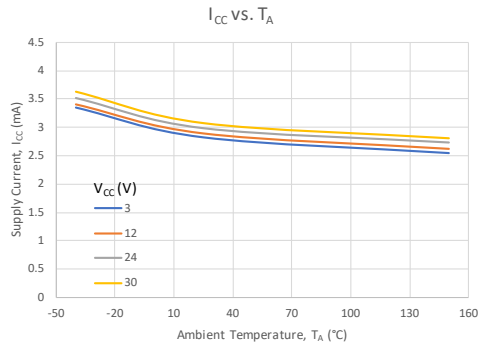
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, on 1-layer PCB based on JEDEC standard	228	°C/W
		Package LH, on 2-layer PCB with 0.463 in. ² of copper area each side	110	°C/W
		Package UA, on 1-layer PCB with copper limited to solder pads	165	°C/W

*Additional thermal information available on the Allegro website.

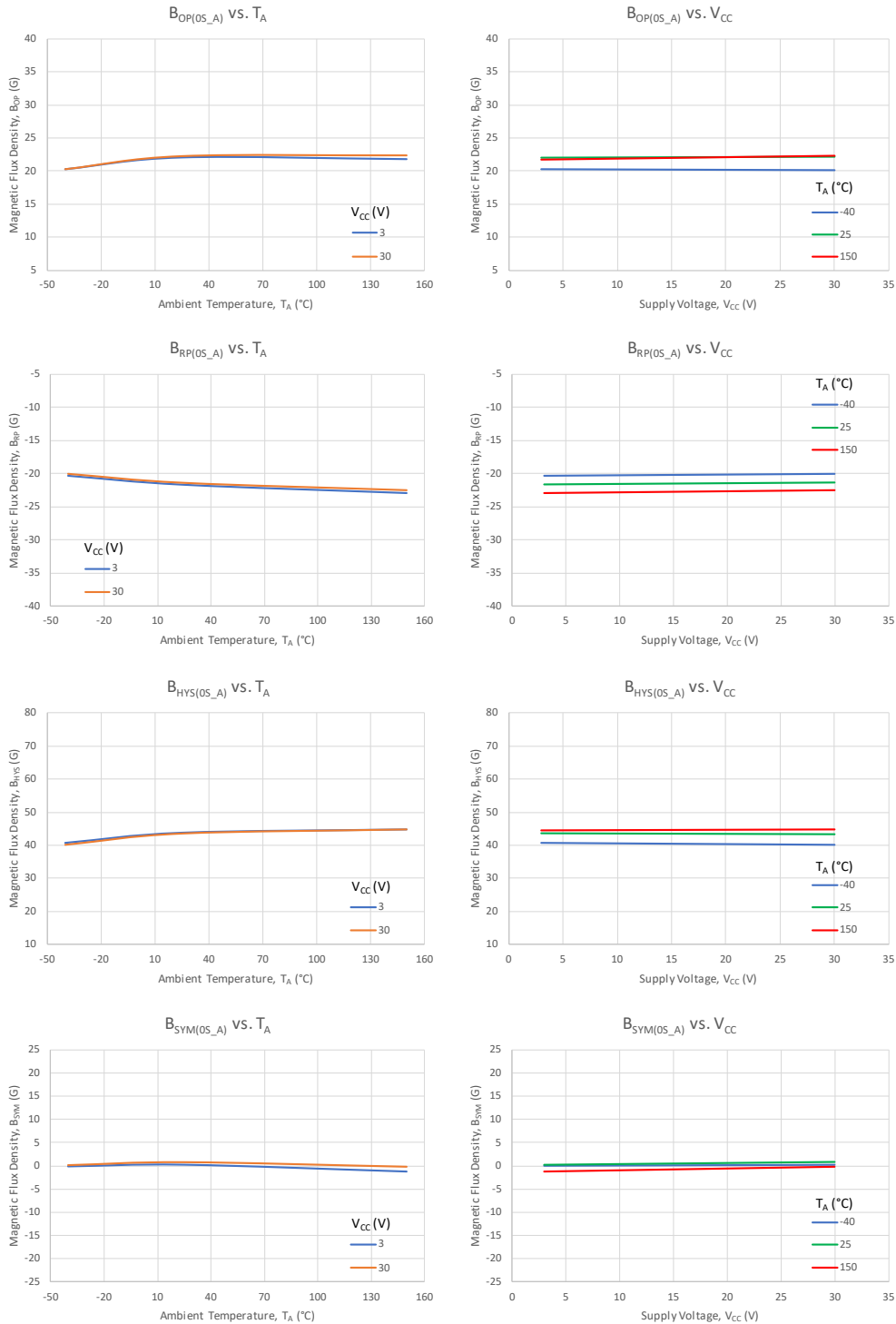
CHARACTERISTIC PERFORMANCE DATA



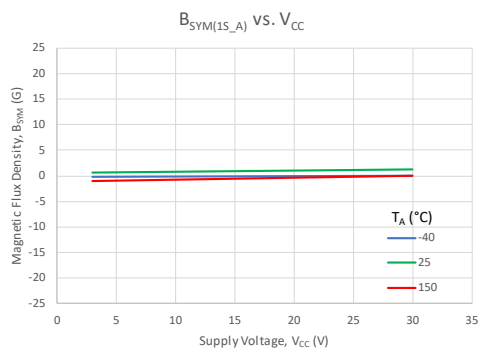
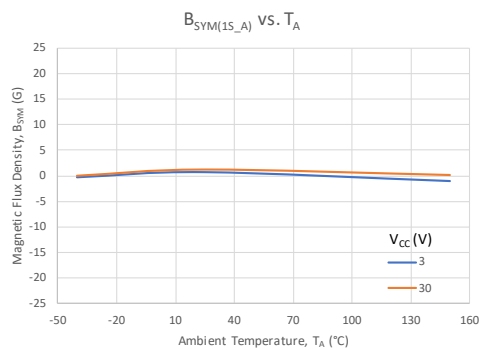
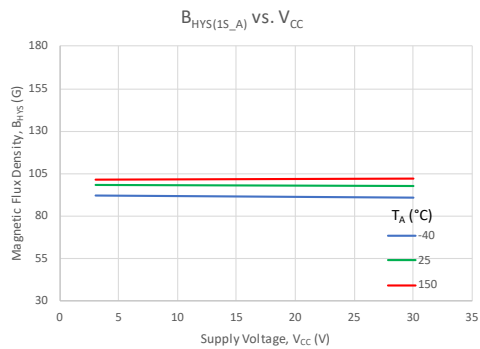
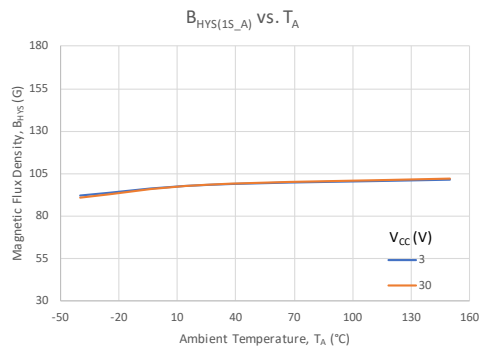
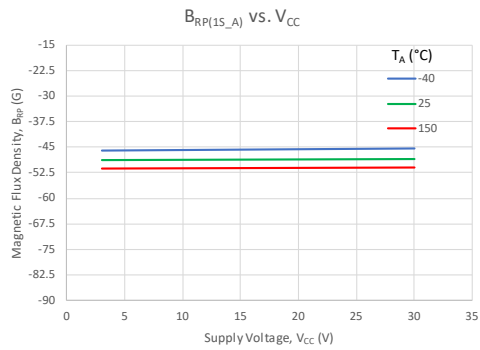
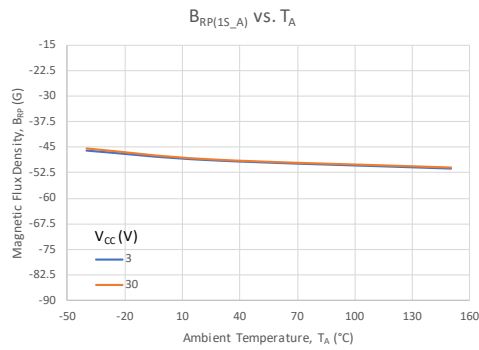
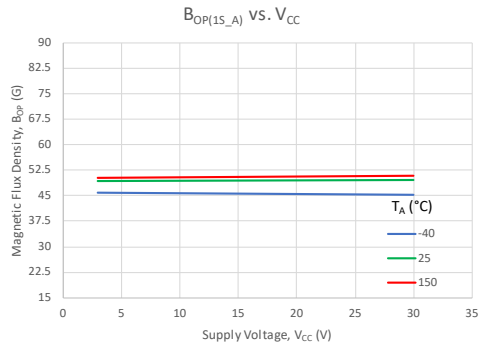
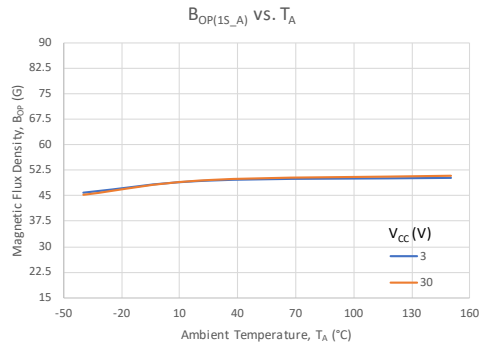
CHARACTERISTIC PERFORMANCE DATA (continued)



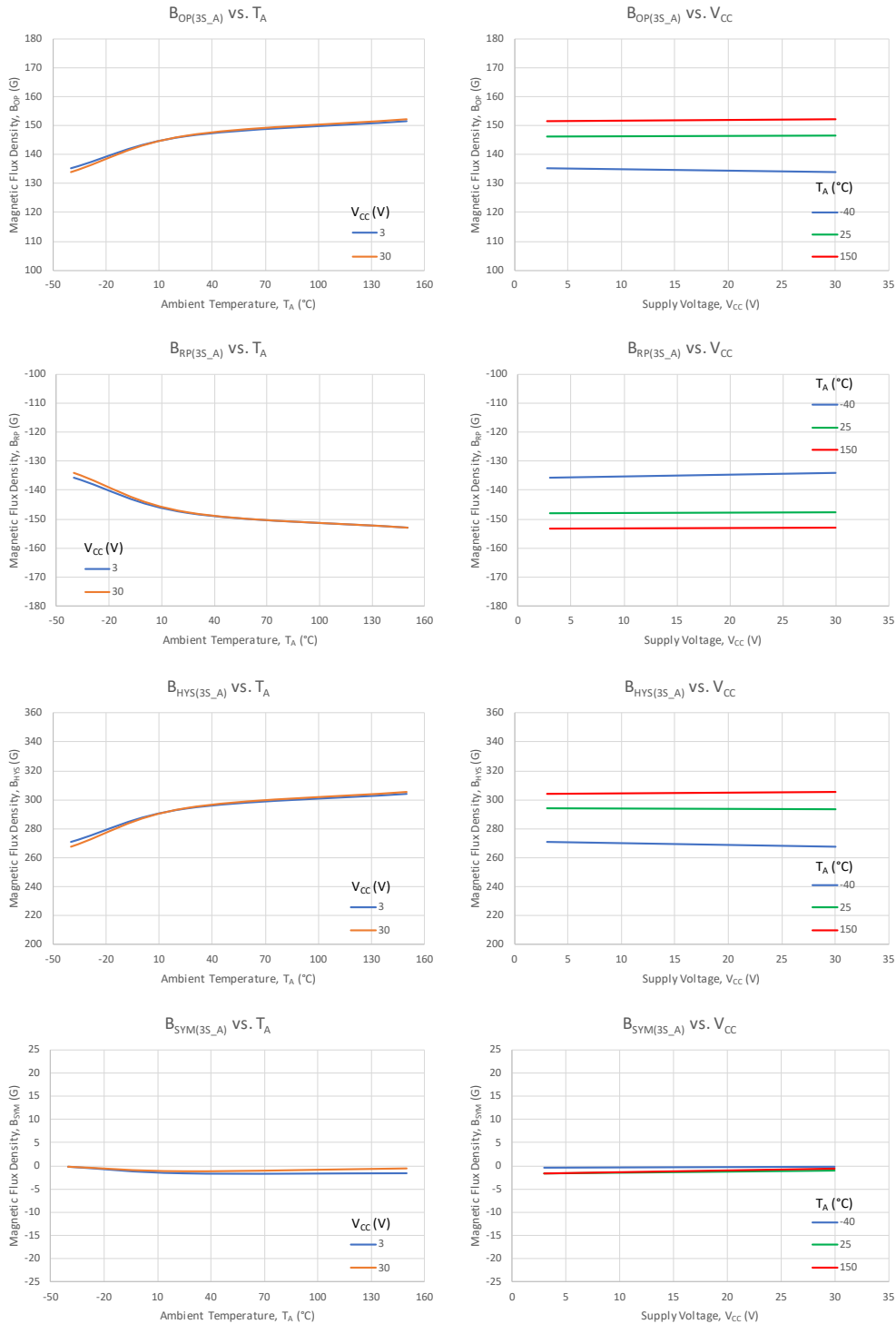
CHARACTERISTIC PERFORMANCE DATA APS12450-0SxA



CHARACTERISTIC PERFORMANCE DATA APS12450-1SxA



CHARACTERISTIC PERFORMANCE DATA APS12450-3SxA



FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches when a magnetic field perpendicular to the Hall-effect sensor exceeds the operate point threshold (B_{OP}). When the magnetic field is reduced below the release point (B_{RP}), the device output switches to the alternate state. The output state (polarity) and magnetic field polarity depends on the selected device options. The device is a latch, therefore B_{OP} and B_{RP} will be in opposite magnetic field polarities.

The difference between operate (B_{OP}) and release (B_{RP}) points is the hysteresis (B_{HYS}). Hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The hysteresis is set to double the programmed operating point.

Figure 1 shows the output switching behavior relative to increasing and decreasing magnetic field. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength. Figure 2 shows the sensing orientation of the magnetic field, relative to the device package.

Note that this device *latches*; that is, a south pole of sufficient strength towards the branded face of the device turns the device on, and the device remains on with removal of the south pole.

Figure 1 shows the potential unipolar and omnipolar options and output polarity options of the APS12450 that can be configured. The direction of the applied magnetic field is perpendicular to the branded face of the APS12450 (see Figure 2).

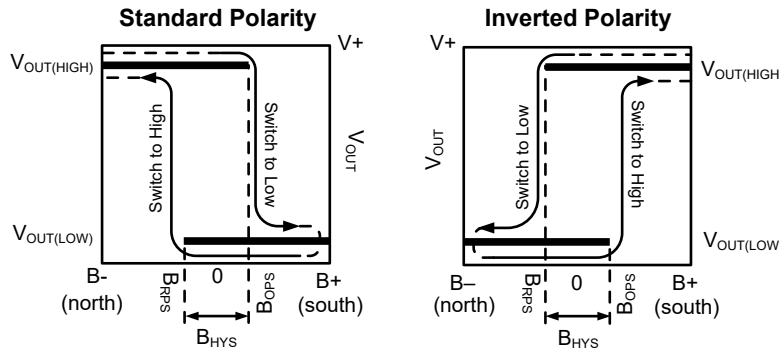


Figure 1: Hall latch magnetic and output polarity options
 B- indicates increasing north polarity magnetic field strength, and
 B+ indicates increasing south polarity magnetic field strength.

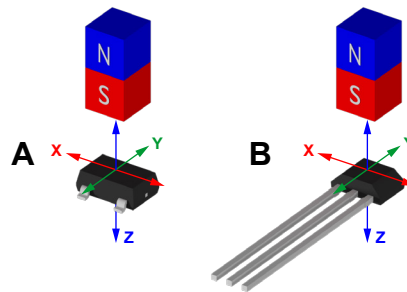


Figure 2: Magnetic Sensing Orientations
 APS12450 LH (Panel A), APS12450 UA (Panel B)

FUNCTIONAL SAFETY

The APS12450 was developed in accordance with the international standard for automotive functional safety, ISO 26262:2011. This product achieves an Automotive Safety Integrity Level (ASIL) rating of ASIL B according to the standard.

Diagnostics Mode Operation

The APS12450 features a proprietary diagnostics routine that meets ASIL B safety requirements. This internal diagnostics routine continuously runs in the background, monitoring all key subsystems of the IC. These subsystems are shown in Table 1 and Figure 3. The diagnostic scheme runs at high speed and provides minimal impact on device performance. Signal path diagnostics are injected and measured in less than 2 μs , while all other diagnostics are running in real time in the background. The Hall element biasing circuit and voltage regulator are checked for valid operation, and the digital and non-volatile memory blocks are checked for valid device configuration.

The signal path monitoring system verifies two internal state

transitions (B_{OP} and B_{RP} within limits) under normal operation. In cases when these output transitions do not occur, or if another internal fault is detected, the output will go to the fault state (see “Three-Wire Diagnostic Output” section).

In the event of an internal fault, the device will continuously run the diagnostics routine every 2 ms (t_{DIAGF}). The periodic recovery attempt sequence allows the device to continually check for the presence of a fault and return to normal operation if the fault condition clears.

In the case where the fault is no longer present, the output will resume normal operation. However, if the fault is persistent, the device will not exit fault mode and the output voltage will continue to be $V_{OUT(FAULT)}$.

When a system rating higher than ASIL B is required, additional external safety measures may be employed (e.g., sensor redundancy and rationality checks, etc.). Refer to the device safety manual for additional details about the diagnostics.

Table 1: Diagnostics Coverage

	Feature	Coverage
1	Hall plate	Connectivity and biasing of Hall plate
2	Signal path	Signal path and Schmitt trigger
3	Voltage regulator	Regulator voltage for normal operation
4	Digital subsystem	Digital subsystem and non-volatile memory
5	Entire system	Overtemperature and redundancies for single point failures
6	Output	Output verified through valid regulations states (external monitor)

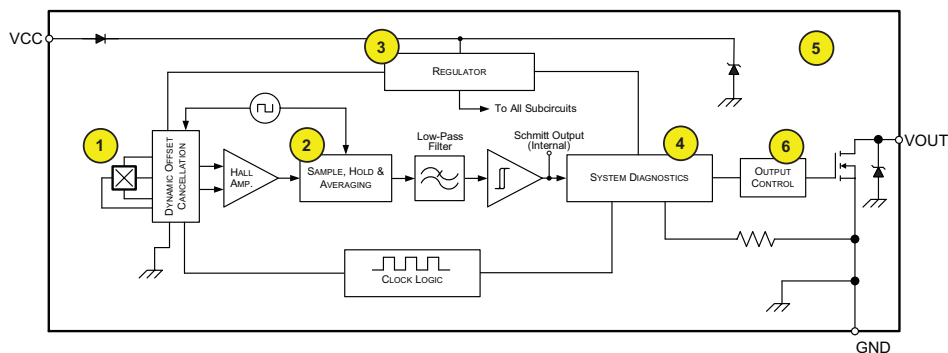


Figure 3: Diagnostics Coverage Block Diagram

Power-On Behavior

During Power-on, the output voltage is in the fault state ($V_{OUT(FAULT)}$), which is the pull-up voltage (V_{PU}), until the device is ready to respond appropriately to the input magnetic field ($t > t_{ON}$). If the device powers-on with the field within the hysteresis band, the output will switch from $V_{OUT(FAULT)}$ to the off state ($V_{OUT(HIGH)}$) with standard output polarity as shown in Figure 4. For inverted output polarity operation, the output will switch from $V_{OUT(FAULT)}$ to $V_{OUT(LOW)}$ (not shown).

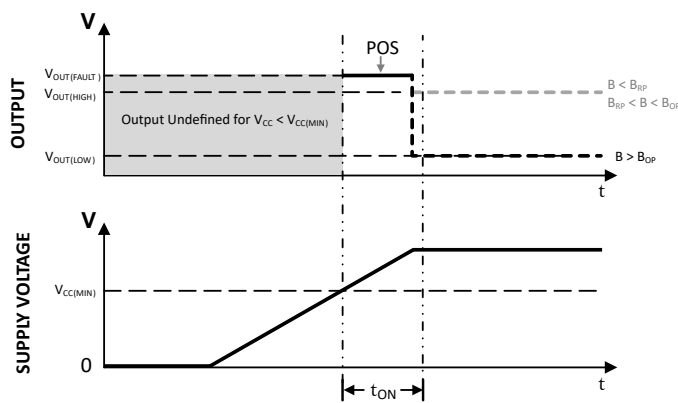


Figure 4: Power-On Sequence

Temperature Coefficient and Magnet Selection

The APS12450 allows the user to select the magnetic temperature coefficient to compensate for drifts of SmCo, NdFeB, and ferrite magnets over temperature, as indicated in the Magnetic Characteristics specifications table. This compensation improves the magnetic system performance over the entire temperature range. For example, the magnetic field strength from NdFeB decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as -40°C, due to the higher magnetic field strength from the NdFeB magnet. The APS12450 compensates the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

A sample calculation is provided in the “Applications Information” section.

Three-Wire Diagnostic Output

Three-wire diagnostic output enables the user to identify various fault conditions external to the IC, in addition to the internal fault detection. The output low ($V_{OUT(LOW)}$) and high ($V_{OUT(HIGH)}$) states are ratiometric to the pull-up voltage, with low and high states being 20% and 80% respectively. For example, a V_{CC} and

$V_{PULL-UP}$ of 5 V, the output state levels will be 1.0 V and 4.0 V ± 0.5 V. The output RC time constant (τ) must be less than 3 μ s (e.g., $R_{PU} = 3$ k Ω and $C_{OUT} = 1$ nF), and V_{PU} must be equal to V_{CC} (recommend pulling up V_{OUT} directly to V_{CC}).

Under normal operation (Figure 5), the output switches between the $V_{OUT(LOW)}$ (20%) and $V_{OUT(HIGH)}$ (80%) states.

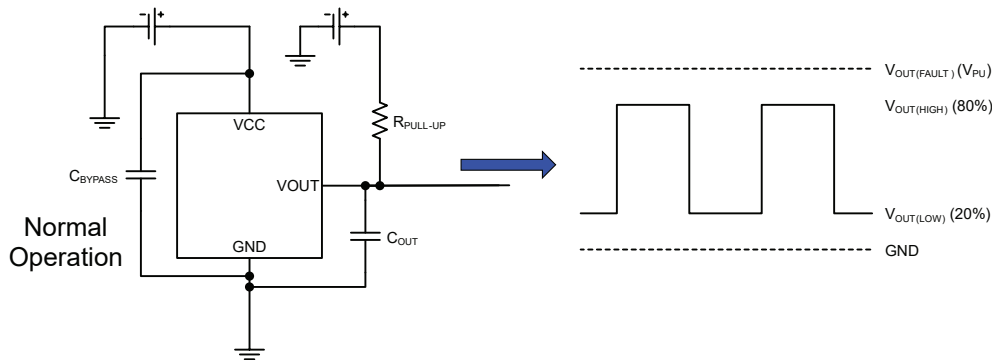


Figure 5: The APS12450 diagnostic output under normal operation (no fault detected)

With various opens and shorts on any of the IC pins, the output will no longer be controlled by the IC. The output itself may continue to switch, depending on the external connectivity fault; however, the output level(s) observed will deviate from the 20% and 80% (of V_{PU}) output levels.

If an internal fault is detected via diagnostics monitoring, the output will be set to the fault state, $V_{OUT(FAULT)}$, which is equal to the pull-up voltage, V_{PU} .

Any output voltage levels outside of the valid $V_{OUT(HIGH)}$ and $V_{OUT(LOW)}$ ranges indicates a fault as shown in Figure 6. The observed voltage on VOUT relative to potential fault conditions are summarized in Table 2.

The output relative to the fault condition is summarized in Table 2 below.

Table 2: Fault Conditions and Resulting Output Level

Fault	Output Level
No Fault	20% or 80% of V_{PU} , respectively
Short, VCC-VOUT	V_{CC}
Short, VOUT-GND	GND
Short, VCC-GND	V_{PU}
Open, VCC	V_{PU}
Open, VOUT	V_{PU}
Open, GND	V_{PU}
Internal Fault	V_{PU}

Note: $V_{OUT(FAULT)} \leq V_{PULL-UP}$ and $V_{PULL-UP} = V_{CC}$.

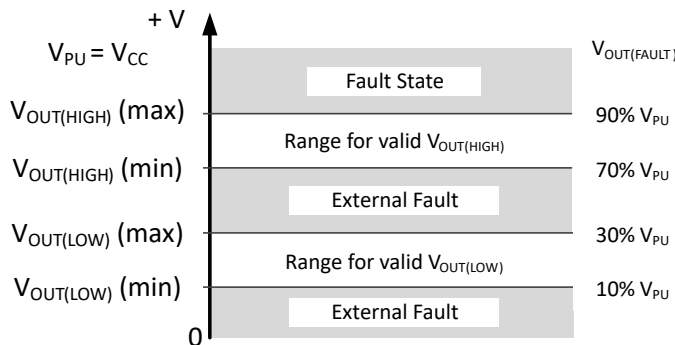


Figure 6: APS12450 valid (normal) and fault condition output levels

Fault Detection and Retry

The fault detection diagnostics runs continuously in the background during normal operation after the device has powered-on. In the event a fault is detected, the output will immediately change to the

$V_{OUT(FAULT)}$ state. The diagnostics will continue to retry the diagnostics approximately every 2 ms. If the fault recovers, the output will return to normal operation. See Figure 7.

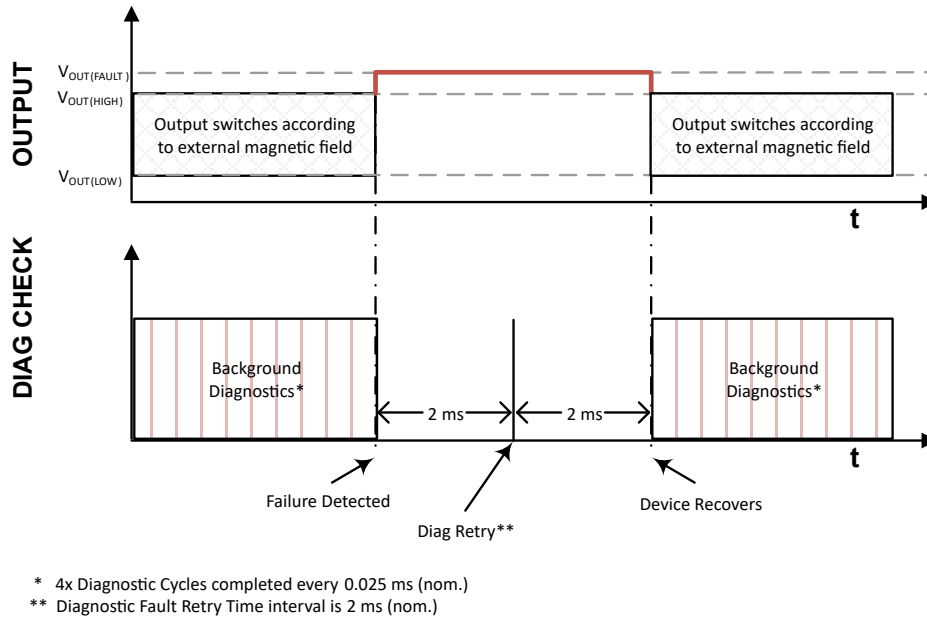


Figure 7: Fault Detection and Retry

Output Overshoot

When the output switches from $V_{OUT(LOW)}$ to $V_{OUT(HIGH)}$, depending upon the RC circuit, a small overshoot can occur ($V_{OUT(H)OVER}$). $V_{OUT(H)OVER}$ is specified as a percentage of $V_{PULL-UP}$ (and/or V_{CC} , which need to be the same). Therefore with an RC Time Constant (τ) of 3 μ s (see the “Applications Information” section), a nominal overshoot of 2% is possible. With $V_{PULL-UP}$ at 5.0 V, the output may overshoot by 0.1 V, for less than 5 μ s ($t_{VOUT(H)OVER}$). Figure 7 demonstrates output edge profile.

For example, with a 5 V pull-up, if $V_{OUT(HIGH)}$ is at the upper limit (90%), $V_{OUT(HIGH)}$ will be 4.5 V. With a τ of 3 μ s at room temperature, the output can briefly reach 4.6 V until it settles to 4.5 V. Since $V_{OUT(HIGH)}$ is valid between 70% and 90%, or 3.5 and 4.5 V,

this condition is not out of specification. The Output Off Voltage Overshoot specification pertains only to conditions where the overshoot is greater than the $V_{OUT(HIGH)MAX}$ specification.

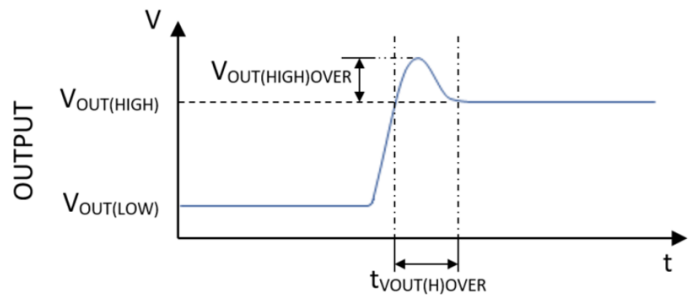


Figure 8: Output Overshoot

APPLICATIONS INFORMATION

Typical Applications

For the LH and UA packages, an external bypass capacitor, C_{BYP} , should be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in Figure 9, a 0.1 μF bypass capacitor is typical, with an optional output capacitor, C_{OUT} (recommended 1 nF).

The time constant of the RC circuit (τ) on output must be less than 3 μs , where:

$$\begin{aligned} \tau &= R_{PULLUP} \times C_{OUT} \\ &= 3 \text{ k}\Omega \times 1 \text{ nF} \\ &= 3 \mu\text{s} \end{aligned}$$

The resistor, R_{PULLUP} , must be between 2 and 30 k Ω .

Temperature Compensation

To calculate the typical effect of the TC_{SENS} on B_{OP} (or B_{RP}), simply multiply the B_{OP} at the starting temperature by TC_{SENS} and the change in temperature.

Sample B_{OP} calculation for TC_{SENS} compensation from 25°C to 150°C, for $TC_{SENS} = -0.12\%/^{\circ}\text{C}$, and $B_{OP(25C)} = 180 \text{ G}$:

$$\Delta T_A = 150^{\circ}\text{C} - 25^{\circ}\text{C} = 125^{\circ}\text{C}$$

$$\begin{aligned} B_{OP(150C)} &= B_{OP(25C)} + (B_{OP(25C)} \times TC \times \Delta T_A) \\ &= 180 \text{ G} + (180 \text{ G} \times -0.12\%/^{\circ}\text{C} \times 125^{\circ}\text{C}) \\ &= 180 \text{ G} + (-27 \text{ G}) \\ &= 153 \text{ G} \end{aligned}$$

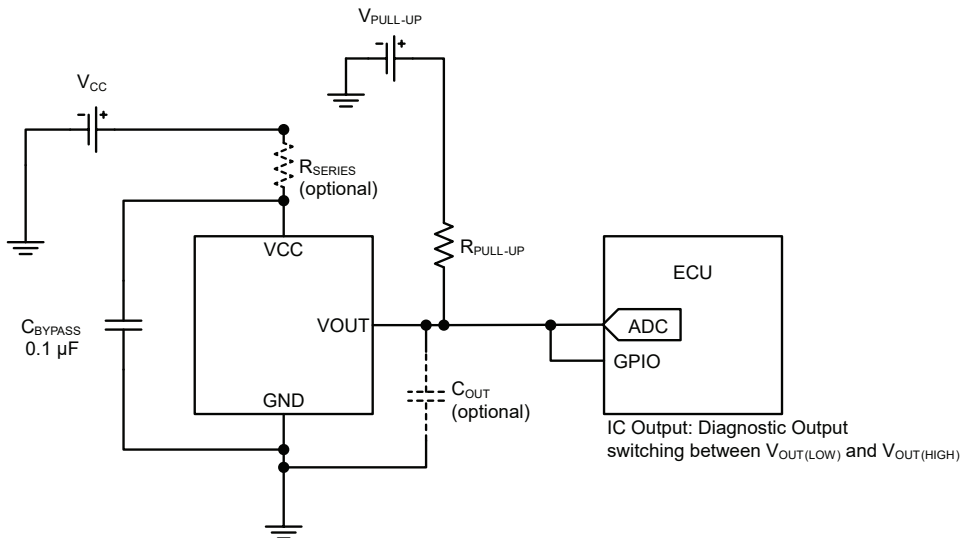


Figure 9: Typical Applications Circuits Diagnostic Output

	Diagnostic Output*
V_{CC}	3 to 30 V
V_{PU}	V_{CC}
C_{BYP}	0.1 μF
C_{OUT}	$\tau_{RC} < 3 \mu\text{s}$
R_{PU}	$I_{OUT} < 12 \text{ mA}$ $\tau_{RC} < 3 \mu\text{s}$ $2 \text{ k}\Omega < R < 30 \text{ k}\Omega$
R_S	100 Ω^*

* The following application circuit conditions are required

- The τ of the RC on output must be $< 3 \mu\text{s}$.
- $2 \text{ k}\Omega < R_{PU} < 30 \text{ k}\Omega$.
- $V_{PU} = V_{CC}$ (recommend pulling VOUT up to VCC).

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide*, AN27701
- *Guidelines For Designing Subassemblies Using Hall-Effect Devices*, AN27703.1
- *Soldering Methods for Allegro's Products – SMT and Through-Hole*, AN26009
- *Functional Safety Challenges to the Automotive Supply Chain* (<https://www.allegromicro.com/en/Design-Center/Technical-Documents/General-Semiconductor-Information/Functional-Safety-Challenges-Automotive-Supply-Chain.aspx>)

All are provided on the Allegro website:

www.allegromicro.com

Chopper Stabilization Technique

A limiting factor for switchpoint accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. “Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)” illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The

subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro’s innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12450 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

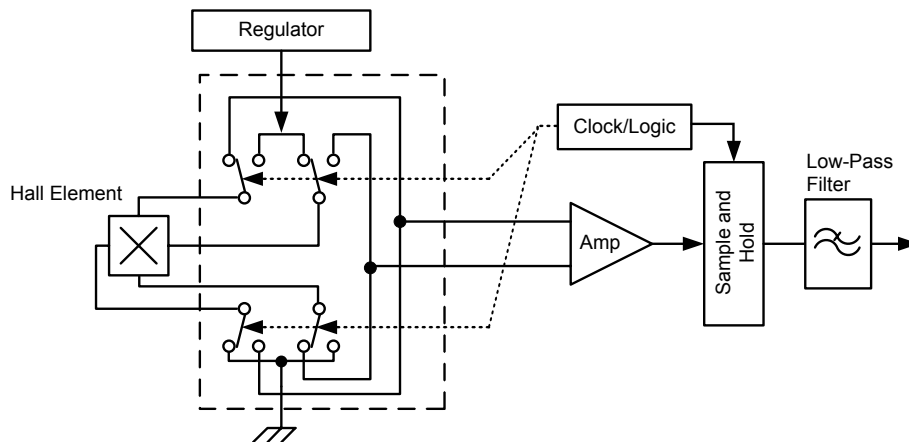


Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

POWER DERATING

The device must be operated below the maximum junction temperature, T_J (max). Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance (junction to ambient), $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K , of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A , and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions: $T_A = 25^\circ\text{C}$, $V_{CC} = 12\text{ V}$, $I_{CC} = 4\text{ mA}$, and $R_{\theta JA} = 110^\circ\text{C/W}$ for the LH package, then:

$$P_D = V_{CC} \times I_{CC} = 12\text{ V} \times 4\text{ mA} = 48\text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 48\text{ mW} \times 110^\circ\text{C/W} = 5.28^\circ\text{C}$$

$$T_J = T_A + \Delta T = 25^\circ\text{C} + 5.28^\circ\text{C} = 31.28^\circ\text{C}$$

Determining Maximum V_{CC}

For a given ambient temperature, T_A , the maximum allowable power dissipation as a function of V_{CC} can be calculated. P_D (max) represents the maximum allowable power level without exceeding T_J (max) at a selected $R_{\theta JA}$ and T_A .

Example: V_{CC} at $T_A = 150^\circ\text{C}$, package UA, using low-K PCB. Using the worst-case ratings for the device, specifically: $R_{\theta JA} = 165^\circ\text{C/W}$, T_J (max) = 165°C , V_{CC} (max) = 24 V , and I_{CC} (max) = 4 mA , calculate the maximum allowable power level, P_D (max). First, using equation 3:

$$\Delta T (max) = T_J (max) - T_A = 165^\circ\text{C} - 150^\circ\text{C} = 15^\circ\text{C}$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, from equation 2:

$$P_D (max) = \Delta T (max) \div R_{\theta JA} = 15^\circ\text{C} \div 165^\circ\text{C/W} = 91\text{ mW}$$

Finally, using equation 1, solve for maximum allowable V_{CC} for the given conditions:

$$V_{CC} (est) = P_D (max) \div I_{CC} (max) = 91\text{ mW} \div 4\text{ mA} = 22.8\text{ V}$$

The result indicates that, at T_A , the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC}$ (est).

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must be improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum T_A

In cases where the V_{CC} (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature T_A (max), for example, in a worst-case scenario with conditions V_{CC} (max) = 40 V , I_{CC} (max) = 4 mA , and $R_{\theta JA} = 228^\circ\text{C/W}$ for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 40\text{ V} \times 4\text{ mA} = 160\text{ mW}$$

Then, by rearranging equation 3 and substituting with equation 2:

$$T_A (max) = T_J (max) - \Delta T$$

$$T_A (max) = 165^\circ\text{C} - (160\text{ mW} \times 228^\circ\text{C/W})$$

$$T_A (max) = 165^\circ\text{C} - 36.5^\circ\text{C} = 128.5^\circ\text{C}$$

In another example, the maximum supply voltage is equal to V_{CC} (min). Therefore, V_{CC} (max) = 3 V and I_{CC} (max) = 4 mA . By using equation 1 the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 3\text{ V} \times 4\text{ mA} = 12\text{ mW}$$

Then, by rearranging equation 3 and substituting with equation 2:

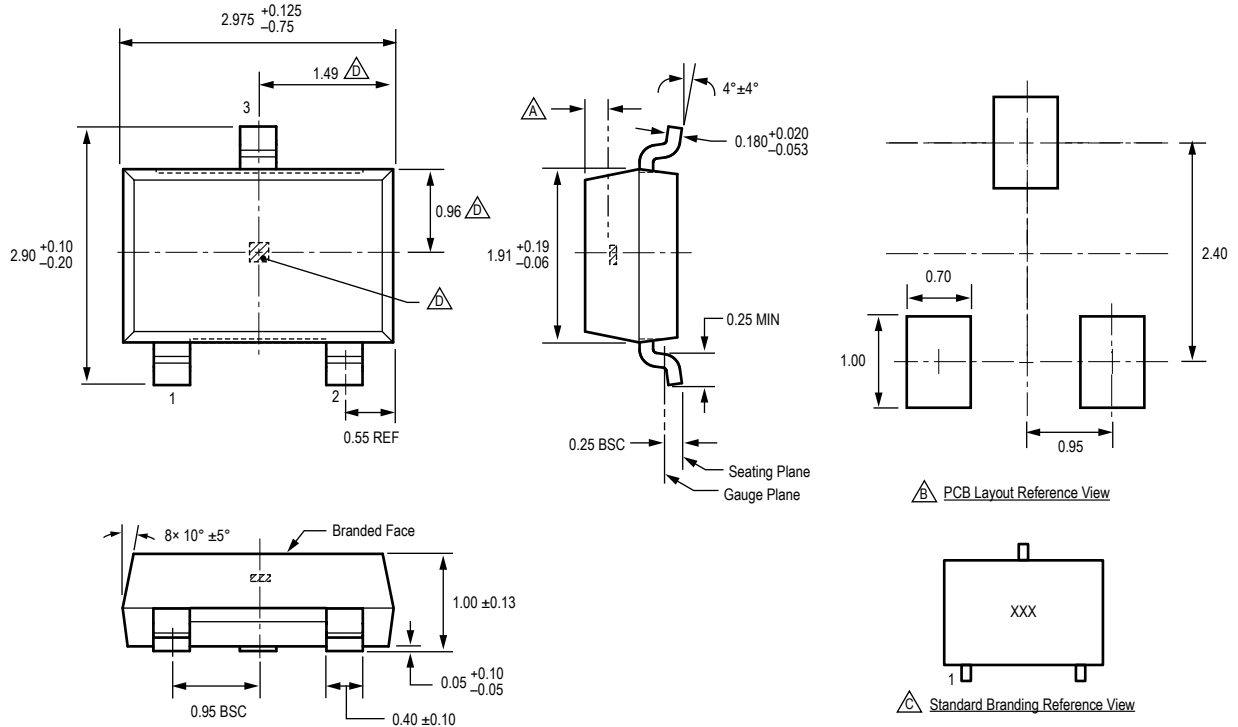
$$T_A (max) = T_J (max) - \Delta T$$

$$T_A (max) = 165^\circ\text{C} - (12\text{ mW} \times 228^\circ\text{C/W})$$

$$T_A (max) = 165^\circ\text{C} - 11.6^\circ\text{C} = 162.3^\circ\text{C}$$

The example above indicates that at $V_{CC} = 3\text{ V}$ and $I_{CC} = 4\text{ mA}$, the T_A (max) can be as high as 162.3°C without exceeding T_J (max). However the T_A (max) rating of the device is 150°C ; the device performance is not guaranteed above $T_A = 150^\circ\text{C}$.

Package LH, 3-Pin SOT23W

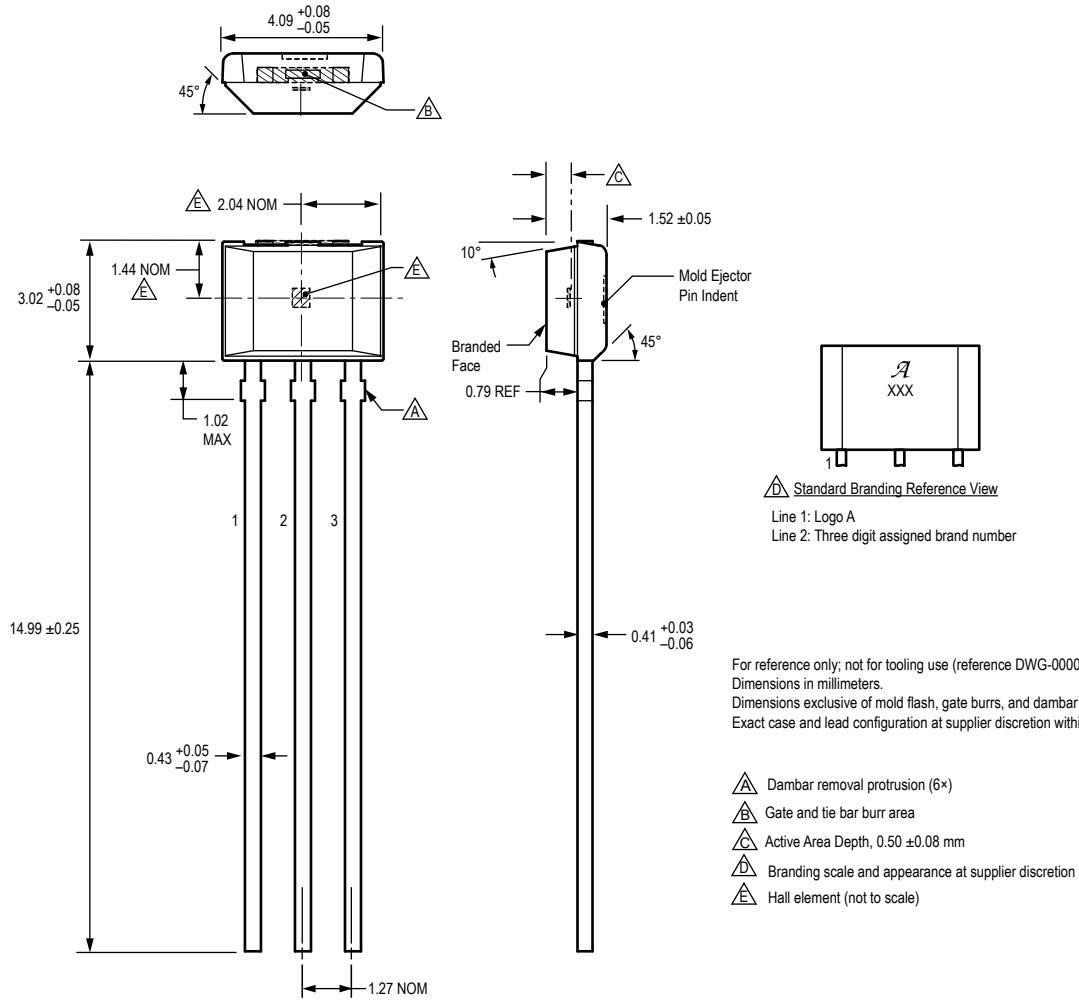


For reference only; not for tooling use (reference DWG-0000628, Rev. 1).
 Dimensions in millimeters.
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions.
 Exact case and lead configuration at supplier discretion within limits shown.

- △ Active Area Depth, 0.28 ±0.04 mm
- △ Reference land pattern layout
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
- △ Branding scale and appearance at supplier discretion
- △ Hall element, not to scale

Line 1 = Three digit assigned brand number

Package UA, 3-Pin SIP, Matrix HD Style



REVISION HISTORY

Number	Date	Description
–	January 31, 2019	Initial release

Copyright ©2019, Allegro MicroSystems, LLC

Allegro MicroSystems, LLC reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, LLC assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:

www.allegromicro.com

