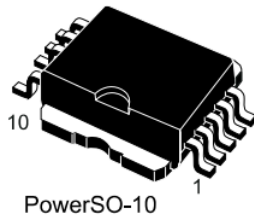


Quad high-side smart power solid-state relay



Features

- Output current: 0.7 A per channel
- Digital input clamped at 32 V minimum voltage
- Shorted load and overtemperature protections
- Built-in current limiter
- Undervoltage shutdown
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

Product status link

[VN330SP-E](#)

Product label



Applications

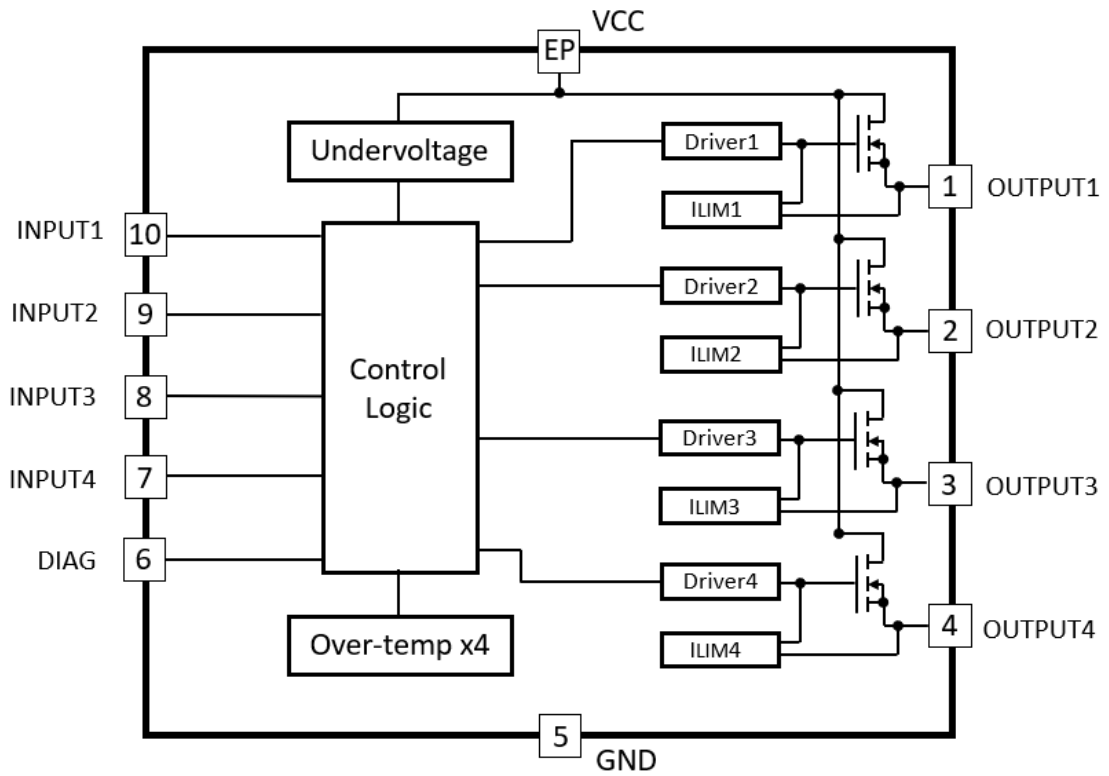
- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines

Description

The VN330SP-E is a monolithic device developed using VIPower technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation prevents dropping of the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. The open drain diagnostic output indicates overtemperature conditions.

1 Block diagram

Figure 1. Block diagram



2 Pin connection

Figure 2. Connection diagram (top view)

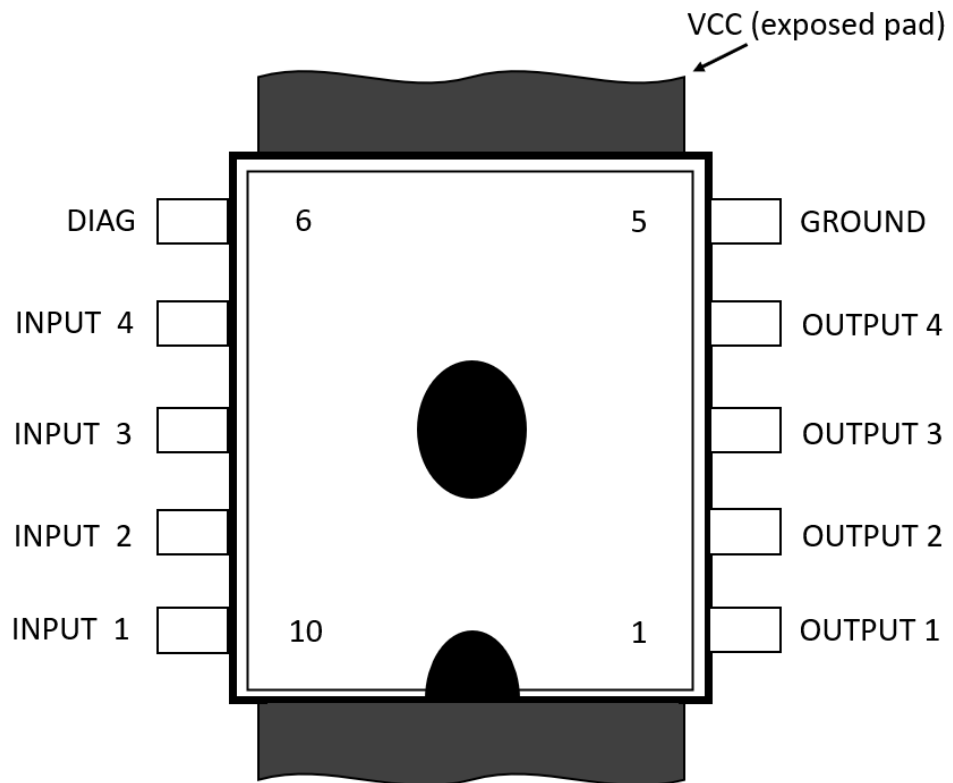
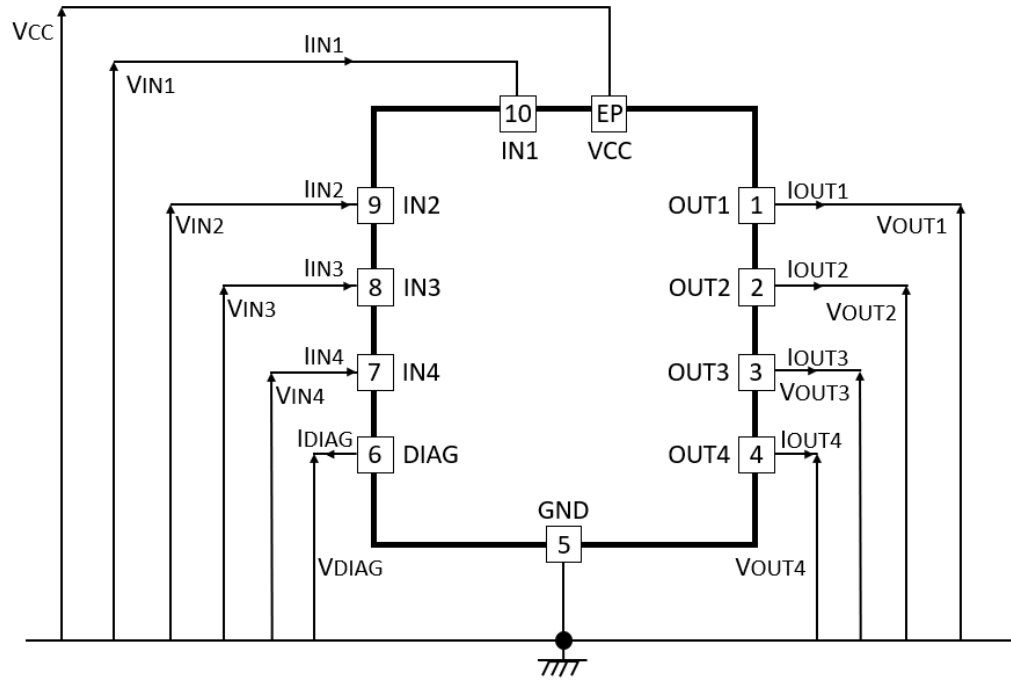


Figure 3. Current and voltage conventions



3 Maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-0.3	V
I_{OUT}	Output current	Internally limited	A
I_R	Reverse output current (per channel)	-6	A
I_{IN}	Input current range	± 10	mA
I_{DIAG}	DIAG pin current	± 10	mA
V_{ESD}	Electrostatic discharge (R = 1.5 k Ω ; C = 100 pF)	2000	V
E_{AS}	Single pulse avalanche energy, all channels active simultaneously, $T_{amb} = 125\text{ }^{\circ}\text{C}$, $I_{LOAD} = 0.625\text{ A}$	4	J
P_{TOT}	Power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	Internally limited	W
T_J	Junction operating temperature	Internally limited	$^{\circ}\text{C}$
T_{STG}	Storage temperature	-55 to 150	$^{\circ}\text{C}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case ⁽¹⁾	Max. 2	$^{\circ}\text{C}/\text{W}$
$R_{th(JA)}$	Thermal resistance junction-ambient ⁽²⁾	Max. 50	$^{\circ}\text{C}/\text{W}$

1. Per channel.

2. When mounted on a four-layer FR-4, with the minimum recommended pad size.

4 Electrical characteristics

10 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C; unless otherwise specified

Table 3. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC}	Supply voltage		10		36	V
R _{DS(on)}	On-state resistance	I _{OUT} = 0.5 A at T _J = 25 °C			0.2	Ω
		I _{OUT} = 0.5 A at T _J = 85 °C			0.32	
		I _{OUT} = 0.5 A at T _J = 125 °C			0.44	
I _S	Supply current	All channels OFF			1	mA
		On-state V _{IN} = 5 V, I _{OUT} = 0 V, T _J = -40 °C			15	mA
V _{demag}	Output voltage at turn-off	I _{OUT} = 0.5 A; L _{LOAD} ≥ 1 mH	V _{CC} -65	V _{CC} -55	V _{CC} -45	V

Table 4. Switching (V_{CC} = 24 V, R_{LOAD} = 48Ω, see Figure 8. Switching parameter test conditions)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(ON)}	Turn-on delay time of output current	Input rise time < 0.1 μs, T _J = 25 °C		30	40	μs
		Input rise time < 0.1 μs, T _J = 125 °C			60	
t _r	Rise time of output current	Input rise time < 0.1 μs, T _J = 25 °C		50	100	μs
		Input rise time < 0.1 μs, T _J = 125 °C			115	
t _{d(OFF)}	Turn-off delay time of output current	Input rise time < 0.1 μs, T _J = 25 °C		20	30	μs
		Input rise time < 0.1 μs, T _J = 125 °C			40	
t _f	Fall time of output current	Input rise time < 0.1 μs, T _J = 25 °C		8	15	μs
		Input rise time < 0.1 μs, T _J = 125 °C			20	
(di/dt) _{on}	Turn-on current slope	Normal operation			0.5	A/μs
		I _{OUT} = I _{LIM} , T _J = 25 °C			2	
(di/dt) _{off}	Turn-off current slope	Normal operation			2	A/μs
		I _{OUT} = I _{LIM} , T _J = 25 °C			4	

Table 5. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Input low level voltage				2	V
V_{IH}	Input high level voltage		3.5			V
$V_{I(HYST)}$	Input hysteresis voltage			0.5		V
I_{IN}	Input current	$V_{IN} = 0$ to 30 V			600	μ A
I_{LGND}	Output current in ground disconnection	$V_{CC} = V_{IN} = V_{GND} = V_{DIAG} = 24$ V; $T_J = 25$ °C			25	mA
V_{ICL}	Input clamp voltage ⁽¹⁾	$I_{IN} = 1$ mA	32	36		V
		$I_{IN} = -1$ mA		-0.7		

1. The input voltage is internally clamped at 32 V minimum, the input pins can be connected to a higher voltage by an external resistor, which cannot exceed 10 mA

Table 6. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DIAG}^{(1)}$	Status voltage output low	$I_{DIAG} = 5$ mA (fault condition)			1	V
$V_{SCL}^{(1)}$	Status clamp voltage	$I_{DIAG} = 1$ mA	32	36		
		$I_{DIAG} = -1$ mA		-0.7		
V_{USD}	Undervoltage shutdown		5		8	V
V_{OL}	Low state output voltage	$V_{IN} = V_{IL}$; $R_{LOAD} \geq 10$ m Ω			1.5	V
I_{LIM}	DC short-circuit current	$V_{CC} = 24$ V; $R_{LOAD} < 10$ m Ω	0.7		2.5	A
I_{OVPK}	Peak short-circuit current	$V_{CC} = 24$ V; $V_{IN} = 30$ V; $R_{LOAD} < 10$ m Ω			4	A
I_{DIAGH}	Leakage on DIAG pin in high state	$V_{DIAG} = 24$ V			100	μ A
I_{LOAD}	Output leakage current	$V_{CC} = 10$ to 36 V; $V_{IN} = V_{IL}$			50	μ A
t_{SC}	Delay time of current limiter				100	μ s
T_{TSD}	Thermal shutdown temperature		150	170		°C
T_R	Thermal reset temperature		135	155		°C

1. Status determination > 100 μ s after the switching edge.

Note: If the INPUT pin is left floating, the corresponding channel automatically switches off. If GND pin is disconnected, the channel switches off provided that V_{CC} does not exceed 36 V.

5 Test circuits

Figure 4. Avalanche energy test circuit

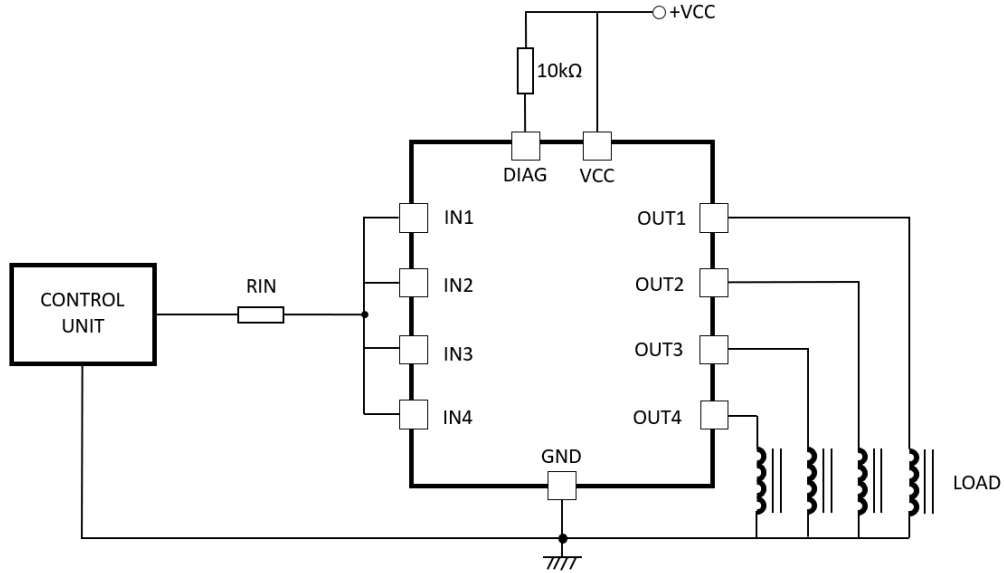
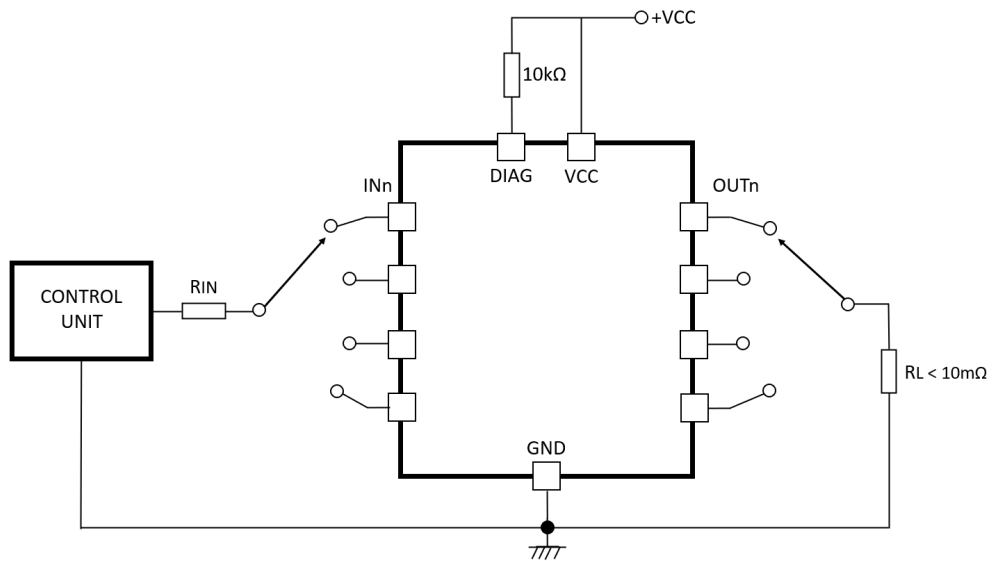


Figure 5. Peak short-circuit test diagram



6 Switching time waveforms and truth table

Table 7. Truth table

Conditions	INPUTn	OUTPUTn	Diagnostic
Normal operation	L	L	H
	H	H	H
Overtemperature	L	L	H
	H	L	L
Undervoltage	L	L	H ⁽¹⁾
	H	L	H ⁽¹⁾
Shorted load (current limitation)	L	L	H
	H	H ⁽²⁾	H

1. DIAG pin is considered pulled-up at application voltage level

2. $V_{OUT} = R_{LOAD} \times I_{LIM}$

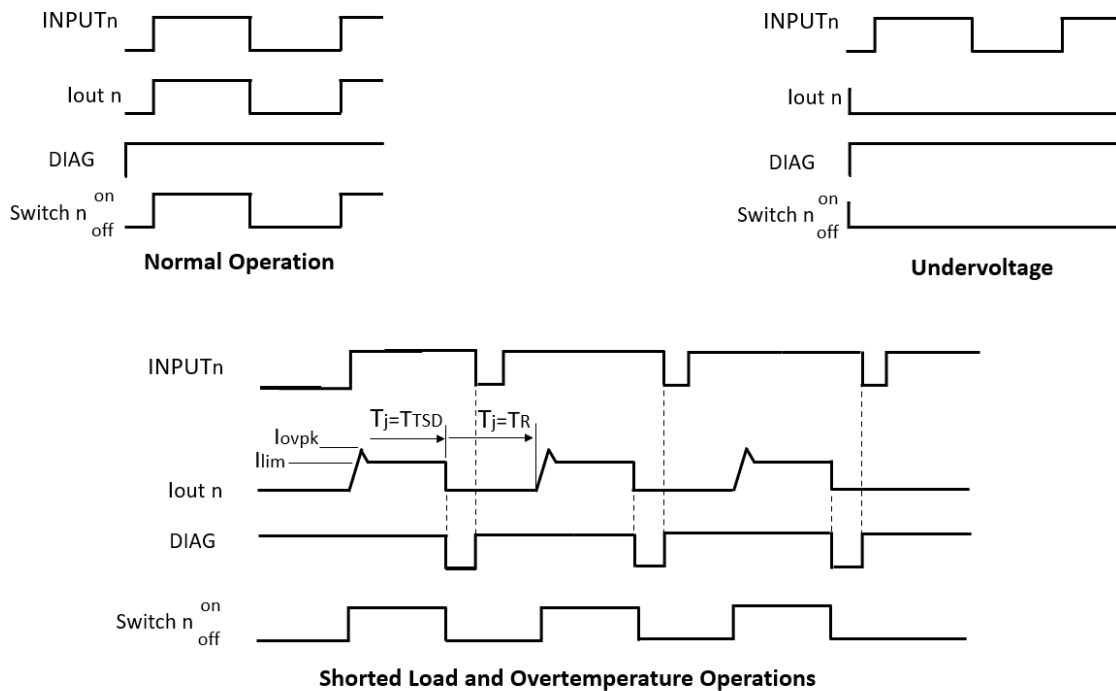
Figure 6. Switching waveforms


Figure 7. Switching parameter test conditions

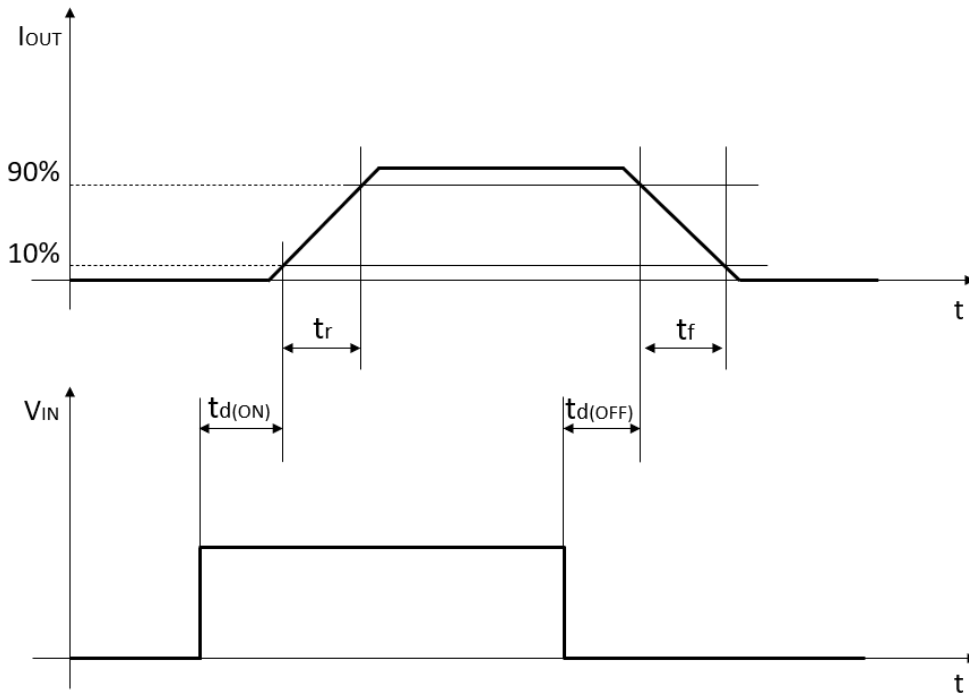
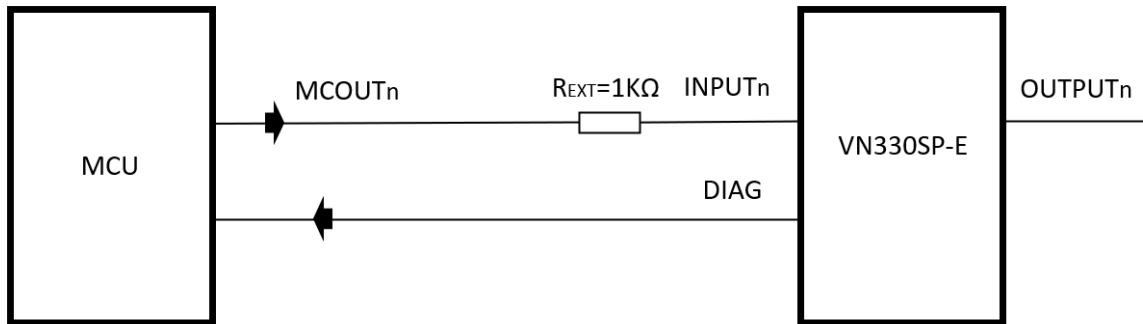


Figure 8. Driving circuit

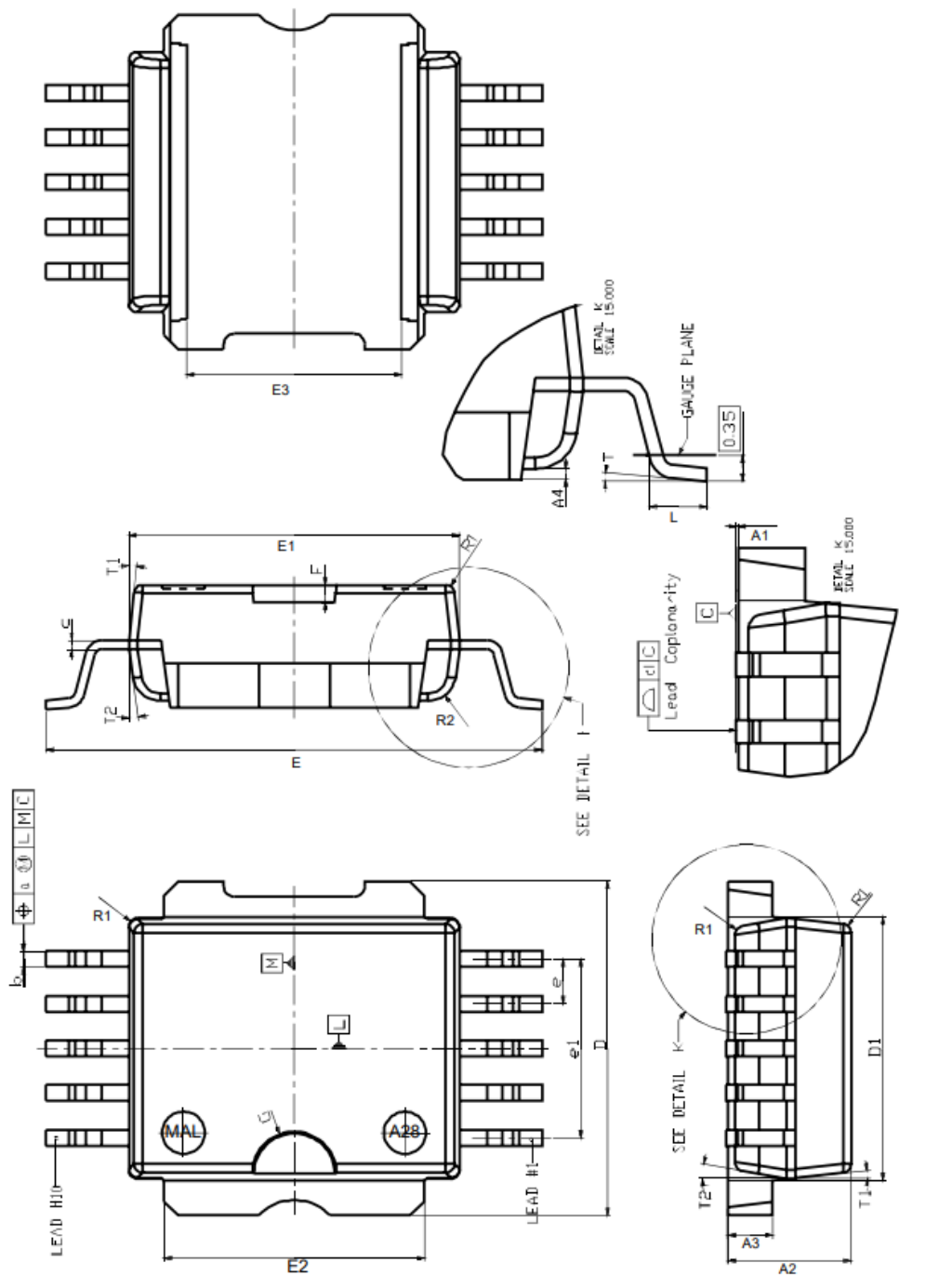


7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 PowerSO-10 package information

Figure 9. PowerSO-10 package outline



7152835 rev.G

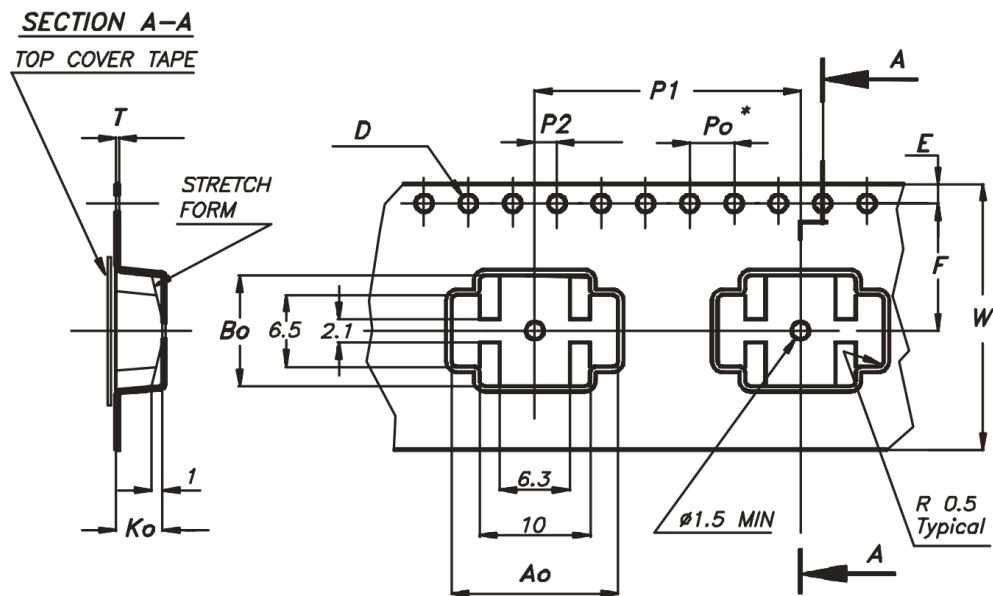
Table 8. PowerSO-10 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1	0	0.05	0.1
A2	3.4	3.5	3.6
A3	1.2	1.3	1.4
A4	0.15	0.2	0.25
a		0.2	
b	0.37	0.45	0.53
c	0.23	0.27	0.32
D	9.4	9.5	9.6
D1	7.4	7.5	7.6
d	0	0.05	0.1
E	13.85	14.1	14.35
E1 ⁽¹⁾	9.3	9.4	9.5
E2	7.3	7.4	7.5
E3	5.9	6.1	6.3
e		1.27	
e1		5.08	
F		0.5	
G		1.2	
L	0.8	1	1.1
R1			0.25
R2		0.8	
T	2 deg	5 deg	8 deg
T1		6 deg	
T2		10 deg	

1. Resin protrusions are not included (max. value 0.15 mm per side)

7.2 PowerSO-10 packing information

Figure 10. PowerSO-10 career tape outline



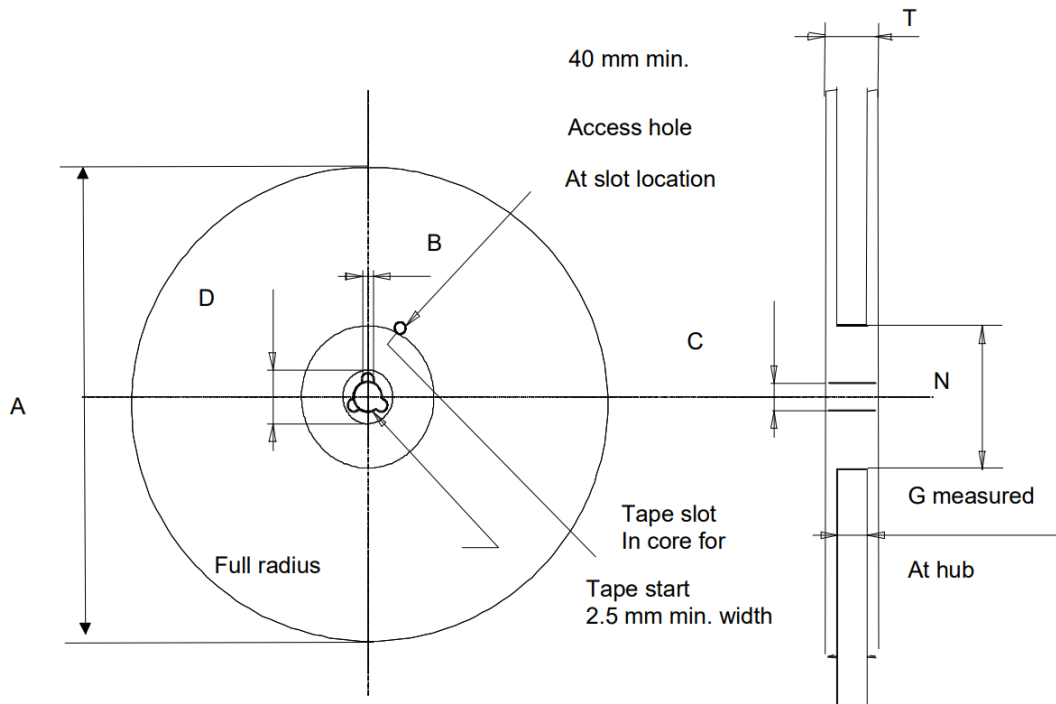
Note: Drawing is not in scale

Table 9. PowerSO-10 career tape dimension mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A0	14.9	15.0	15.1
B0	9.9	10.0	10.1
K0	4.15	4.25	4.35
F	11.4	11.5	11.6
E	1.65	1.75	1.85
W	23.7	24.0	24.3
P2	1.9	2.0	2.1
P0	3.9	4.0	4.1
P1	23.9	24.0	24.1
T	0.025	0.30	0.35
D(Ø)	1.50	1.55	1.60

Note: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm

Figure 11. PowerSO-10 reel outline



Note: Drawing is not in scale

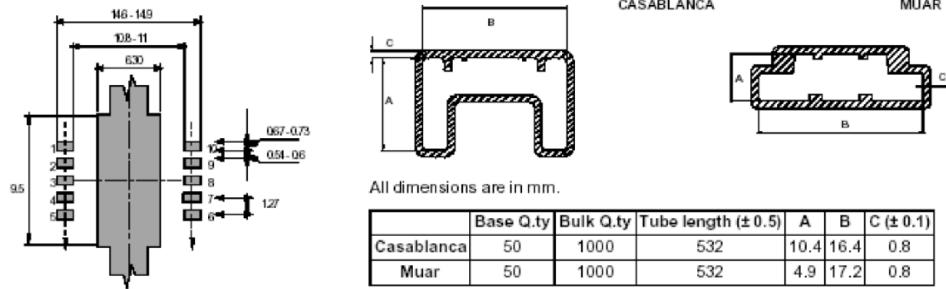
Table 10. PowerSO-10 reel dimension mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
B	1.5		
C	12.8	13	13.2
D	20.2		
N	60		
G	23.7	24.4	
T			30.4

Table 11. PowerSO-10 base and bulk quantity in tape and reel

Base quantity	Bulk quantity
600	600

Figure 12. PowerSO-10 suggested pad and tube shipment (no suffix)



Note: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm

8 Ordering information

Table 12. Ordering information

Part number	Package	Packaging
VN330SP-E	PowerSO-10	Tube
VN330SPTR-E		Tape and reel

Revision history

Table 13. Document revision history

Date	Revision	Changes
06-Sep-2005	1	Initial release.
31-Oct-2006	2	Typo in electrical characteristics temperature conditions updated on <i>page 5</i>
27-Mar-2007	3	Document reformatted, typo in <i>Note 1 on page 6</i>
14-Feb-2017	4	Updated Table 3. Power section . Inserted Figure 13. PowerSO-10 suggested pad and tube shipment (no suffix)
03-May-2022	5	Document reformatted; updated description and value of EAS in table 1 ; changed fig.4 ; some minor typo corrected

Contents

1	Block diagram	2
2	Pin connection	3
3	Maximum ratings	5
4	Electrical characteristics	6
5	Test circuits	8
6	Switching time waveforms and truth table	9
7	Package information	11
	7.1 PowerSO-10 package information	11
	7.2 PowerSO-10 packing information	13
8	Ordering information	16
	Revision history	17
	List of tables	19
	List of figures	20

List of tables

Table 1.	Absolute maximum ratings	5
Table 2.	Thermal data	5
Table 3.	Power section	6
Table 4.	Switching ($V_{CC} = 24\text{ V}$, $R_{LOAD} = 48\Omega$, see Figure 8. Switching parameter test conditions)	6
Table 5.	Logic inputs.	7
Table 6.	Protection and diagnostic	7
Table 7.	Truth table	9
Table 8.	PowerSO-10 package mechanical data	12
Table 9.	PowerSO-10 carrier tape dimension mechanical data	13
Table 10.	PowerSO-10 reel dimension mechanical data	14
Table 11.	PowerSO-10 base and bulk quantity in tape and reel	14
Table 12.	Ordering information.	16
Table 13.	Document revision history	17

List of figures

Figure 1.	Block diagram	2
Figure 2.	Connection diagram (top view)	3
Figure 3.	Current and voltage conventions	4
Figure 4.	Avalanche energy test circuit	8
Figure 5.	Peak short-circuit test diagram	8
Figure 6.	Switching waveforms.	9
Figure 7.	Switching parameter test conditions	10
Figure 8.	Driving circuit	10
Figure 9.	PowerSO-10 package outline	11
Figure 10.	PowerSO-10 carrier tape outline	13
Figure 11.	PowerSO-10 reel outline	14
Figure 12.	PowerSO-10 suggested pad and tube shipment (no suffix)	15

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved