12500 TI Boulevard, MS 8640, Dallas, Texas 75243

Notification# 20180221002
Datasheet for ADS131A02, ADS131A04
Change Notification

Date: February 23, 2018
To: PREMIER FARNELL PCN

Dear Customer:

This is a notice of change to a product data sheet for a device that is currently offered by Texas Instruments. The details of this change are on the following pages.

We request you acknowledge receipt of this notification within **30** days of the date of this notice.

The proposed first ship date is indicated on page 3 of this notification, unless customer agreement has been reached on an earlier implementation of the change.

This notice does not change the end-of-life status of any product. Should product affected be on a previously issued product withdrawal/discontinuance notice, this notification does not extend the life of that product or change the life time buy offering/discontinuance plan.

For questions regarding this notice, contact your local Field Sales Representative or the PCN Manager (PCN_ww_admin_team@list.ti.com).

Sincerely,

PCN Team
SC Business Services

20180221002
Data Sheet Change Notification
Attachments

Products Affected:

The devices listed on this page are a subset of the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

DEVICE	CUSTOMER PART NUMBER
ADS131A02IPBSR	null
ADS131A04IPBSR	null

Technical details of this Product Change follow on the next page(s).

PCN Number:	20180221002	**PCN Date:**	February 23, 2018
Title:	Datasheet for ADS131A02, ADS131A04		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	May 23, 2018		
Change Type:			

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized below.

TEXAS INSTRUMENTS

ADS131A02, ADS131A04

SBAS590D – MARCH 2016 – REVISED JANUARY 2018

Changes from Revision C (November 2016) to Revision D	Page
• Changed document title from *2- or 4-Channel, 24-Bit, Simultaneously-Sampling, Delta-Sigma ADC* to *2- or 4-Channel, 24-Bit, 128-kSPS, Simultaneous-Sampling, Delta-Sigma ADC*	1
• Changed V_{AVDD} to AVDD, V_{AVSS} to AVSS, V_{GND} to GND, and V_{IOVDD} to IOVDD throughout document	1
• Changed *Features* section	1
• Changed *Description* section	1
• Deleted footnote 2	6
• Changed AVDD, AVSS, VNCP, and XTAL2 pin descriptions and footnote 1 for clarity	6
• Changed *CAP to GND Power supply voltage* parameter specifications from *GND – 0.3 V* to *0.3 V* for the minimum specification and from *GND + 2.0 V* to *2.0 V* for the maximum specification	7
• Changed *Analog input voltage* parameter descriptions from *REFEXT to AVDD* to *REFEXT* and from *REFN input* to AVSS to *REFN*	7
• Changed *Digital input voltage* parameter description to include the names of the digital input pins	7
• Deleted CMRR footnote from *Recommended Operating Conditions* table	8
• Added symbol to *Reference input voltage* parameter	8
• Changed *Offset drift* parameter typical specification from 1.2 µV/°C to 2.5 µV/°C and maximum specification from 3 µV/°C to 4 µV/°C	9
• Changed *Gain drift* parameter typical specification from 0.25 ppm/°C to 0.5 ppm/°C	9
• Deleted separate AVDD PSRR specification for the ADS131A02	9

- Changed *Reference buffer offset* parameter typical specification from 170 µV to 250 µV 9
- Changed *Reference buffer offset drift* parameter typical specification from 1.1 µV/°C to 4 µV/°C and maximum specification from 4.3 µV/°C to 7 µV/°C 9
- Changed *Temperature drift parameter* typical specification from 4 ppm/°C to 6 ppm/°C 10
- Deleted *VNCP* parameter minimum specification and changed typical specification from –1.95 V to –2 V 10
- Changed *Electrical Characteristics* table so all *Power-Supply* subsections are condensed to one *Power-Supply* subsection 10
- Changed *free-air* to *ambient* in condition statements of *Timing Requirements* tables 12
- Changed location of several interface timing parameters to the *Timing Requirements* and *Switching Characteristics* tables from the *Detailed Description* section 12
- Changed unit from *ns* to t_{CLKIN} in $t_{c(SC)}$ and $t_{w(SCHL)}$ rows of *Timing Requirements: Synchronous Master Interface Mode* table 13
- Added $\overline{DRDY}$ *Synchronization Timing for Synchronous Slave Mode (CLKSRC = 0)* to $\overline{RESET}$ *Pin and Command Timing* figures 16
- Changed *Clock* section for clarification and changed setting of XTAL2 pin 26
- Changed *Clock Mode Configurations* figure to include load capacitors for clarity 27
- Changed *Analog Input* section for clarity 28
- Changed *Equivalent Analog Input Circuitry* figure 28
- Changed *Input Overrange and Underrange Detection* section for clarity 30
- Changed location of *Reference* section 30
- Changed *External Reference Driver* figure 31
- Changed *Internal Reference* figure 31
- Changed *Digital Decimation Filter* section for clarity 32
- Deleted figure and table from *Reset (*$\overline{RESET}$*)* section 35
- Changed *Fixed versus Dynamic-Frame Mode* section for clarity 36
- Added *Cyclic Redundancy Check (CRC)* section for clarity 39
- Changed *CRC with CRC_MODE = 0* and *CRC Using the WREGS Command* figures to using red shading instead of *//Zero* 39
- Changed *Data Ready (*$\overline{DRDY}$*)* section for clarity 43
- Changed *pulldown* to *pullup* in bulleted list of *ADC Frame Complete (*$\overline{DONE}$*)* section 47
- Changed description of *UNLOCK from POR or RESET* section 52
- Changed description of *RREG: Read a Single Register* section 52
- Changed *number of registers written plus one (n+1)* to *number of registers written minus one* in *WREGS: Write Multiple Registers* section 54
- Changed *User Register Description* section for clarity 56
- Changed *Unused Inputs and Outputs* section for clarity 67
- Changed title of *Multiple Device Configuration* section and changed description for clarity 68
- Changed first paragraph of *First Device Configured in Asynchronous Interrupt Mode* to condense data from last three paragraphs into one 68
- Changed description of *First Device Configured in Synchronous Master Mode* section to condense all paragraphs into one 70
- Changed description of *All Devices Configured in Synchronous Slave Mode* section to condense all paragraphs into one 72
- Changed *ADS131A0x Configuration Sequence* figure 79
- Changed *GND* to *AVSS* in VNCP pin description of *Negative Charge Pump* section 80
- Changed title of *Internal Digital LDO* section 80
- Changed description of *Power-Supply Sequencing* section 80
- Changed *Bipolar Analog Power Supply* to *Unipolar Analog Power Supply with Negative Charge Pump Enabled* figures 81
- Changed first sentence of *Layout Example* section 83
- Changed *ADS131A0x Layout Example* figure to improve layout 83

The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS131A02, ADS131A04	SBAS590C	SBAS590D

http://www.ti.com/product/ADS131A02
Reason for Change:
To accurately reflect device characteristics.
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):
Electrical specification performance changes as indicated above.
Changes to product identification resulting from this PCN:
None.
Product Affected:

ADS131A02IPBS	ADS131A02IPBSR	ADS131A04IPBS	ADS131A04IPBSR

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com