



# BUK7S1R2-40H

N-channel 40 V, 1.2 mΩ standard level MOSFET in LFPAK88

6 August 2020

Product data sheet

## 1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LFPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

## 2. Features and benefits

- Fully automotive qualified to beyond AEC-Q101:
  - -55 °C to +175 °C rating suitable for thermally demanding environments
- LFPAK88 package:
  - Designed for smaller footprint and improved power density over older wire bond packages such as D<sup>2</sup>PAK for today's space constrained high power automotive applications
  - Thin package and copper clip enables LFPAK88 to be highly efficient thermally
- LFPAK copper clip technology enabling improvements over wire bond packages by:
  - Increased maximum current capability and excellent current spreading
  - Improved  $R_{DSon}$
  - Low source inductance
  - Low thermal resistance  $R_{th}$
- LFPAK Gull Wing leads:
  - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
  - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
  - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
  - Reduced cell pitch and superjunction platform enables lower  $R_{DSon}$  in the same footprint
  - Improved SOA and avalanche capability compared to standard TrenchMOS
  - Tight  $V_{GS(th)}$  limits enable easy paralleling of MOSFETs

## 3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- LED lighting
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}; \text{Fig. 2}$	[1]	-	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$		-	-	294	W

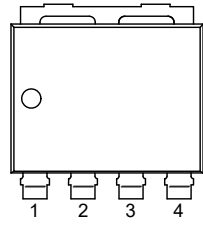
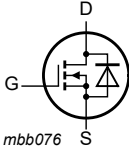
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	0.74	1.06	1.2	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	14	28	nC
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ [2]	-	38	-	nC
S	softness factor	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_j = 25\text{ °C}$	-	0.82	-	

[1] 300A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating emperature.

[2] includes capacitive recovery

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK7S1R2-40H	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7S1R2-40H	7S1R240H

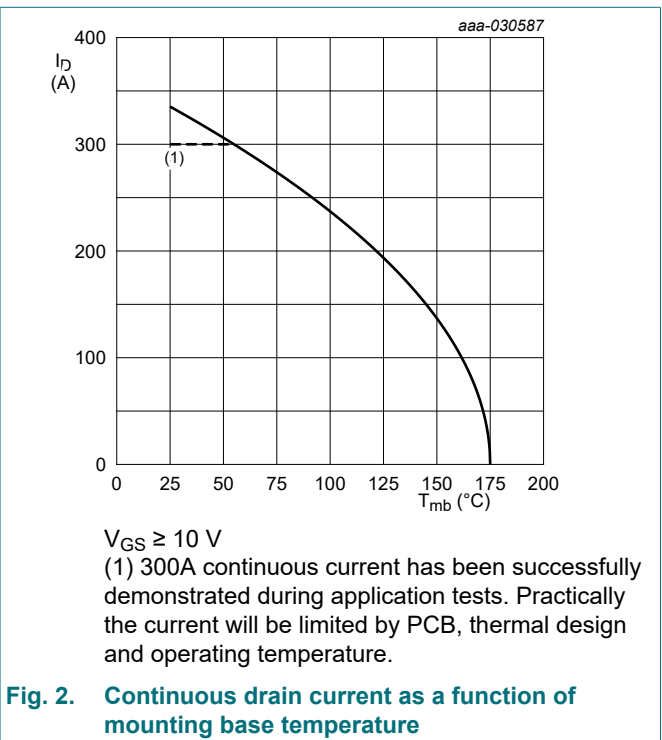
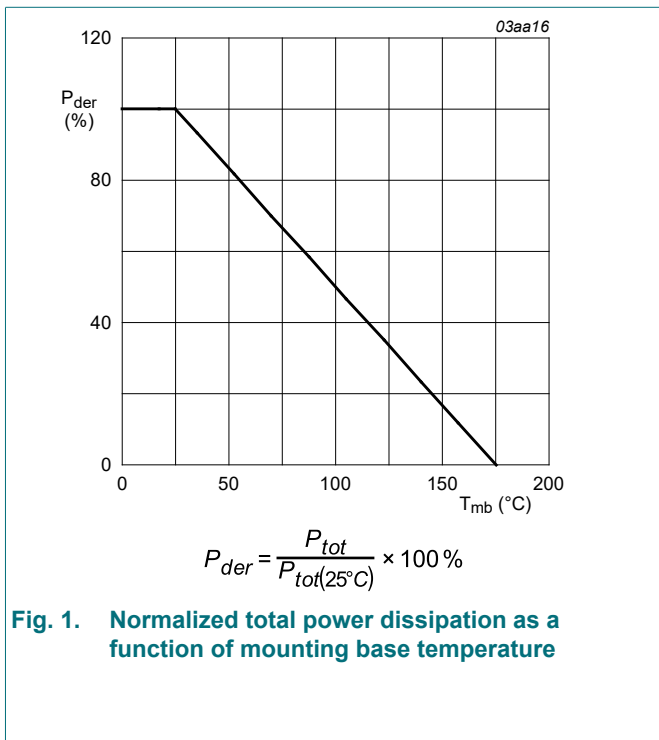
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	40	V
V <sub>GS</sub>	gate-source voltage	DC; T <sub>j</sub> ≤ 175 °C		-10	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	294	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>	[1]	-	300	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 3</a>		-	1341	A
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[2]	-	294	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	1341	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 120 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; <a href="#">Fig. 4</a>	[3] [4]	-	277	mJ
I <sub>AS</sub>	non-repetitive avalanche current	V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; R <sub>GS</sub> = 50 Ω; <a href="#">Fig. 4</a>	[5]	-	199	A

- [1] 300A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] 294A continuous current has been successfully demonstrated during application. Practically the current will be limited by PCB, thermal design and operating temperature.
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.
- [5] Protected by 100% test.



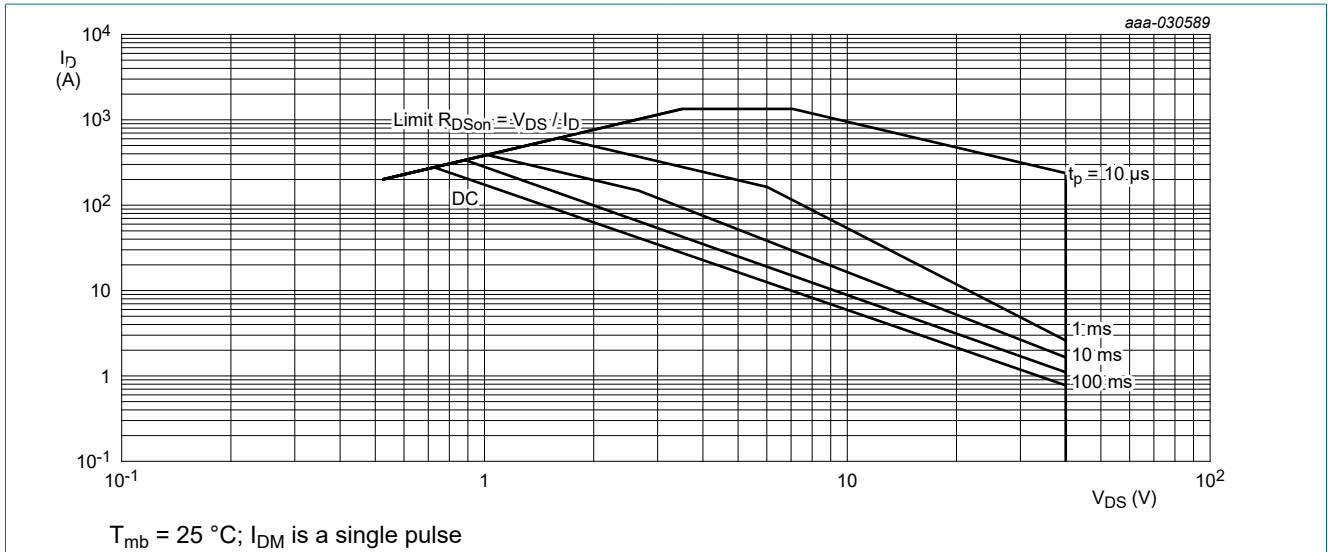


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

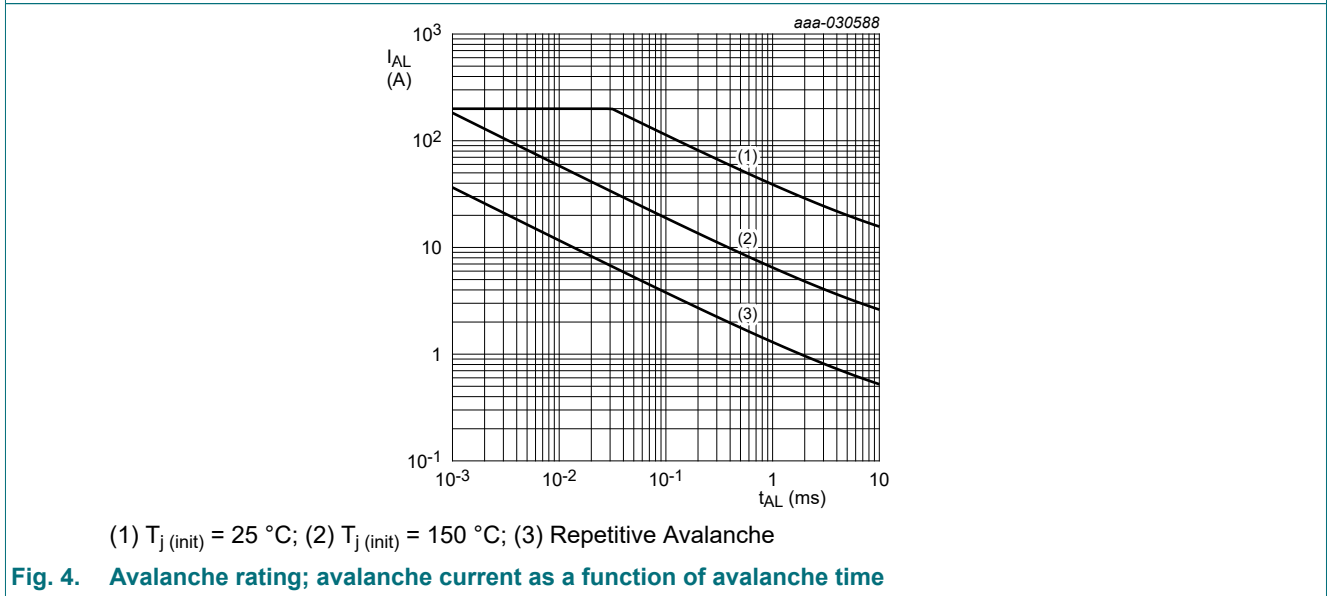


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.45	0.51	K/W

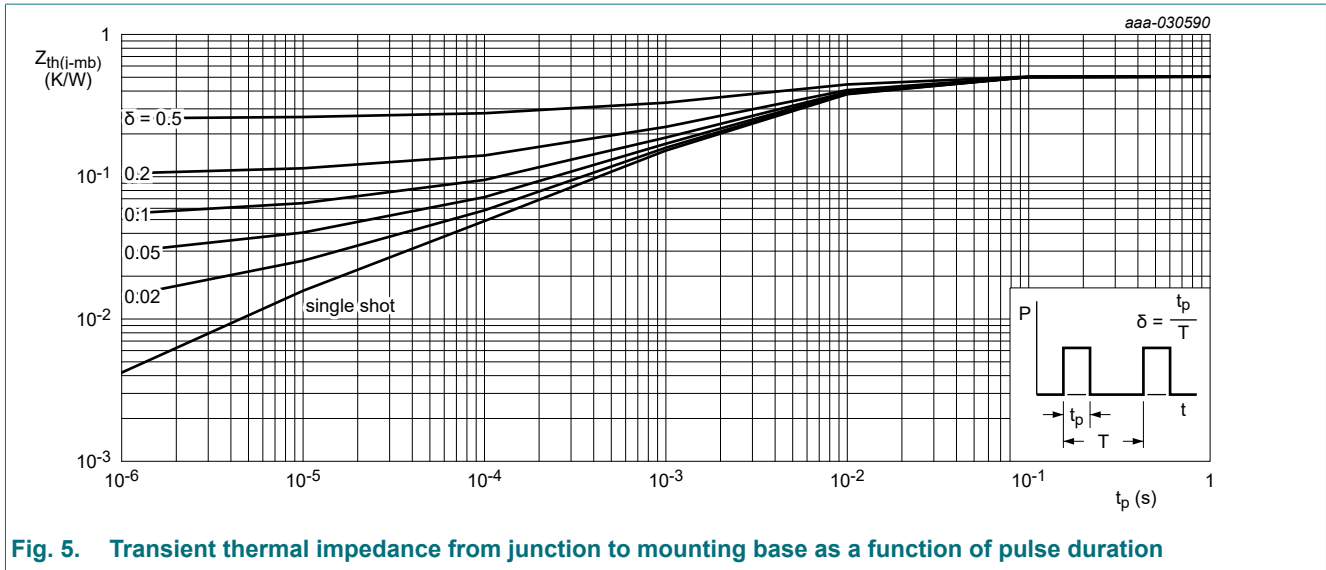


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

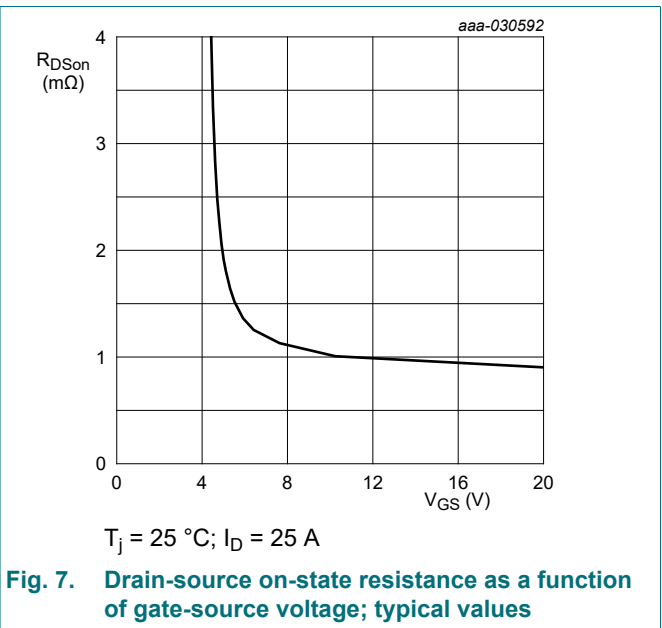
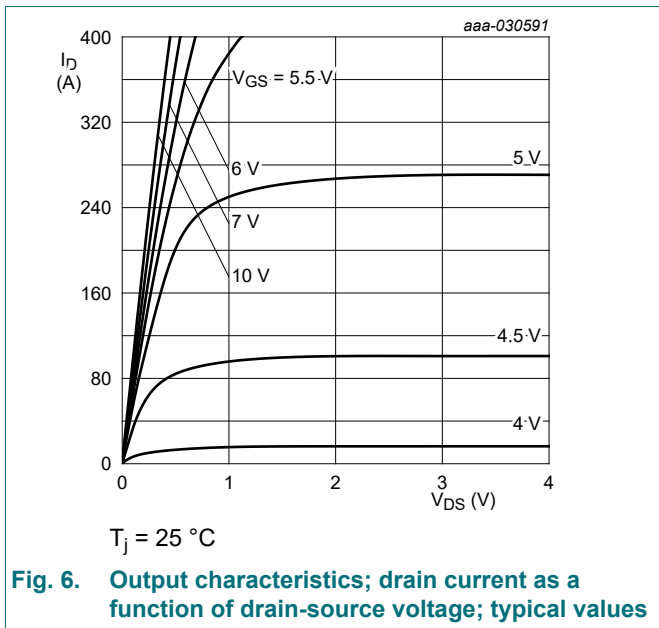
## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	2.4	3	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	4.3	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	1	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	1.2	$\mu A$
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.6	25	$\mu A$
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	180	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	0.74	1.06	1.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 105 \text{ }^\circ C; \text{ Fig. 12}$	1.05	1.59	1.9	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 125 \text{ }^\circ C; \text{ Fig. 12}$	1.16	1.76	2.1	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C; \text{ Fig. 12}$	1.46	2.21	2.6	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	0.4	1.05	2.6	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 32 \text{ V}; V_{GS} = 10 \text{ V}; \text{ Fig. 13}; \text{ Fig. 14}$	-	80	112	nC
$Q_{GS}$	gate-source charge		-	22	33	nC
$Q_{GD}$	gate-drain charge		-	14	28	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	6014	8420	pF
$C_{oss}$	output capacitance		-	1352	1893	pF
$C_{rss}$	reverse transfer capacitance		-	244	537	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ } \Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 5\text{ } \Omega$	-	19	-	ns
$t_r$	rise time		-	16	-	ns
$t_{d(off)}$	turn-off delay time		-	50	-	ns
$t_f$	fall time		-	22	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.77	1	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}$	-	39	-	ns
$Q_r$	recovered charge		[1]	38	-	nC
S	softness factor	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.82	-	
		$I_S = 25\text{ A}; di_S/dt = -500\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.73	-	

[1] includes capacitive recovery



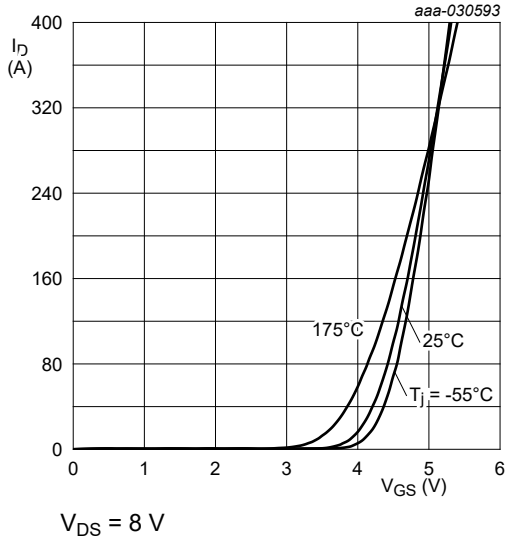


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

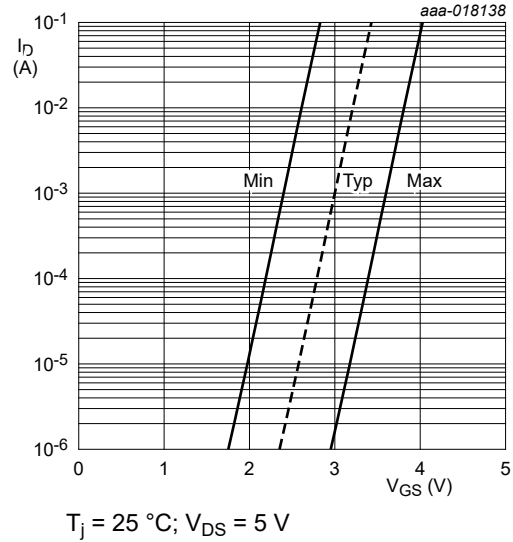


Fig. 9. Sub-threshold drain current as a function of gate-source voltage

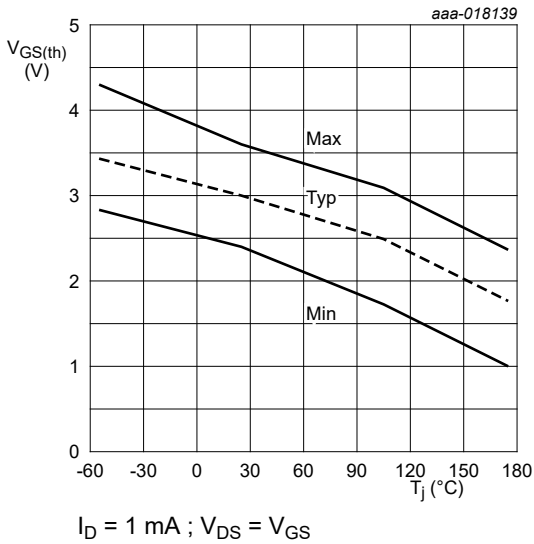


Fig. 10. Gate-source threshold voltage as a function of junction temperature

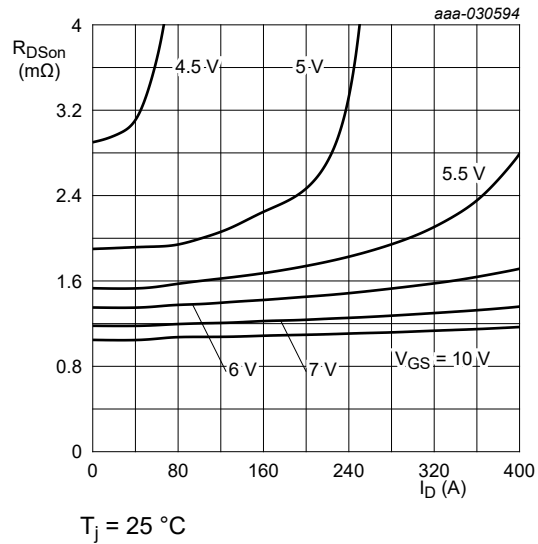
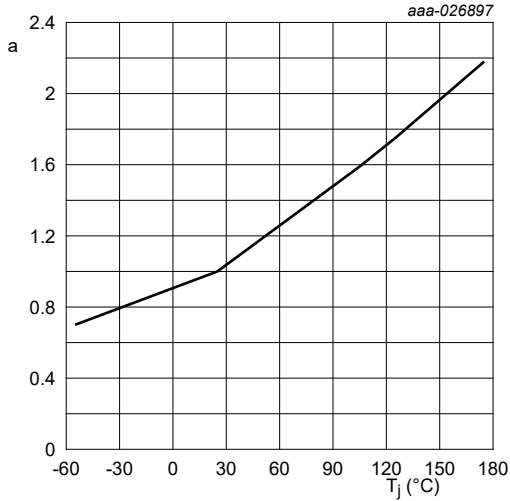
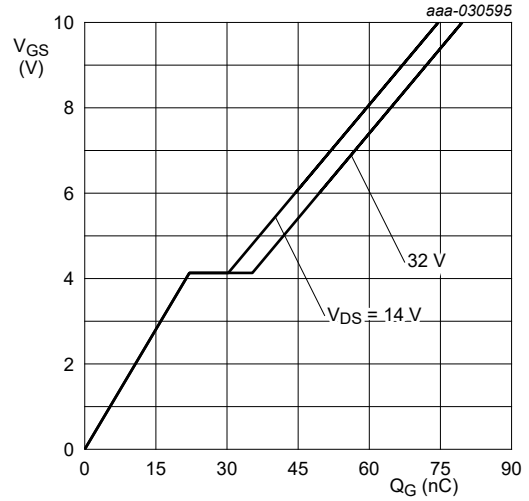


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$T_j = 25^{\circ}\text{C}; I_D = 25\text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

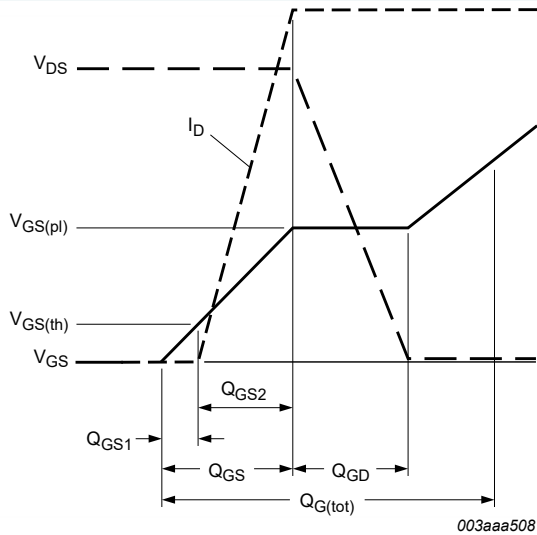
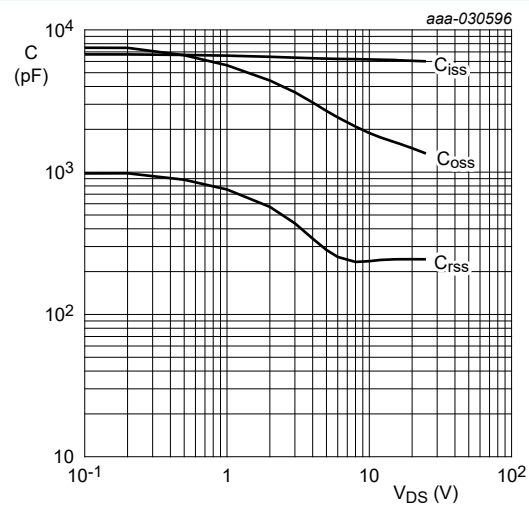


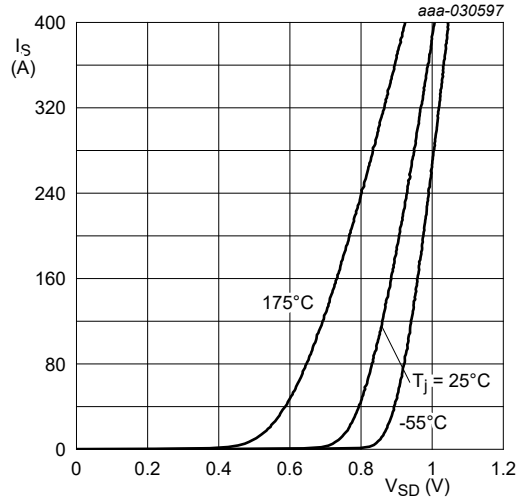
Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

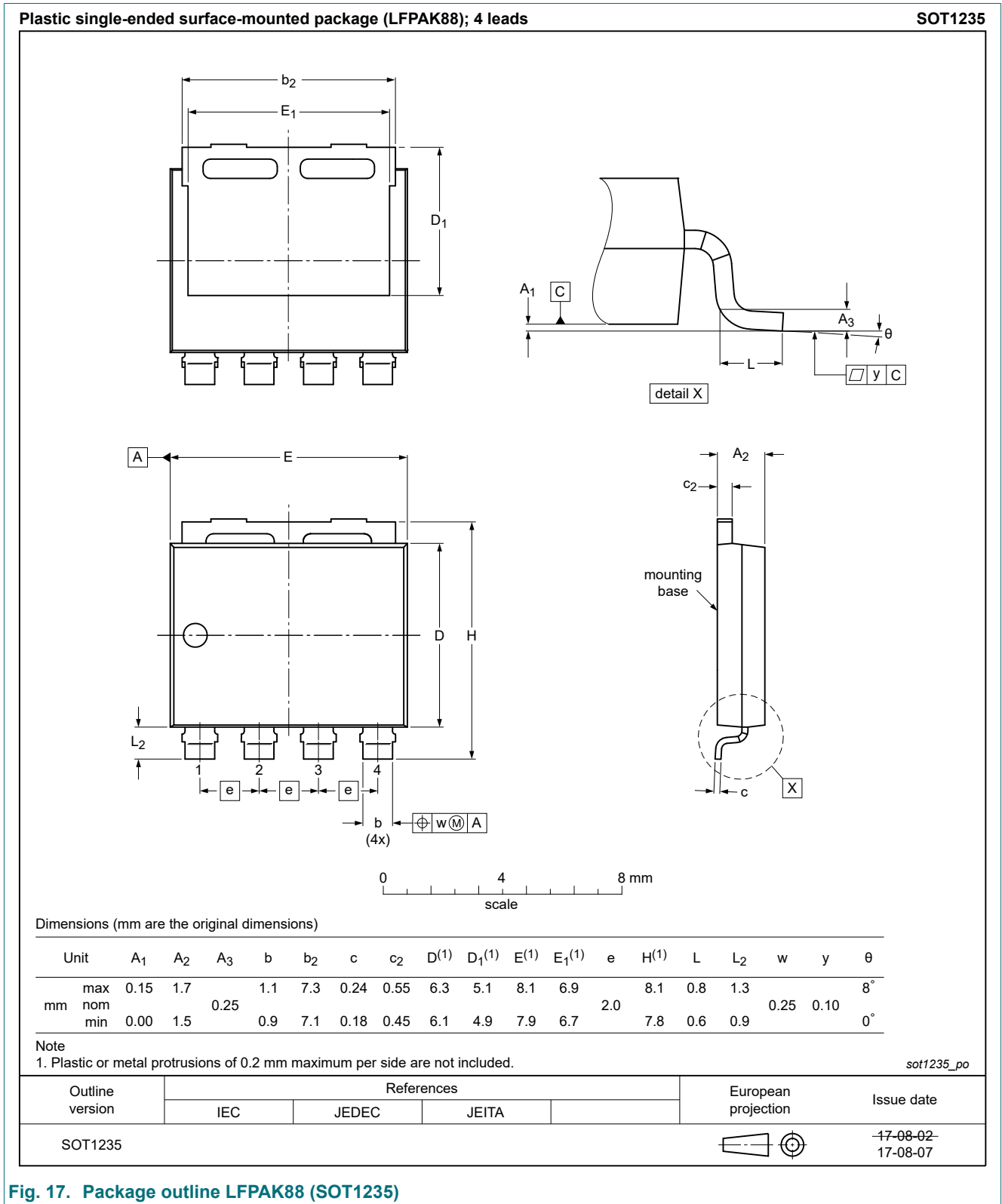




$V_{GS} = 0\text{ V}$

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

**11. Package outline**



**Fig. 17. Package outline LPAK88 (SOT1235)**

## 12. Soldering

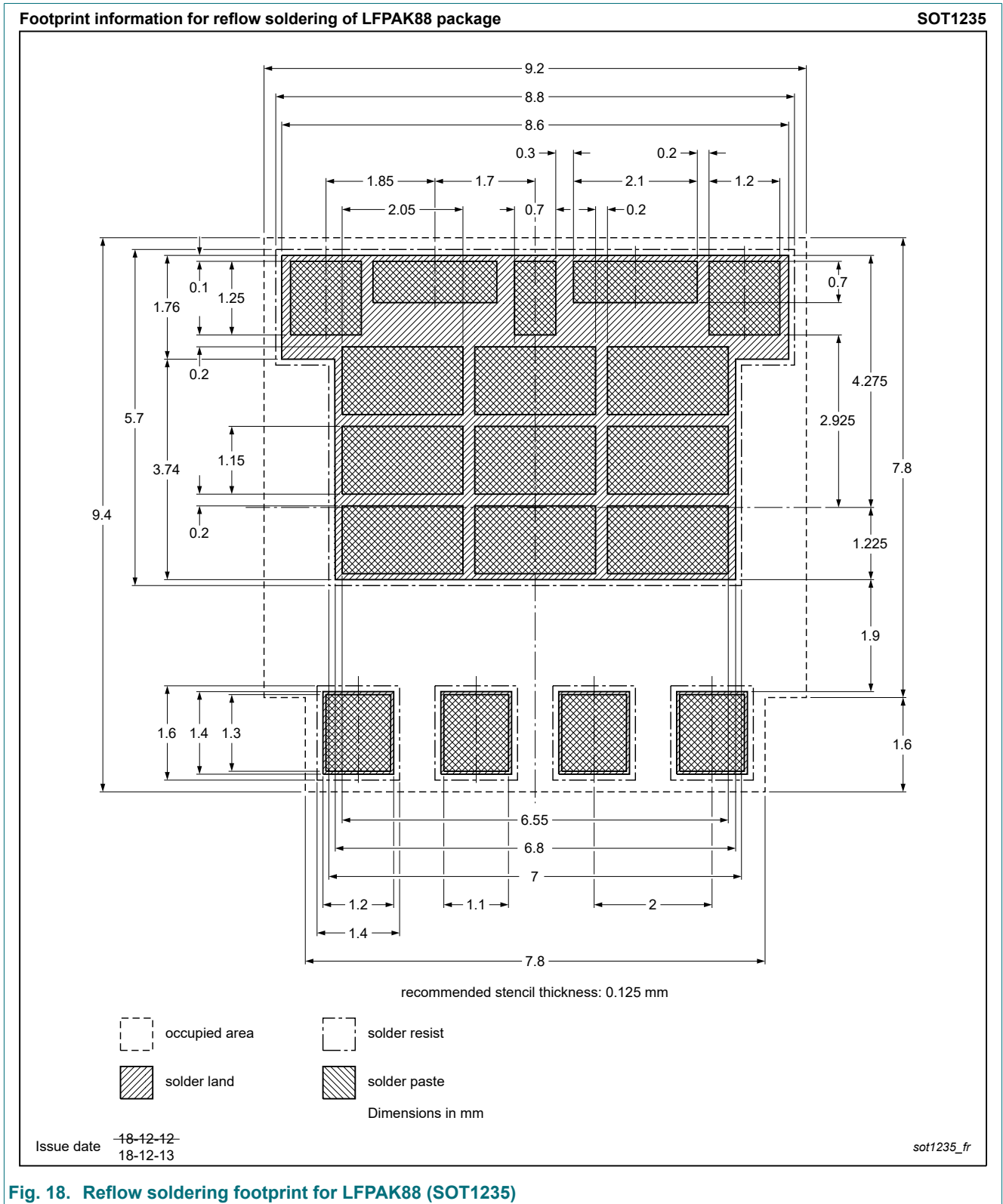


Fig. 18. Reflow soldering footprint for LPAK88 (SOT1235)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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