TAA630S

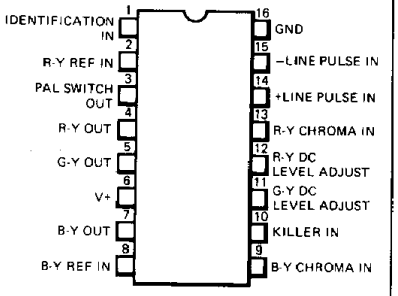
PAL CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TAA630S is a synchronous demodulator for direct drive of color video output stages. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The TAA630S is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. This circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator and a color killer switch.

- **DOUBLE BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

CONNECTION DIAGRAM
16-PIN DIP
(TOP VIEW)
PACKAGE OUTLINE 9B



ORDER INFORMATION

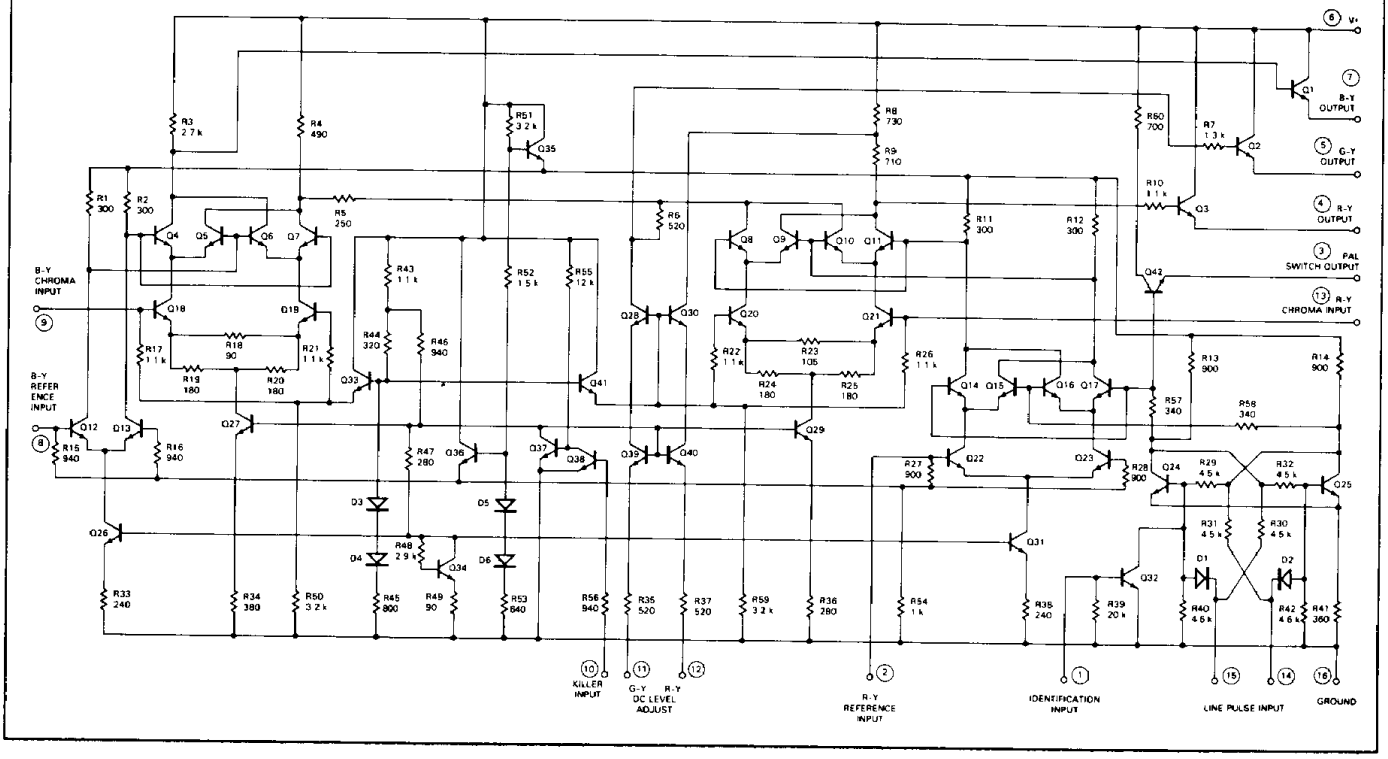
TYPE	PART NO.
630S	TAA630S
(630T)	(TAA630T)†

†Not recommended for new designs.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 1)	550 mW
Color Difference Output Currents	5.0 mA
Voltage on Identification Input	5.0 V
Current Into Identification Input	1.0 mA
Operating Temperature Range	−20°C to +60°C
Storage Temperature Range	−55°C to +125°C
Pin Temperature (Soldering, 10 s)	260°C

EQUIVALENT CIRCUIT



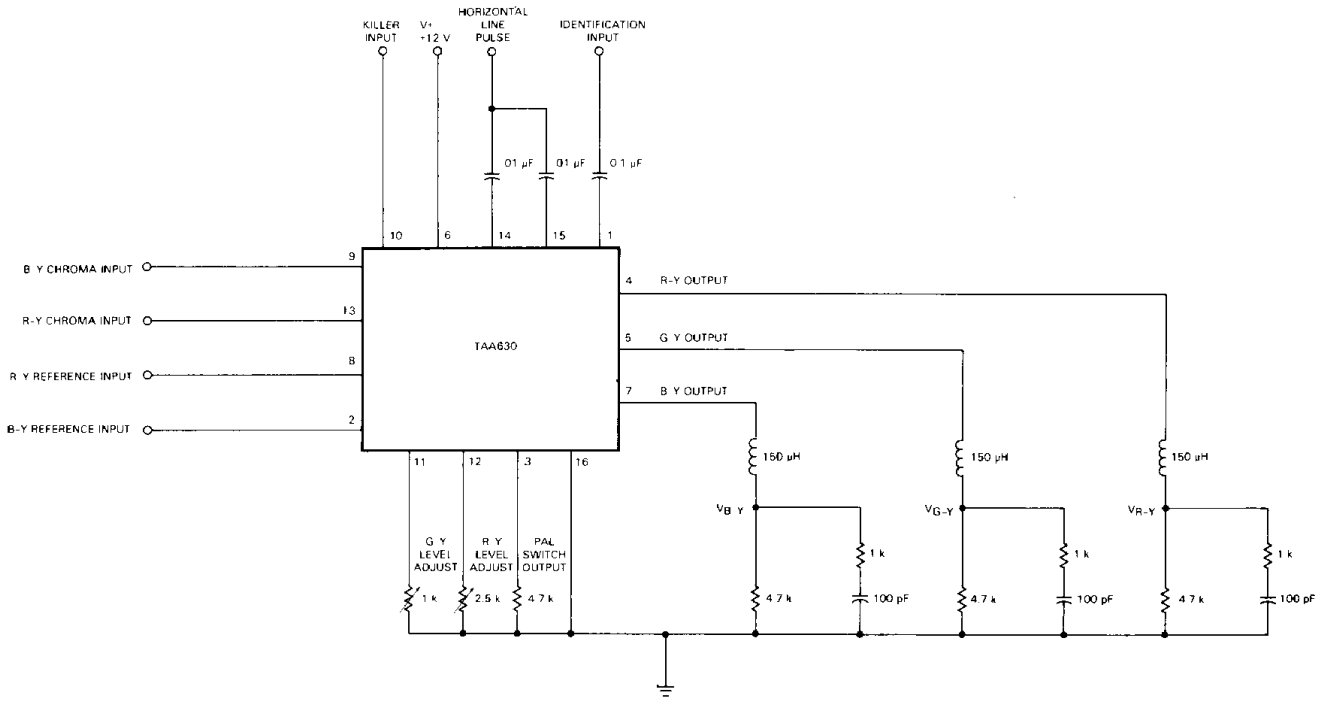
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS: T_A = 25°C, V_+ = 12V, See Test Circuit, unless otherwise specified.

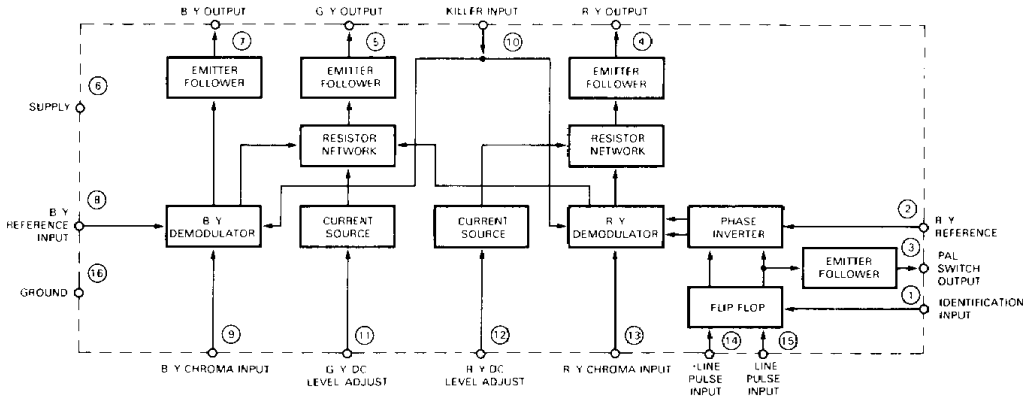
CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (I_6)			32		mA
Color Difference Gain	$V_9 = V_{13}$ = 50 mV p-p				
R-Y Channel	f = 4.4 MHz		7.0		
B-Y Channel/R-Y Channel			1.78		
G-Y Channel			Note 2		
Maximum Color Difference Output Voltage	Notes 3, 4				
R-Y Output (V_4 p-p)			3.2		Vp-p
B-Y Output (V_7 p-p)			4.0		Vp-p
G-Y Output (V_5 p-p)			1.8		Vp-p
Color Difference DC Output Voltage					
R-Y Output (V_4)	Note 5		Adjustable to V_7		
B-Y Output (V_7)			7.4		V
G-Y Output (V_5)	Note 5		Adjustable to V_7		
Input Resistance of Chroma Inputs (R_9, R_{13})	$V_9 = V_{13}$ = 20 mV_{RMS}	800			Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})	f = 4.4 MHz (sinusoidal)			10	pF
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Input Resistance of Reference Inputs (R_2, R_8)	Note 7	660		1250	Ω
Peak-to-Peak PAL Switch Output Voltage (V_3 p-p)	Note 6		2.5		Vp-p
Activation Threshold Voltage (V_1)	Identification circuit is active	0.75			V
Activation Threshold Current (I_1)		80			μA
Deactivation Threshold Voltage (V_1)	Identification circuit is inactive			0.4	V
DC Voltage at Color Killer Input (V_{10}):					
Color On		0.9			V
Color Off				0.3	V

NOTES:
1. 16 V is permissable during warm-up.
2. G-Y Output is typically equal to −0.51 (R-Y) −0.19 (B-Y).
3. Gain is equal to 0.7 of small signal gain.
4. Reference input (V_2 p-p and V_8 p-p) range is 0.5 V to 2.0 V.
5. To be adjusted with a variable voltage (V ≤ 1.2 V) or with resistors connected between pin 11 and ground for G-Y and pin 12 and ground for R-Y.
6. f_{out} = 0.5 x Line Pulse Frequency, $V_{14} = V_{15}$ = −2.5 V to −5.0 V (Peak), PAL identification signal required, V_1 = 2.0 to 6.0 V p/p.
7. $V_2 = V_8$ = 400 mV RMS, f = 4.4 MHz (sinusoidal).

TEST CIRCUIT



BLOCK DIAGRAM



TYPICAL APPLICATION