

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TENTATIVE

VIDEO-CHROMA-DEFLECTION SYSTEM FOR A COLOR TELEVISION (PAL, NTSC)

The TA7698AP combines a PAL/NTSC Video-Chroma subsystem and a Deflection combination on a single monolithic integrated circuit to provide a PAL or PAL/NTSC color television. This device includes a Video amplifier, PAL and NTSC color demodulator these are designed to provide color differential signal outputs, and improved Sync-separator, Horizontal oscillator with saw tooth wave type AFC, Horizontal pre-driver with X'ray protection circuit, Vertical oscillator and Vertical pre-driver in a 42 leads dual-in-line type plastic package.

FEATURES:

Video-Chroma Section

- . Simple PAL/NTSC System switch (Demodulator, Flip-flop, Tint control for NTSC)
- . Suitable to a Multi-CTV System :

TA7698AP ... PAL/NTSC Dual System

TA7698AP + SECAM combination ... 3 or more system

- . Minimum Numbers of External Parts Required.
- . Stabilized with Respect to Variation of Temperature and Supply Voltage.
- . A Few Initial Adjustment Required.

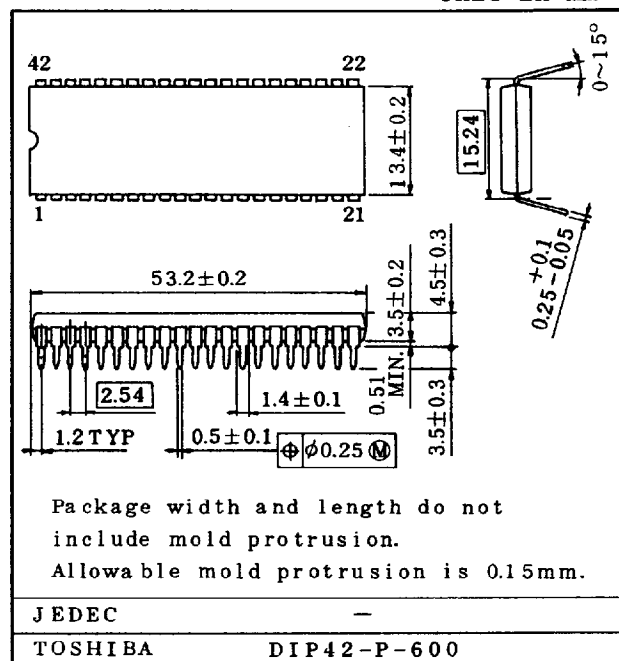
Deflection Section

- . Excellent Temperature Stability of Horizontal Oscillator.
- . Exact 50% Duty Cycle Output Due to the 2-f_H Oscillator and Flip-Flop Circuit.
- . Excellent Inter-race.

TA7698AP

TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

Unit in mm



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MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{CC} MAX	15	V
Horiz. Supply Current	I _{CC} MAX	40	mA
Max. Input Signal Level	e _{IN} 3,5,14,15,17, 19,28,37,39	5	V _{p-p}
Max. Control Terminal Voltage	V ₄ MAX, V ₅ MAX, V ₇ MAX, V ₉ MAX	V _{CC}	V
Term. 1 Max. Output Current	I ₁ MAX	4	mA
Term. 8 Max. Output Current	I ₈ MAX	10	mA
Term. 10 Max. Output Current	I ₁₀ MAX	4	mA
Term. 13 Max. Output Current	I ₁₃ MAX	4	mA
Min. Load Resistance	R _{LD}	1.8	kΩ
Term. 23 Max. Output Current	I ₂₃ MAX	4	mA
Vertical Stage Output Current	I ₂₄ MAX	20	mA
Term. 25 Max. Output Current	I ₂₅ MAX	4	mA
Term. 26 Max. Input Voltage	V ₂₆ MAX	V _{CC}	V
Term. 27 Max. Output Current	I ₂₇ MAX	20	mA
Term. 30 MAX. Input Current	-I ₃₀ MAX	1	mA
Horiz. Max. Sink Current	-I ₂₄ MAX	30	mA
Horiz. Ave. Sink Current	-I ₂₄	15	mA
Term. 35 Max. Input Voltage	V ₃₅ MAX	V _{CC}	V
Term. 36 Max. Voltage	V ₃₆ MAX	V _{CC}	V
Term. 38 Max. Input Voltage	V ₃₈ MAX	5	V
Term. 40 Max. Output Current	I ₄₀ MAX	5	mA
Term. 42 Max. Sink Current	-I ₄₂ MAX	4	mA
Max. Power Dissipation	P _D MAX	2.2	W
Operating Temperature	T _{opr}	-20~65	°C
Storage Temperature	T _{stg}	-55~150	°C

Note: Derated above Ta=25°C in the proportion of 17.6mW/°C.

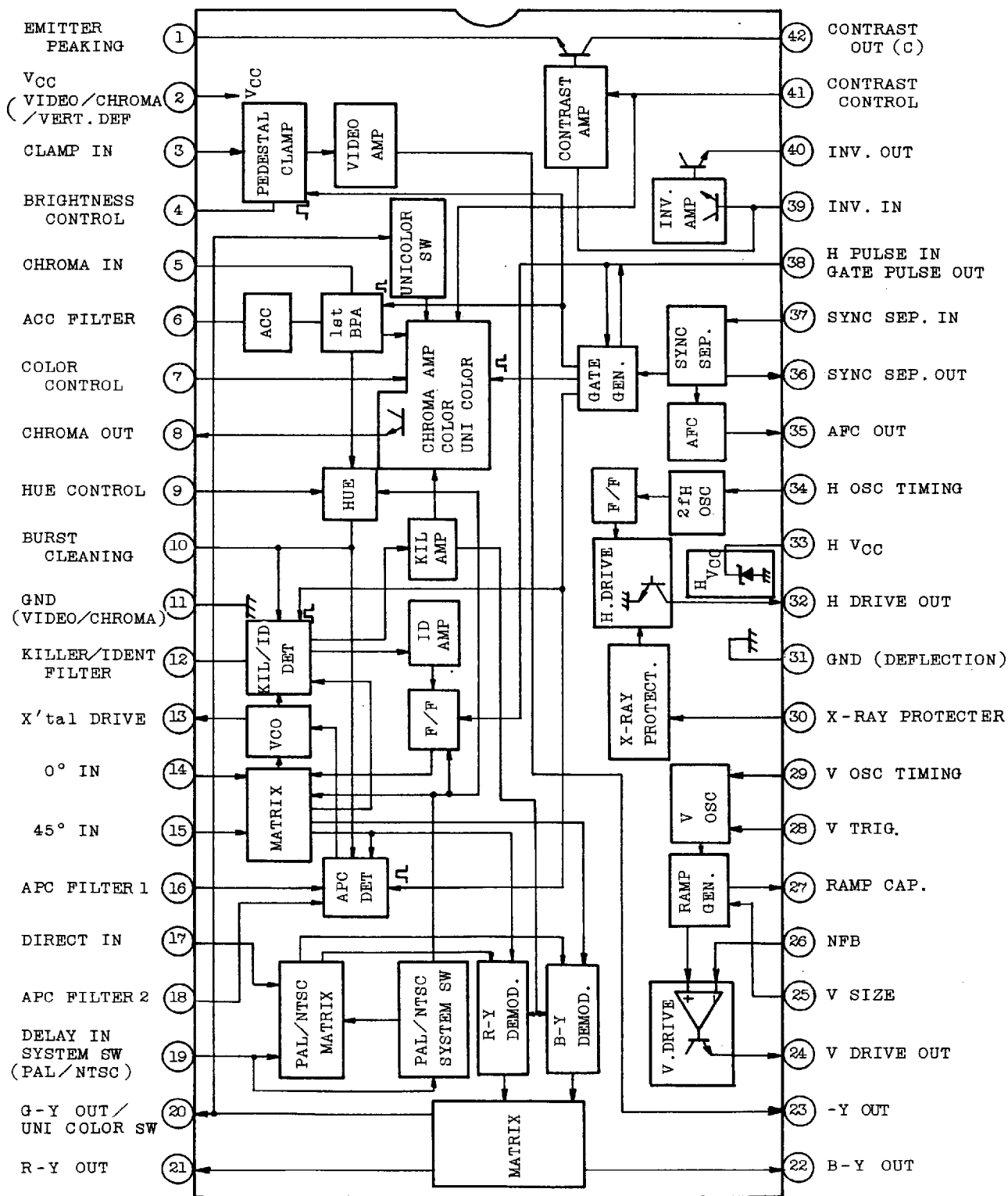
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BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $V_2=12V$, $T_a=25^\circ C$)
VIDEO SECTION (1)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 36	SW 41	SW 4A	SW 4B	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Recommendable Supply Voltage	V_{CC1}								10.8	12	13.2	V
12V Supply Current	I_{CC1}	1	2						60	82	106	mA
Video Gain	Gv	2	23 39	OFF	ON	OFF	ON	$V_C=10V$, $V_X=4.25V$, $V_Z=4.0V$ v_{39} :500kHz 1Vp-p(Multi Burst) $C_V=20\log(v_{23}/v_{39})$	3	6	7	dB
Contrast Gain Control Range	ΔG_V	2	23	OFF	ON	OFF	ON	$V_C=10V \sim 2V$, $V_X=4.25V$, $V_Z=4.0V$ v_{39} :500kHz 1Vp-p(Multi Burst) $\Delta G_V=20\log(v_{23}^{MAX.}/v_{23}^{MIN.})$	40	-	-	dB
Video Frequency Characteristics	ΔG_{VF}	2	23	OFF	ON	OFF	ON	$V_C=10V$, $V_X=4.25V$, $V_Z=4.0V$ v_{39} :500kHz, 4.0MHz 1Vp-p (Multi Burst) $\Delta G_{VF}=20\log(v_{23} \text{ 4MHz}/v_{23} \text{ 500kHz})$	-3.5	-1.5	0.5	dB
DC Restoration Ratio	K	2	23	OFF	ON	ON	ON	$V_C=10V$, $V_Z=4.0V$ V_X :Pedestal #39=3.25V v_{39} :2.5Vp-p 10 STEP APL 10%~90% $K = (1 - \frac{v_{23} \text{ pedestal}}{v_{23} \text{ 100\% APL}}) \times 100$	63	70	77	%
Max. Video Output	$v_{23} \text{ MAX}$	2	23	OFF	OFF	OFF	ON	$V_X=4.25V$, v_{39} :No Signal $V_Z=2V \sim 7V$ 10% to 90% of Variation	5.0	7.5	-	Vp-p
Video DC Output Term. Co-effici	$\partial V_{23}/\partial T$	2	23	OFF	OFF	OFF	ON	$V_X=4.25V$, $V_Z=4.0V$ v_{39} :No Signal $T_a=-20^\circ C \sim 65^\circ C$	-2.5	0	2.5	mV/ $^\circ C$

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VIDEO SECTION (2)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 36	SW 41	SW 4A	SW 4B	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Inverter Amp. Gain	GR	2	40	OFF	OFF	OFF	OFF	VX=4.25V v ₃₉ =500kHz, 1Vp-p GR=20log(v ₄₀ /v ₃₉)	2.2	3.5	4.6	dB
Inverter Amp. Differential	DGR	2	40	OFF	OFF	OFF	OFF	VX:3.3~5.3V v ₃₉ :3.58MHz, 100mVp-p DGR=(v _{40MAX} /v _{40MIN} -1) X 100	-	2.5	5	%
Inverter Amp. Differential Phase	DPR	2	40	OFF	OFF	OFF	OFF	VX:3.3~5.3V v ₃₉ :3.58MHz, 100mVp-p DPR=φ40MAX-φ40MIN	-	3	5	deg
Inverter Amp. Frequency Characteristics	4GRF	2	40	OFF	OFF	OFF	OFF	VX=4.25V v ₃₉ =500kHz, 4MHz, 1Vp-p 4GRF=20log(v ₄₀ 4MHz/v ₄₀ 500kHz)	-3.5	-0.1	0.5	dB
Inverter Amp. 3.58MHz Linearity	v _{L39}	2	39 40	OFF	OFF	OFF	OFF	VX=4.25V Measure #39 input level at #40 maximum output.	1.6	-	-	Vp-p
Contrast Control Open Voltage	V ₄₁	1	41	-	-	-	-		6.7	7.2	7.7	V
Color Control Open Voltage	V ₇	1	7	-	-	-	-		5.5	6.0	6.5	V
Tint Control Open Voltage	V ₉	1	9	-	-	-	-		5.5	6.0	6.5	V
Pedestal Amp. Gain	Gp		3 23	OFF	ON	OFF	ON	VX=4.25V, VZ=4V v ₃₉ =500kHz, 1Vp-p (Multi Burst) Gp=20log(v ₂₃ /v ₃)	9.5	12.0	13.5	dB

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CHROMA (1) PAL (Unless otherwise specified, $V_C=10V$, $V_S=10V$, SW36:ON, SW10:OFF, SW4A:ON, SW4B:ON)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Max. Chroma Output Voltage	eCmp	3	8	ON	ON	OFF	a	b	ON	$v_5:120mVp-p(B:C=1:1)$	0.5	0.75	1.05	Vp-p
Burst Output Voltage	ebp	3	10	ON	ON	OFF	a	b	ON	$v_5:120mVp-p(B:C=1:1)$	0.45	0.70	0.95	Vp-p
ACC Characteristics (1)	eap	3	8	ON	ON	OFF	a	b	ON	$v_5:15mVp-p(B:C=1:1)$	0.2	0.43	-	Vp-p
ACC Characteristics (2)	Ap	3	8	ON	ON	OFF	a	b	ON	$v_5:100mVp-p, 300mVp-p(B:C=1:1)$ $Ap = \frac{v_8(v_5=300mVp-p)}{v_8(v_5=100mVp-p)}$	-	1.0	1.3	-
Chroma Input Dynamic Range	eCip	3	8	ON	ON	OFF	a	b	ON	$v_5:100mVp-p \rightarrow 800mVp-p$	500	600	-	mVp-p
Uni Color Control Range (1) (Uni Color) (Switch ON)	$\Delta eCU1p$	3	8	ON	ON	OFF	a	b	ON	$V_C=4\sim 10V, V_S=10V$ $v_5:120mVp-p(B:C=1:1)$ $\Delta eCU1p = 20 \log \frac{v_8(v_C=10V)}{v_8(v_C=4V)}$	40	-	-	dB
Uni Color Control Range (2) (Switch OFF)	$\Delta eCU2p$	3	8	ON	ON	OFF	a	b	OFF	Same as above	-	0	-	dB
Uni Color Control Phase Shift	$\Delta \theta Up$	3	8	ON	ON	OFF	a	b	ON	$V_C=4V\sim 10V, V_S=10V$ $v_5:120mVp-p(B:C=1:1)$	-	-	5	deg
Residual Color	CKp	3	8	ON	ON	OFF	a	b	ON	$V_C=10V, V_S=0V$ $v_5:120mVp-p(B:C=1:1)$	-	-	3	mVp-p

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CHROMA (2) PAL

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Color Control Phase Shift	$\Delta\theta_{CCp}$	3	8	ON	ON	OFF	a	b	ON	VC=10V, VS=2~10V $v_5=120mVp-p$ (B:C=1:1)	-	3	-	deg
Burst-Chroma Phase Difference	$\Delta\theta_{bCp}$	3	8 10	ON	ON	OFF	a	b	ON	Burst phase difference between pin 8 and pin 10.	-	60	-	deg
Tint Control Range	$\Delta\theta_{bH1p}$	3	10	ON	ON	ON	a	b	ON		-	0	-	deg
Tint Control Phase Distribution	$\Delta\theta_{bH2p}$	3	10	ON	ON	ON	a	b	ON		-	0	-	deg
Killer Det. Sensitivity	e_{kp}	3	8 10	OFF	ON	OFF	a	a	ON	Change the burst level at pin 5 from 0 to 150mVp-p. Measure burst level at pin 10 when killer starts to operate.	30	60	110	mVp-p
Ident Det. Sensitivity	e_{lp}	3	21 10	OFF	ON	OFF	a	a	ON	Change burst level at pin 5 from 0 to 150mVp-p. Measure burst level at pin 10 when ident starts to operate.	-	60	-	mVp-p
APC Pull-in Range	f_{pp}	3	13	OFF	OFF	OFF	a	a	ON	$v_5:120mVp-p$ burst	± 300	± 500	-	Hz
Phase Det. Sensitivity	μp	3	16 18	OFF	OFF	OFF	a	c	ON	$v_5:120mVp-p$ burst	-	25	-	mV/deg
Control Sensitivity	βp	3	13 16 18	OFF	OFF	OFF	a	a	ON	$v_5:120mVp-p$ burst	-	2.2	-	Hz/mV

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CHROMA (3) PAL

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Color Differential Output Voltage	eORp	21	21	ON	ON	OFF	a	a	ON	v ₁₇ , v ₁₉ :100mVp-p 4.443618MHz CW:4.433618MHz	1.8	2.4	3.0	Vp-p
	eOG	3	20	ON	ON	OFF	a	a	ON		-	-	-	
	eOBp	22	22	ON	ON	OFF	a	a	ON		3.2	4.2	5.4	
Max. Color Differential Output Voltage	eORMp	21	21	ON	ON	OFF	a	a	ON	v ₁₇ , v ₁₉ :500mVp-p 4.43618MHz CW:4.433618MHz	3.8	5.5	-	Vp-p
	eOGMp	3	20	ON	ON	OFF	a	a	ON		-	-	-	
	eOBMp	22	22	ON	ON	OFF	a	a	ON		3.8	5.5	-	
Relative Amplitude	R-Y/B-Yp	21/	21/	ON	ON	OFF	a	a	ON	v ₁₇ :200mVp-p 4.443618MHz CW:4.433618MHz	0.46	0.56	0.66	-
	G-Y/B-Yp	22/	22/	ON	ON	OFF	a	a	ON		0.24	0.34	0.44	
Relative Phase	θ_{R-Yp}	3	21/	ON	ON	OFF	a	a	ON		220	90	100	deg
	θ_{G-Yp}	22	22/	ON	ON	OFF	a	a	ON		230	230	240	
Residual Carrier	ercRp	21	21	ON	ON	OFF	a	a	ON		-	-	300	mVp-p
	ercGp	3	20	ON	ON	OFF	a	a	ON		-	-	-	
	ercBp	22	22	ON	ON	OFF	a	a	ON		-	-	-	
Demodulator Bandwidth	fBRp	21	21	ON	ON	OFF	a	a	ON	v ₁₇ :200mVp-p 10kHz~5MHz	1.1	2.1	3.2	MHz
	fBGp	3	20	ON	ON	OFF	a	a	ON		-	-	-	
	fBBp	22	22	ON	ON	OFF	a	a	ON		-	-	-	
Demo. Output DC Voltage	EORp	21	21	OFF	OFF	OFF	a	b	ON		6.8	7.4	8.0	V
	EOGp	1	20	OFF	OFF	OFF	a	b	ON		-	-	-	
	EOBp	22	22	OFF	OFF	OFF	a	b	ON		-	-	-	
Demo. Output DC Voltage Difference	EO(R-G)p	21	21	OFF	OFF	OFF	a	b	ON	v ₁₇ , v ₁₉ no input	-0.2	0	0.2	V
	EO(R-B)p	1	20	OFF	OFF	OFF	a	b	ON		-	-	-	
	EO(B-G)p	22	22	OFF	OFF	OFF	a	b	ON		-	-	-	

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CHROMA (3) PAL

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	TEST CONDITION						MIN.	TYP.	MAX.	UNIT
				SW 41	SW 7	SW 9	SW 12	SW 15	SW 20				
Demo. Output DC Voltage Therm. Co-effic.	$\Delta EOR_{\theta P}$	21											
	$\Delta EOG_{\theta P}$	1	20	OFF	OFF	OFF	a	b	ON	-3	-0.5	2	mV/°C
	ΔEOB_{θ}		22										
Demo. Output Diffence Voltage Therm. Co-effic.	$EO(R-G)_{\theta P}$	21											
	$EO(R-B)_{\theta P}$	1	20	OFF	OFF	OFF	a	b	ON	-2	0	2	mV/°C
	$EO(B-G)_{\theta}$		22										
System SW Threshold	V_{ths}	3	19	OFF	OFF	OFF	a	b	ON	2.4	3	3.6	V
DC Change by System SW	ΔEOR	21											
	ΔEOG	3	20	OFF	OFF	OFF	a	b	ON	-100	0	100	mV
	ΔEOB		22										

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CHROMA (4) NTSC (Unless otherwise specified, $V_C=10V$, $V_S=10V$, SW36:ON, SW10:OFF, SW4A:ON, SW4B:ON)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Max. Chroma Output Voltage	e_{CMN}	4	8	ON	ON	OFF	a	b	ON	$v_5=120mVp-p (B:C=1:1)$	0.5	0.75	1.05	Vp-p
Burst Output Voltage	e_{bN}	4	10	ON	ON	OFF	a	b	ON	$v_5=120mVp-p (B:C=1:1)$	0.45	0.70	0.95	Vp-p
ACC Characteristics (1)	e_{aN}	4	8	ON	ON	OFF	a	b	ON	$v_5=15mVp-p (B:C=1:1)$	0.2	0.43	-	Vp-p
ACC Characteristics (2)	A_N	4	8	ON	ON	OFF	a	b	ON	$v_5=100mVp-p$, $300mVp-p (B:C=1:1)$ $A_P = \frac{v_8(v_5=300mVp-p)}{v_8(v_5=100mVp-p)}$	-	1.0	1.3	
Chroma Input Dynamic Range	e_{cIN}	4	8	ON	ON	OFF	a	b	ON	$v_5=100mVp-p \rightarrow 800mVp-p$	500	600	-	mVp-p
Uni Color Control Range (1) (Uni Color SW ON)	Δe_{CU1N}	4	8	ON	ON	OFF	a	b	ON	$V_C=4\sim 10V$, $V_S=10V$ $v_5=120mVp-p (B:C=1:1)$ $\Delta e_{CU1P} = 20 \log \frac{v_8(v_C=10V)}{v_8(v_C=4V)}$	40	-	-	dB
Uni Color Control Range (2) (SW OFF)	Δe_{CU2N}	4	8	ON	ON	OFF	a	b	OFF		-	0	-	dB
Uni Color Control Phase Shift	$\Delta \theta_{UN}$	4	8	ON	ON	OFF	a	b	ON	$V_C=4V\sim 10V$, $V_S=10V$ $v_5=120mVp-p (B:C=1:1)$	-	-	5	deg
Residual Color	e_{cKN}	4	8	ON	ON	OFF	a	b	ON	$V_C=10V$, $V_S=0V$ $v_5=120mVp-p (B:C=1:1)$	-	-	3	mVp-p

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CHROMA (5) NTSC

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Color Control Phase Shift	$\Delta\theta_{CCN}$	4	8	ON	ON	OFF	a	b	ON	$V_C=10V, V_S=2\sim10V$ $v_5=120mVp-p (B:C=1:1)$	-	3	7	deg
Burst-Chroma Phase Difference	$\Delta\theta_{bCN}$	4	8 10	ON	ON	OFF	a	b	ON		-	60	-	deg
Tint Control Range	$\Delta\theta_{bH1N}$	4	10	ON	ON	ON	a	b	ON	$V_C=10V$ $V_T=2\sim10V$ $v_5=120mVp-p (B:C=1:1)$	75	95	110	deg
										$f=4.43MHz$ $f=3.58MHz$	100	120	140	
Tint Control Phase Distribution	$\Delta\theta_{bH2N}$	4	10	ON	ON	ON	a	b	ON	$V_C=10V$ $v_5=120mVp-p (B:C=1:1)$ v_7	34	47	62	deg
										$f=4.43MHz$ $f=3.58MHz$	45	60	80	
Killer Det. Sensitivity	e_{KN}	4	8 10	OFF	ON	OFF	a	a	ON		15	30	75	mVp-p
APC Pull-in Range	f_{PN}	4	13	OFF	OFF	OFF	a	a	ON		± 300	± 500	-	Hz
Phase Det. Sensitivity	μ_N	4	16 18	OFF	OFF	OFF	a	c	ON		-	25	-	mV/deg
Control Sensitivity	β_N	4	13 16 18	OFF	OFF	OFF	a	a	ON		-	2.2	-	Hz/mV

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CHROMA (6) NTSC

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Color Differential Output Voltage	eORN	4	21	ON	ON	OFF	a	a	ON	v_{17} : 100mVp-p 4.443618MHz CW: 4.433618MHz	3.0	4.1	5.3	Vp-p
	eOGN		20	ON	ON	OFF	a	a	ON		1.0	1.6	2.2	
	eOBN		22	ON	ON	OFF	a	a	ON		3.0	4.1	5.3	
Max. Color Differential Output Voltage	eORMN	4	21	ON	ON	OFF	a	a	ON	v_{17} : 500mVp-p 4.443618MHz CW: 4.433618MHz	4.5	5.5	-	Vp-p
	eOGMN		20	ON	ON	OFF	a	a	ON		1.4	1.8	-	
	eOBMN		22	ON	ON	OFF	a	a	ON		4.5	5.5	-	
Relative Amplitude	R-Y/B-YN	4	21/	ON	ON	OFF	a	a	ON	v_{17} : 100mVp-p 4.443618MHz CW: 4.433618MHz	0.88	1.00	1.1	-
	G-Y/B-YN		22/	ON	ON	OFF	a	a	ON		0.28	0.38	0.48	
			22/	ON	ON	OFF	a	a	ON					
Relative Phase	θ R-YN	4	21/	ON	ON	OFF	a	a	ON		-	105	-	deg
	θ G-YN		22/	ON	ON	OFF	a	a	ON		-	235	-	
			22/	ON	ON	OFF	a	a	ON					
Residual Carrier	ercRN	4	21	ON	ON	OFF	a	a	ON		-	-	300	mVp-p
	ercGN		20	ON	ON	OFF	a	a	ON					
	ercBN		22	ON	ON	OFF	a	a	ON					
Demodulator Band Width	fBRN	4	21	ON	ON	OFF	a	a	ON	v_{17} : 100mVp-p, 10kHz~5MHz	1.1	2.1	3.2	MHz
	fBGN		20	ON	ON	OFF	a	a	ON					
	fBBN		22	ON	ON	OFF	a	a	ON					
Demo. Output DC Voltage	EORN	1	21	OFF	OFF	OFF	a	b	ON	v_{17} :	6.8	7.4	8.0	V
	EOGN		20	OFF	OFF	OFF	a	b	ON					
	EoBN		22	OFF	OFF	OFF	a	b	ON					
Demo. Output DC Voltage Difference	EO(R-G)N	1	21	OFF	OFF	OFF	a	b	ON	v_{17} :	-0.3	0	0.3	V
	EO(G-B)N		20	OFF	OFF	OFF	a	b	ON					
	EO(B-G)N		22	OFF	OFF	OFF	a	b	ON					

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TOSHIBA CORPORATION

9097247 0019737 180

CHROMA (6) NTSC

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 41	SW 7	SW 9	SW 12	SW 15	SW 20	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Demo. Output DC Voltage Therm. Co-effic.	$\Delta EOR\theta_N$	1	21							Ta=-20~65°C	-3	0	2	mV/°C
	$\Delta EOG\theta_N$		20	OFF	OFF	OFF	a	b	ON					
	$\Delta EOB\theta_N$		22											
Demo. Output Diff. Voltage Therm. Co-effic.	$\Delta EO(R-G)\theta_N$	1	21							Ta=-20~65°C	-2	0	2	mV/°C
	$\Delta EO(R-B)\theta_N$		20	OFF	OFF	OFF	a	b	ON					
	$\Delta EO(B-G)\theta_N$		22											

TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

TA7698AP

HORIZONTAL SECTION (1) (SW24, SW27, SW28 : OFF, SW29:a)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 34	SW 35	SW 36	SW 37	SW 32	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Horizontal Regulated Voltage	V33	1	33	-	-	-	-	-		7.4	8.2	9.0	V
Recommendable Supply Current	I33	5	33							22	26	30	mA
Horizontal Free Running Frequency	f _H	5	34	OFF	OFF	OFF	b	a	V _H =4V	14.725	15.625	16.125	kHz
f _H Thermal Drift	4f _{HT}	5	34	OFF	OFF	OFF	b	a	V _H =4V Ta=-20~60°C	-90	70	230	Hz
AFC Clamping Voltage	V _{CL}	1	35	-	-	-	-	a	SW1:a, SW2:a	3.9	4.5	5.1	V
AFC Sink Current	I _{IN35}	1	35	-	-	-	-	a	SW1:a, SW2:b	2.7	3.7	5.0	mA
AFC Source Current	I _{O35}	1	35	-	-	-	-	a	SW1:a, SW2:c	2.7	4.0	5.0	mA
Horiz. Drive Residual Voltage	V _{OL32}	5	32	OFF	OFF	OFF	b	a	V _H =4V Saturation Voltage of #32	-	-	0.3	V
Horiz. Output Pulse Duty	T _{O32}	5	32	OFF	OFF	OFF	b	a	V _H =4V T _{O32} =Duty cycle of H period.	45	50	55	%
Horiz. Osc. Starting Voltage	V33 START	5	33	OFF	OFF	OFF	b	a	V _B :Variable Measure min V _B which provides 150% duty output to #32	-	-	4.0	V

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TOSHIBA CORPORATION

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TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

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HORIZONTAL SECTION (2)

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 34	SW 35	SW 36	SW 37	SW 32	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
4V Supply Current	I ₃₃ START	5	33	OFF	OFF	OFF		a	V _B =4V Measure I ₃₃	4.6	6.7	8.8	mA
AFC Pull-in Range	Δf_H PULL	5	32 37	ON	ON	OFF		a b	V _H :Variable Observe #32 and #37 waveform. S37 a→b, Measure the frequency difference.	-	±900	-	Hz
AFC Hold Range	Δf_H HOLD	5	32 37	ON	ON	OFF		a b	Same as above	-	±1800	-	Hz
AFC Voltage Sensitivity	β_H	5	32	OFF	OFF	OFF		a	V _A =4.5V, Set V _H so that f _H will be 15.75kHz. Then, change V _A 4V±0.5V, Measure f _H difference.	-	1900	-	Hz/V
X'ray Protector Voltage Sensitivity	V _{IN30}	5	30	OFF	OFF	OFF		a	Apply variable DC voltage to #30(V ₃₀). Measure V ₃₀ and I ₃₀ when #32 output disappears.	0.75	0.93	1.1	V
X'ray Protector Current Sensitivity	I _{IN30}	5	30	OFF	OFF	OFF		a		0.05	0.18	1.0	μA
H. Drive Output Excess Voltage Protector Current Sens.	I _{IN32}	5	32	OFF	OFF	OFF		b	Apply variable DC voltage to #32 through 1kΩ resistor. Measure V ₃₂ and I ₃₂ just before V ₃₂ goes down.	0.05	0.18	1.0	μA
Excess Voltage Protector Voltage Sens.	V _{IN32}	5	32	OFF	OFF	OFF		b		7.1	8.6	9.5	V

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TOSHIBA CORPORATION

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TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

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VERTICAL SECTION

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 24	SW 26	SW 28	SW 29	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vertical Frequency	f _v	5	27	OFF	OFF	OFF	c		47	50	54.1	Hz
Retrace Time	Tr	5	27	OFF	OFF	OFF	c	H period of #27 output pulse	450	690	850	μsec
f _v Pull-in Range	Δf _v PULL	5	27	OFF	OFF	ON , OFF	b	Set f _v to 50Hz at SW28:OFF ;fOSC28 Measure f _v at SW28:ON ;fOSC'28 Δf _v PULL=fOSC28-fOSC'28	9.0	10.0	11.0	Hz
Term. 27 Max. Output Voltage	V _{O27}	1	27	-	-	-	-	SW29:ON, SW4:OFF	7.7	8.5	9.2	V
Term. 27 Max. Output Current	I _{O27}	1	27	-	-	-	-	SW29:ON, SW4:ON	15	27	50	mA
Max. Common Mode Input Voltage	V _{IH26}	5	26	ON	ON	OFF	a	V ₂₇ =6→12V	11.9	-	-	V
Min. Common Mode Input Voltage	V _{IL26}	5	26	ON	ON	OFF	a	V ₂₇ =6→0V	-	2.8	3.7	V

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TOSHIBA CORPORATION

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TOSHIBA

INTEGRATED CIRCUIT

TECHNICAL DATA

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VERTICAL SECTION

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 24	SW 26	SW 28	SW 29	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Term. 27 Input Current	II27	5	27	ON	ON	OFF	a	V27=6V	0.25	1.0	4.5	μA
Term. 26 Input Current	II26	5	26	ON	ON	OFF	a	V27=6V	0.18	1.0	6.3	μA
Max. Drive Output Voltage	VOH24	5	24	OFF	ON	OFF	d		7.3	8.0	8.7	V
Min. Drive Output Voltage	VOL24	5	24	OFF	OFF	OFF	d		-	-	0.3	V
Term. 25 Bias Voltage	V25	5	25					I25=-0.2mA	3.7	3.9	4.1	V
fV Thermal Drift	ΔfVT	5	27	OFF	OFF	OFF	c	Ta=-20-60°C	-1.0	0	2.0	Hz

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TOSHIBA CORPORATION

TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

TA7698AP

SYNC SEPARATOR

CHARACTERISTIC	SYMBOL	TEST CCT	TEST PIN	SW 34	SW 35	SW 36	SW 37	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Sync. Separator Current Sensitivity	IIN37	5	36 37	OFF	OFF	OFF	c	Measure #37 input current when V36 goes L level to H.	18	35	113	μA
Sync. Output H level	VOH36	5	36	OFF	OFF	OFF	c	V _S =2V Measure V36	7.0	8.2	9.4	V
Sync. Output L level	VOL36	5	36	OFF	OFF	OFF	b	Measure V36	0	0.2	1.0	V
Gate Pulse H level	VOH38	5	38	OFF	OFF	OFF	b	V _D =12V, V36=5V Measure V38	4.3	5.3	6.1	V
Gate Pulse L level	VOL38	5	38	OFF	OFF	OFF	b	V _D =12V Measure V38	-	1.6	-	V
H Pulse Threshold	V38ON	5	38	OFF	OFF	OFF	b	V _D :Variable 0~2V Measure V _D when V38 goes H to L.	0.7	1	1.5	V

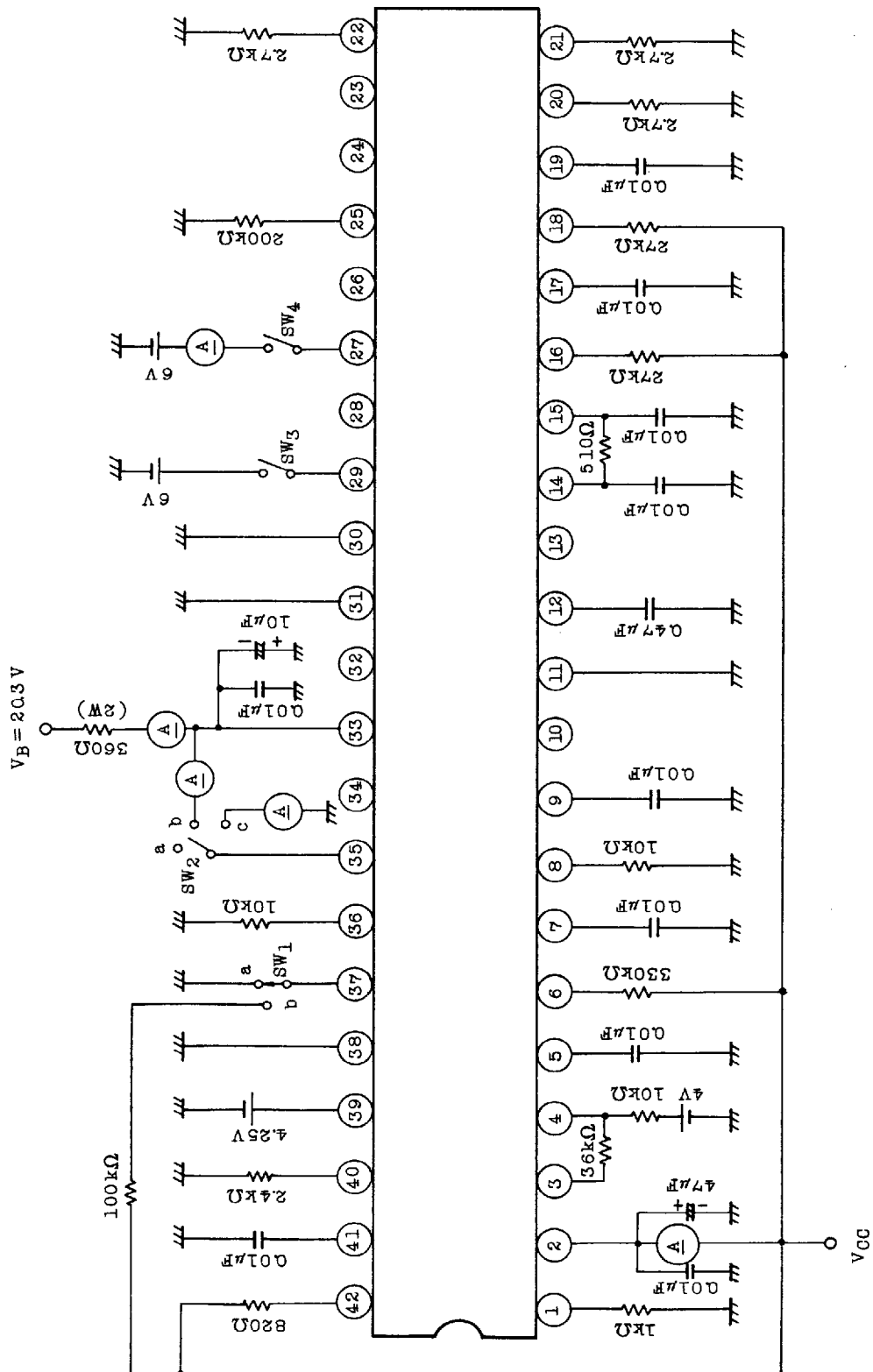
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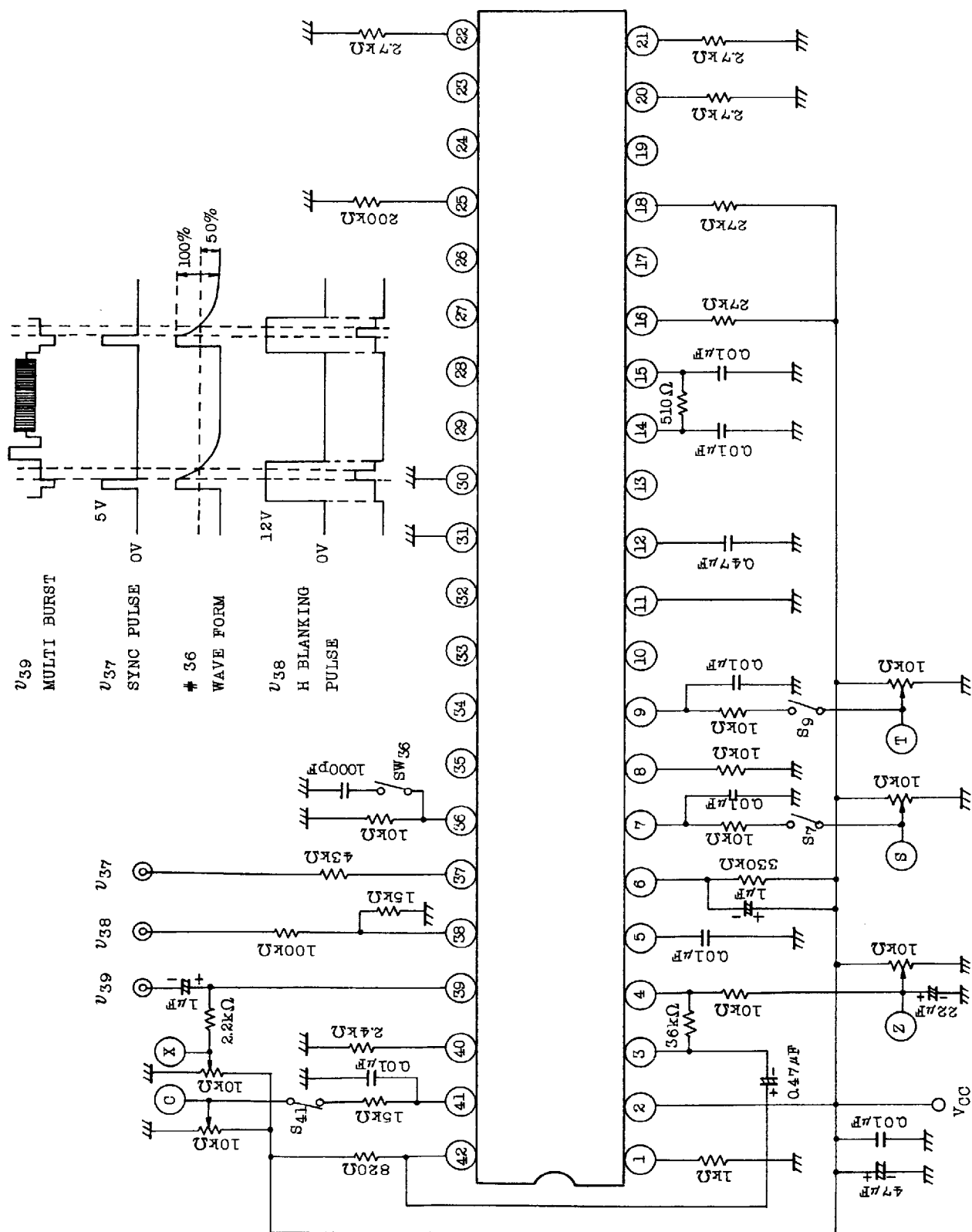
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TEST CIRCUIT 1. DC



TEST CIRCUIT 2. Video



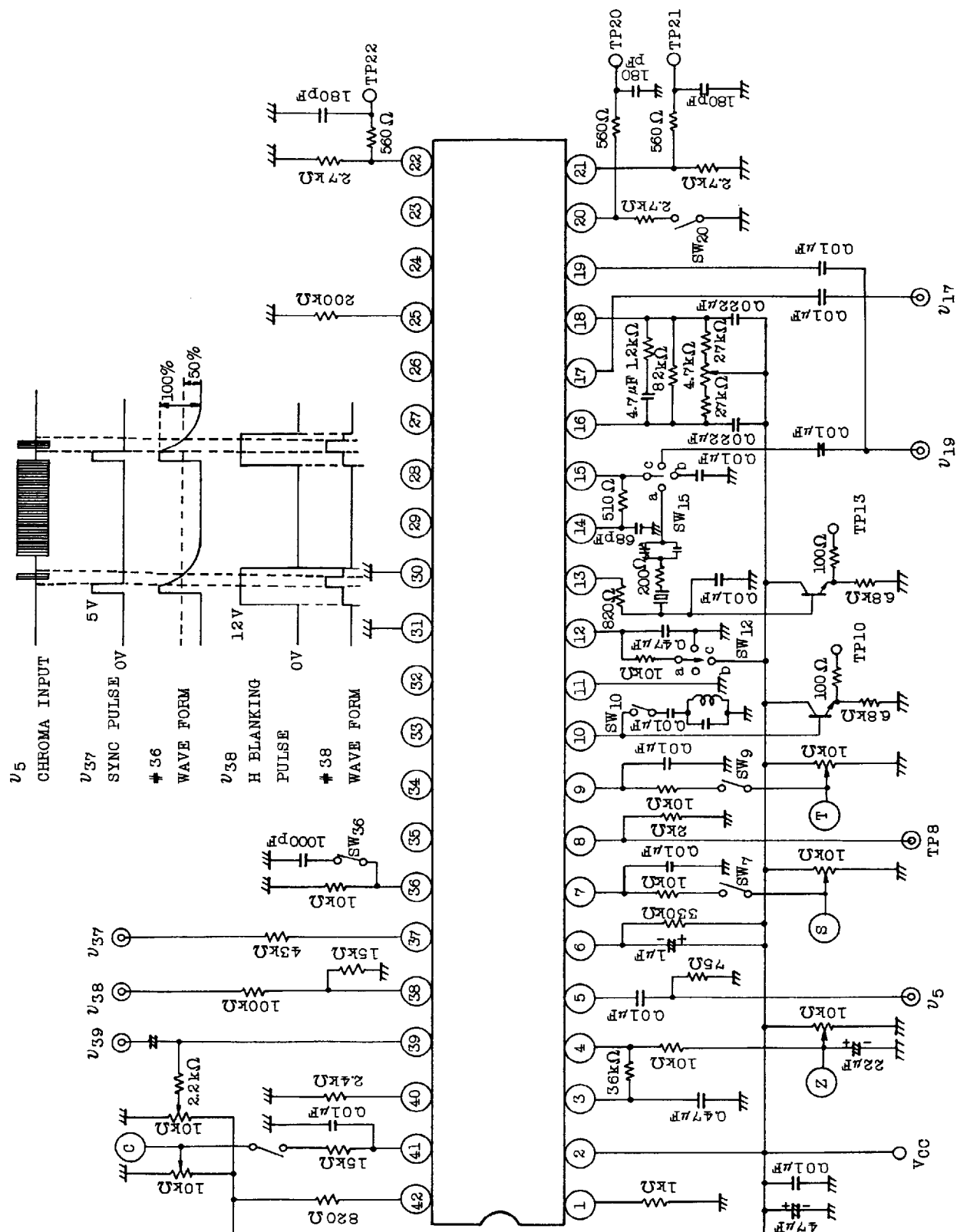
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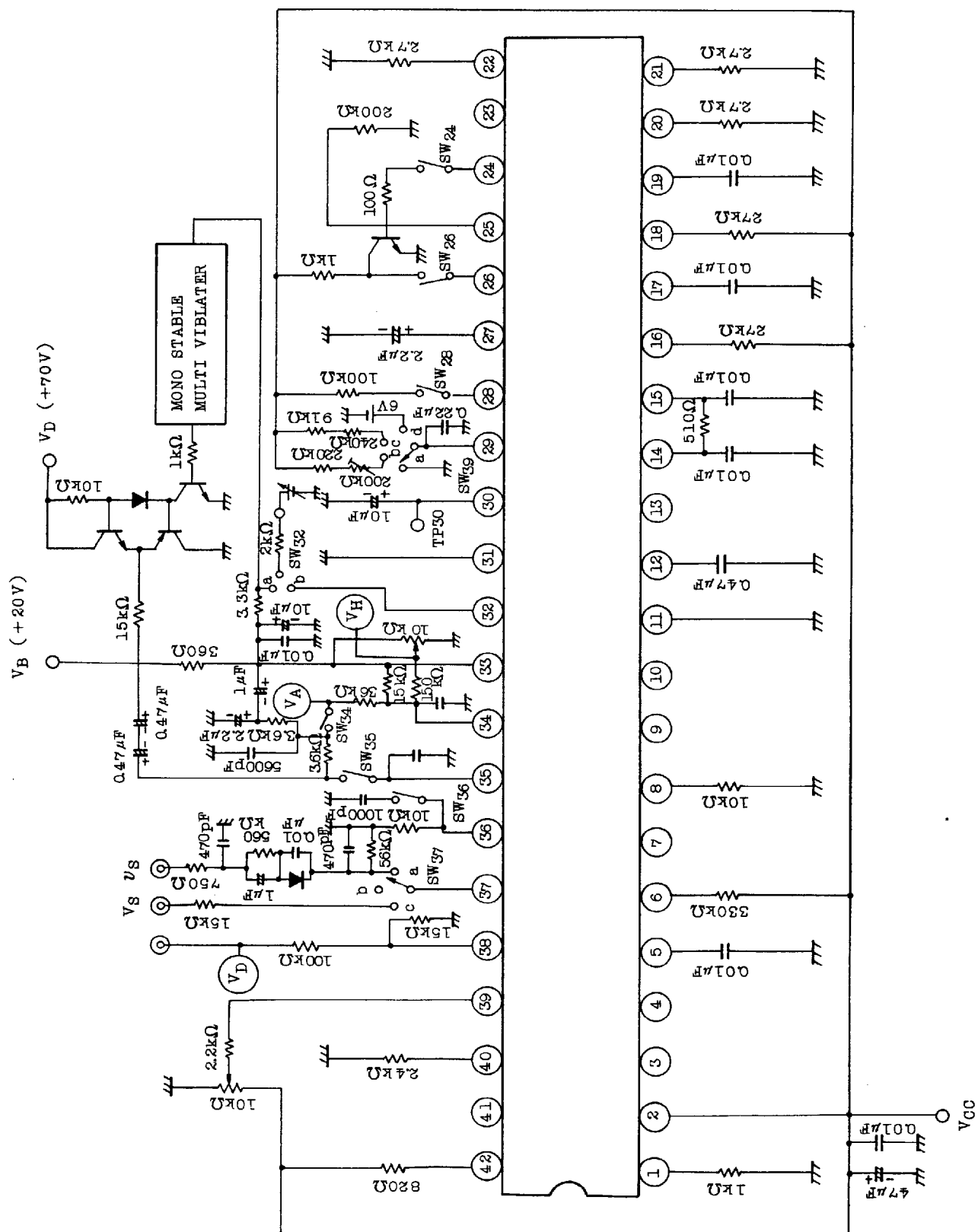
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TEST CIRCUIT 3. Chroma (PAL)



[illegible]

TEST CIRCUIT 5. Deflection



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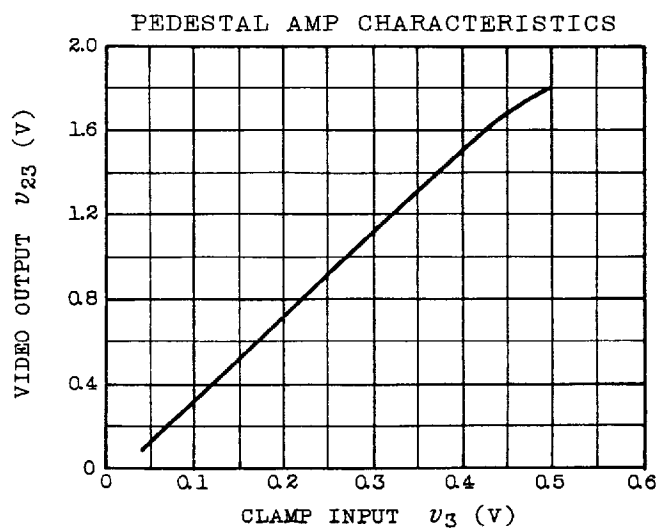
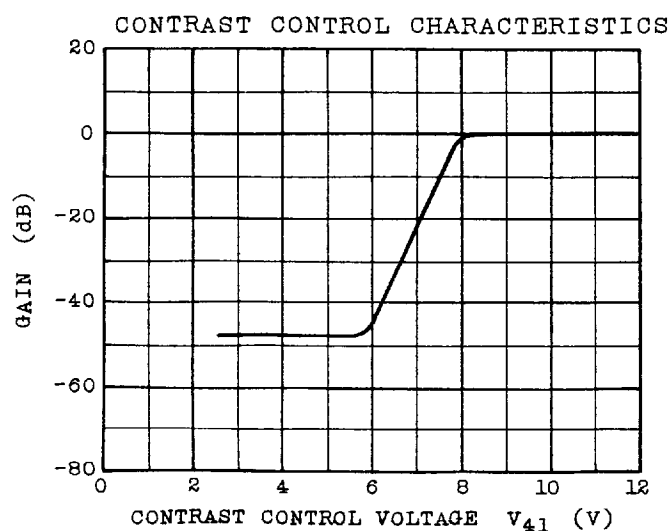
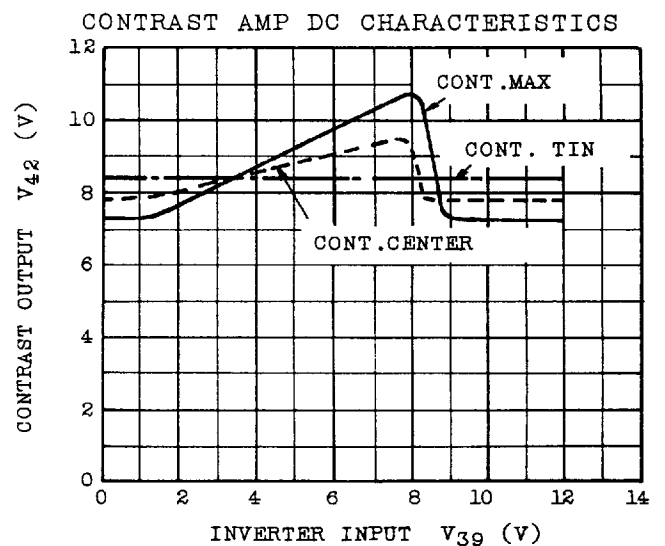
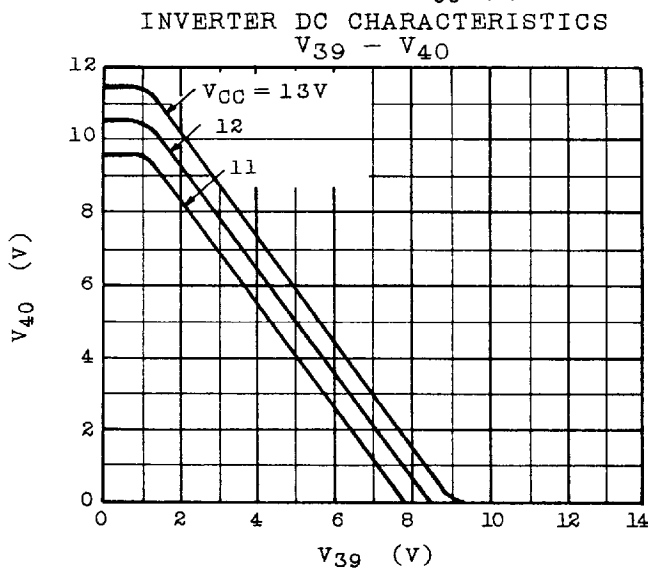
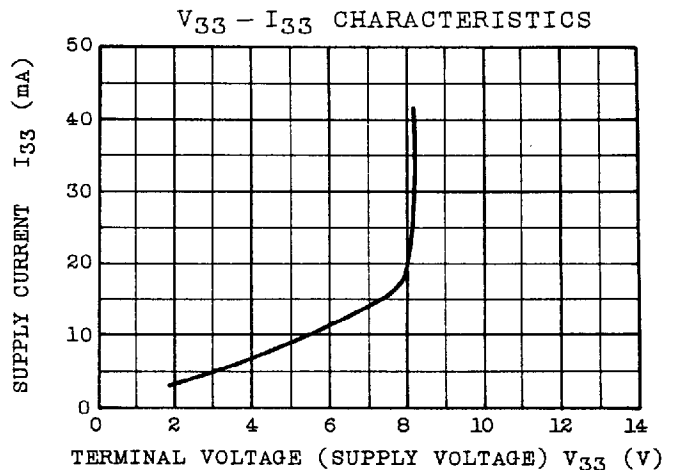
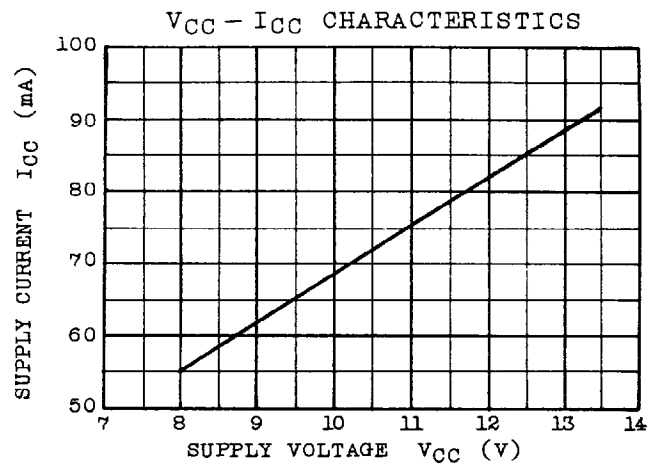
TOSHIBA CORPORATION

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TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

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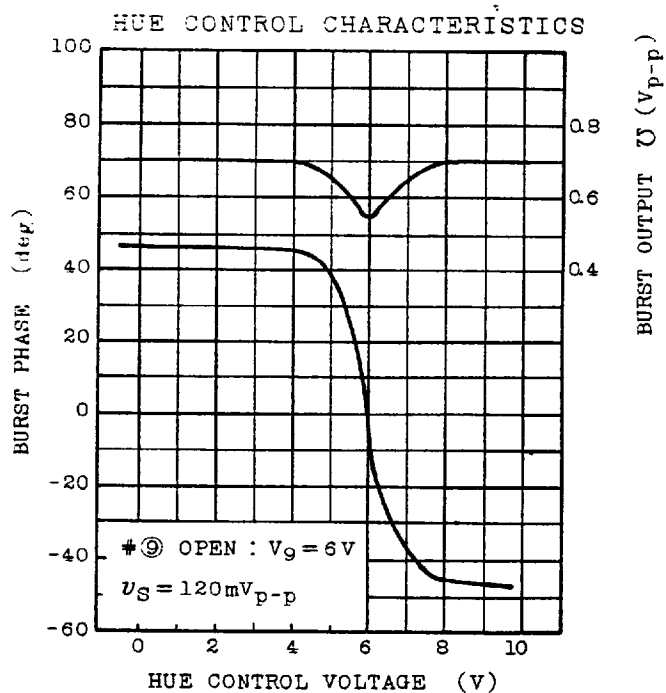
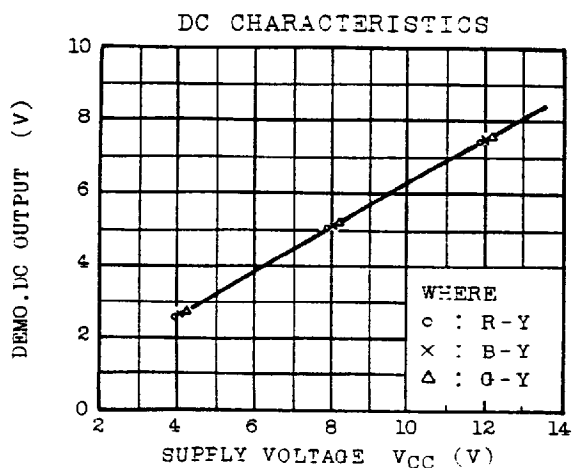
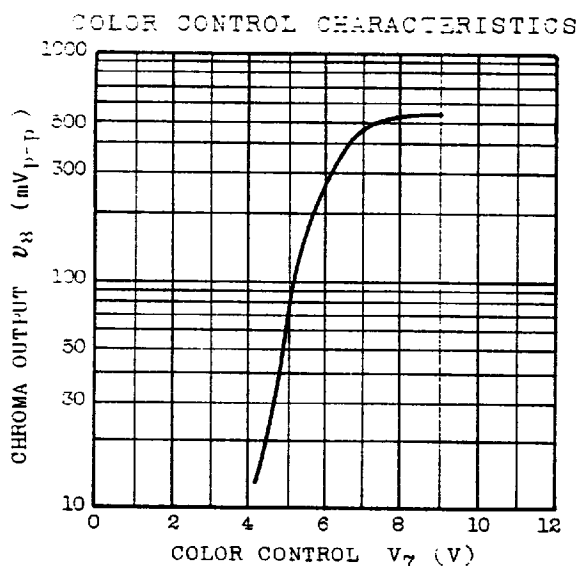
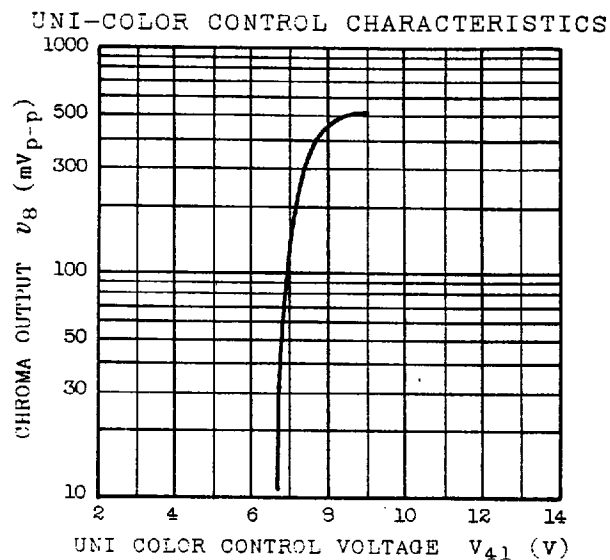
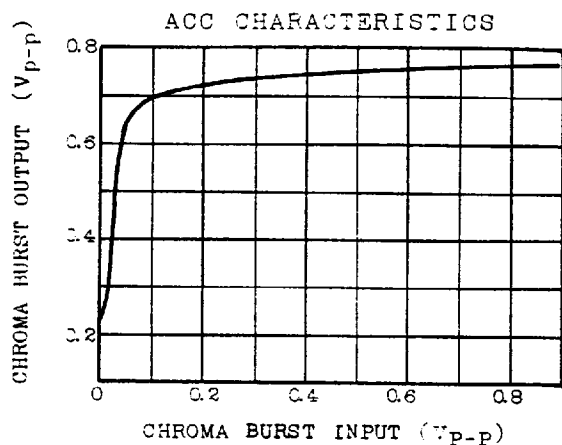
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TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

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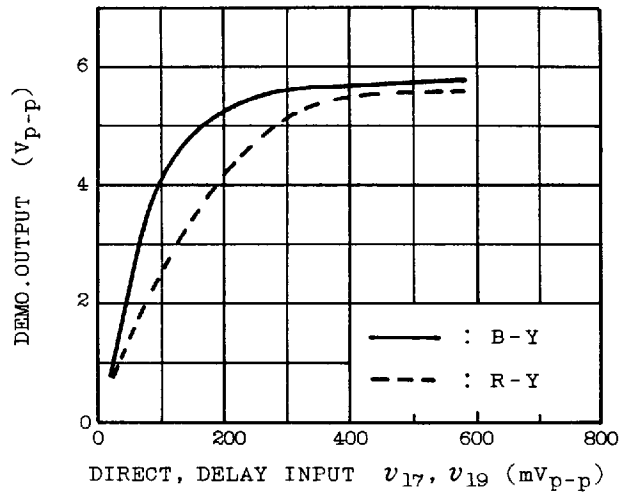
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INTEGRATED CIRCUIT

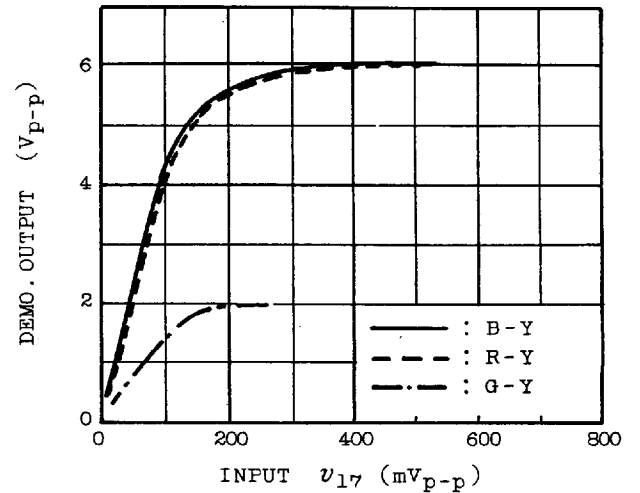
TECHNICAL DATA

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DEMO.OUTPUT CHARACTERISTICS (PAL)



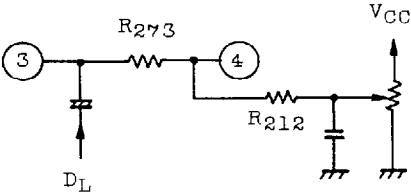
DEMO.OUTPUT CHARACTERISTICS (NTSC)



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TOSHIBA CORPORATION

TERMINAL DESCRIPTION (1)

TERMINAL		FUNCTION
1	Emitter Peaking	An Emitter-output of the contrast amplifier. Contrast gain and peaking characteristics are determined by a ratio of load impedances connected to #1 and #42 terminal.
2	V _{CC1}	Supply terminal for Video, Chroma, Sync Sep and vertical Deflection. 12V typ is recommended.
3	Pedestal Clamp Input	Delayed video signal is applied. The typical gain of the pedestal amplifier is 12.6dB.
4	Brightness Control*	Control terminal of Brightness (DC level of -Y output). The DC restoration ratio is adjustable by superposing video signal component from the pedestal clamp input. 
5	Chroma Input	Chroma signal from a chroma take off coil is applied. The typical input level is 120mVp-p burst amplitude.
6	ACC Filter	Filter capacitor is connected.
7	Color Control* (Killer Output)	Control terminal of color saturation. Terminal voltage of #7 turns to low level when color Killer operates.
8	Chroma Output	Output terminal of chroma signal which is color controled, uni-color controled and burst gated.

TERMINAL DISCRIPTION (2)

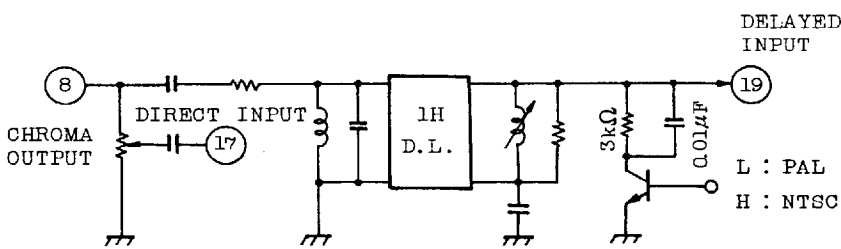
TERMINAL		FUNCTION
9	Tint (Hue) Control*	Control terminal of Tint (Hue). Burst phase is controled.
10	Burst Cleaning	Burst cleaner (tuned Tank) is connected. Burst signal at this terminal is already phase-shifted by Tint control(NTSC). It is possible to set a phase shift between burst signal and chroma signal by the tank circuit alingment.
11	GND 1	GND terminal for Video and Chroma section. Suitable de-coupling capacitor should be connected between V _{CC} 1 and GND 1.
12	Killer Ident Filter	A capacitor for an ident filter is connected. The terminal voltage is V _{CC} (color), 8V typ (B/W) and GND (Ident).
13 14 15	X'tal Drive -45° Input 0° Input	Terminals for a sub-carrier oscillator. A X'tal is connected between #13 and #15 and a 45° ($\frac{\pi}{4}$) phase shift circuit is between #15 and #14. Reference vectors for color demodulator, APC detector and Killer/Ident detector are composed from sub-carrier signals of #14 and #15.
16 18	APC Filter	APC Filter circuit is connected. Two terminals are provided for reducing internal off-set.
17	Direct Dig. Input	Chroma signal from #8 (chroma output) is attenuated and applied to this terminal. The input level is 0.25Vp-p typ. (Burst level). When PAL application, input levels of #17 and #19 should be the same. Internal PAL matrix circuit reduces cross-talk between the direct signal and delayed signal. When NTSC application, internal gain changes to keep the same demodulator outputs as PAL-application.

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TOSHIBA CORPORATION

TERMINAL DISCRIPTION (3)

TERMINAL			FUNCTION																																	
19	Delayed Signal Input PAL/NTSC System SW		Chroma signal from #8 (Chroma Output) is applied to this terminal through an 1H delay line. The input level is 0.25Vp-p typ. (Burst level). PAL/NTSC System SW Function When #19 terminal voltage is below 2V, internal switch turns to NTSC mode. To reduce external parts number, an application circuit shown below is recommendable.																																	
																																				
			A transistor switch shunt the delayed chroma signal and shift #19 DC voltage below 2V.																																	
				<table><tr><th rowspan="2"></th><th colspan="2">RELATIVE PHASE</th><th colspan="2">RELATIVE AMPLITUDE</th><th rowspan="2">MATRIX</th><th rowspan="2">TINT CONTROL</th><th rowspan="2">FLIP·FLOP</th></tr><tr><th>R-Y</th><th>G-Y</th><th>B-Y/R-Y</th><th>G-Y/B-Y</th></tr><tr><td>PAL</td><td>±90°</td><td>230°</td><td>1.78</td><td>0.58</td><td>PAL</td><td>OFF</td><td>ON</td></tr><tr><td>NTSC</td><td>105°</td><td>235°</td><td>0.95</td><td>0.31</td><td>NTSC</td><td>ON</td><td>STOP</td></tr></table>			RELATIVE PHASE		RELATIVE AMPLITUDE		MATRIX	TINT CONTROL	FLIP·FLOP	R-Y	G-Y	B-Y/R-Y	G-Y/B-Y	PAL	±90°	230°	1.78	0.58	PAL	OFF	ON	NTSC	105°	235°	0.95	0.31	NTSC	ON	STOP			
	RELATIVE PHASE		RELATIVE AMPLITUDE		MATRIX		TINT CONTROL	FLIP·FLOP																												
	R-Y	G-Y	B-Y/R-Y	G-Y/B-Y																																
PAL	±90°	230°	1.78	0.58	PAL	OFF	ON																													
NTSC	105°	235°	0.95	0.31	NTSC	ON	STOP																													
20	G-Y Output		G-Y demodulator output terminal/Uni-color switch. When a load resistor is connected between #20 and GND, G-Y output and Uni-color function are enabled. When #20 is open, Uni-color function is disabled and #41 controls only contrast for PAL/SECAM or PAL/NTSC/SECAM applications.																																	
21	R-Y Output		R-Y demodulator output terminal.																																	
22	B-Y Output		B-Y demodulator output terminal.																																	

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TOSHIBA**INTEGRATED CIRCUIT****TECHNICAL DATA****TA7698AP**

TERMINAL DISCRIPTION (4)

TERMINAL		FUNCTION
23	-Y Output	Output terminal of -Y (Luminance) signal which is contrast/brightness controled.
24	Vertical Output	Vertical driver output terminal (Emitter follower). It is capable to drive SRPP output circuit directly.
25	Vertical Height	Constant current discharge rate of ramp capacitor connected #27 terminal is determined by a resistor value which connected between this terminal and GND. (Vertical amplitude is in the propotion of the discharge rate).
26	NFB	NFB terminal for DC/AC. NFB wave form is compared with ramp wave form of #27 terminal.
27	Ramp Capacitor	A ramp capacitor is connected. It should be stable and having low $\tan \delta$ value. (2.2 μ F tantalum capacitor is recommended.) The ramp capacitor is charged to a reference voltage determined internally during retrace period, and discharged constantly to get required linearity during trace period.
28	Vertical Sync Input (V. trig.)	Composite sync signal from #36 (Sync Output) is integrated and applied to this terminal.
29	Vertical Oscillator Timing Constant	CR timing constant for vertical oscillator is connected. Vertical retrace time is determined the timing resistor value and internal discharge resistor value.
30	X-ray Protector	SCR type X-ray protector. The threshold is 0.9V typ. When X-ray protector operate, horizontal drive output #32 turns to low level. It also operates when #32 voltage exceeds 9V (typ.).
31	GND 2	GND terminal for Vertical/Horizontal, AFC and Synce Separator. De-coupling capacitors from VCC1 and VCC2 should be connected to this GND.

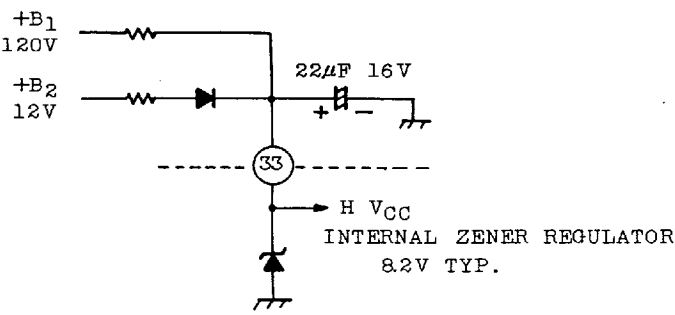
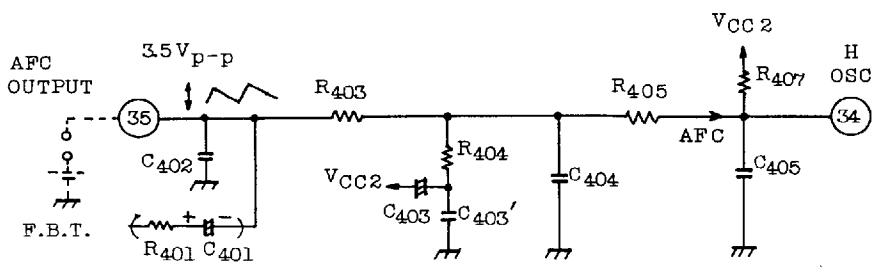
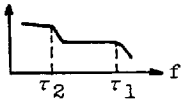
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TOSHIBA CORPORATION

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TERMINAL DISCRIPTION (5)

TERMINAL		FUNCTION
32	H. Drive Output	Open collector output for Horizontal driver. External load resistor is required.
33	V _{CC2} (H. V _{CC})	Supply terminal for horizontal deflection circuit starting up. 
34	Horizontal Oscillator Timing Constant	2f _H oscillator timing CR is connected. Thermal co-efficient of this CR should be selected to compensate f _H thermal drift which is specified.
35	AFC Output	I/O terminal of horizontal AFC circuit. The refference voltage of AFC is 4.5V typ..  C402 : Flyback Pulse integral capacitor C405, R407 : Horizontal Osc. Timing constant R403, C404 : AFC time constant τ_1 R404, C403, C403' : AFC τ_2 R405 : Determines AFC control sensitivity. 

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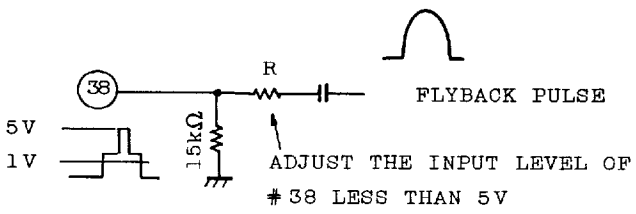
TOSHIBA CORPORATION

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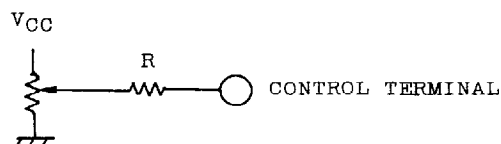
TERMINAL DISCRIPTION (6)

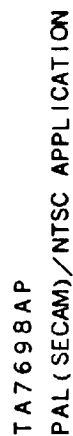
TERMINAL		FUNCTION
36	Sync. Sep. Output	Output terminal of composite sync signal/Timing constant for gate pulse generation. Falling edge of the gate pulse (t_2) is adjusted by external capacitor and resistor. Rising edge (t_1) is internally determined. If adjustment of t_1 is required, a capacitor which connected between #37 (Sync. Sep. Input) and GND will be changed to shift sync signal timing. COMPOSITE VIDEO SIGNAL # 37 OUTPUT INTERNAL GATE PULSE t_1 t_2 t_2' 8.4V $V_{th} = 4.2V$ Generated gate pulse is masked by flyback pulse from #38, and applied to the pedestal clamp circuit and the burst gate circuit.
37	Sync Sep. Input	Input terminal of the base-time constant type sync separator. Composite video signal from #40 (Inverter Output) is applied through sync sep. time constant circuit. Slice level of horizontal sync and vertical sync can be set independently. INVERTER OUTPUT (40) R206 R301 R302 C301 D301 C302 R303 C303 37 SYNC SEP. INPUT R206 : #40 load resistor R301, C302, R303 : Horizontal sync slice level R301, C301, R302 : Vertical sync slice level D301 : Timing constant separation C303 : Noise Filter/Gate pulse rising edge timing. To deepen the slice level Horizontal : R301 increase or R303 decrease Vertical : R301 increase or R302 decrease

TERMINAL DISCRIPTION (7)

TERMINAL		FUNCTION
38	Flyback Pulse Input	Input terminal of flyback pulse for flip-flop driving, horizontal blanking and gate pulse masking. Pulse height of flyback pulse should be less than 5V. #38 terminal voltage is clamped to 5V during gate pulse period. 
39	Inverter Amp. Input	Composite video signal from PIF is applied directly. Input dynamic range is 2.0V to 6.5V. (Sync negative composite video is required.)
40	Inverter Amp. Output	Output terminal of the inverter amplifier. The output signal is applied to the sync. separator and the chroma band pass circuit.
41	Contrast Control*	Contrast/Contrast-Uni-color control See #20
42	Contrast Amp. Output	Collector output of contrast amplifier. See #1. #42 terminal voltage (operating) should be above 6V.

* Control sensitivity of each control terminal is adjustable by a series resistor R.





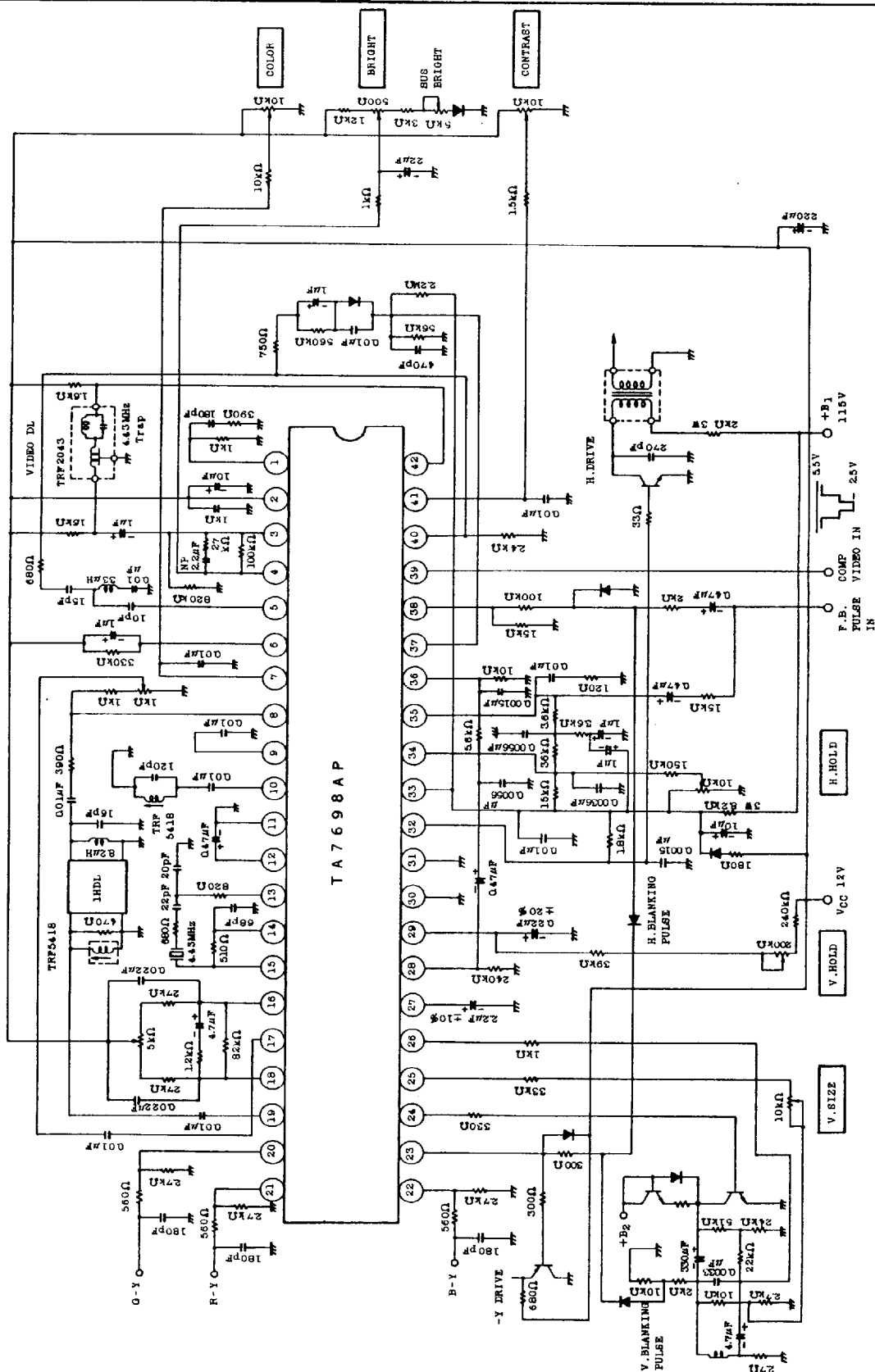
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TOSHIBA INTEGRATED CIRCUIT

TECHNICAL DATA

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PAL APPLICATION

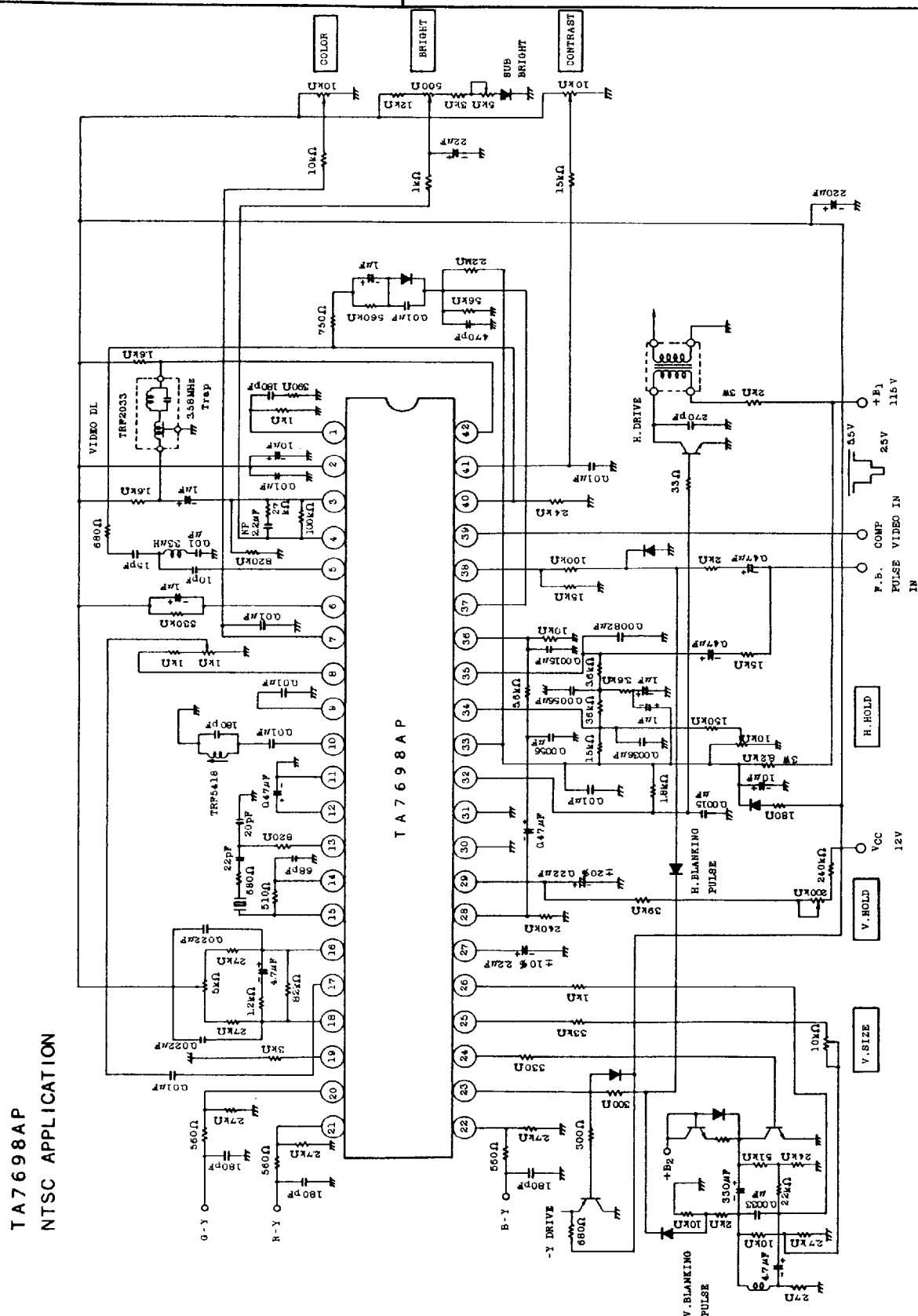


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NTSC APPLICATION

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